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DESIGN AND IMPLEMENTATION OF VLSI ARCHITECTURE FOR ACCURATE ADER

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ABSTRACT: Approximation can increase performance or reduce power consumption with a simplified or inaccurate circuit in application contexts where strict requirements are relaxed. For applications related to human senses, approximate arithmetic can be used to generate sufficient results rather than absolutely accurate results. Approximate design exploits a tradeoff of accuracy in computation versus performance and power. However, required accuracy varies according to applications, and 100% accurate results are still required in some situations. In this project, design and implementation of VLSI architecture for accurate adder is proposed. This accurate adder performed in three stages, they are propagate and generate stage, black& gray cell stage and Post processing stage. In this propagator and generator signals are generated by using propagate and generate stage. Black and Gray cell stage will generate the carry. The accurate operation is also performed for the carry generated signals in order to reduce the critical path delay and improve performance. Then the post processing stage will take the output of accurate adder then performs the operation and gives sum and carry as output. At last from results it can observe that the propose system gives effective results.

KEYWORDS: VLSI, Accurate Adder, propagate and generate stage, Post processing Stage, propagator, Generator, Black cell & Gray Cell.

I. INTRODUCTION

Fastest technologies are developed in present days. In present days, reduction of device size, fast operation and low power consumption are required. The designing of low power VLSI system has more demand in mobile communication. Due to the device designed by designer with high speed, low power consumption and small silicon area, the device is available with low power. ALU (Arithmetic logic unit) and FU (Floating point unit) are the main parts in computations [1].

Logical computations are addition, subtraction, multiplication, division and logical operations are AND, OR, INV and comparison which are processed by Arithmetic logic unit (ALU). Data path has an important role in digital signal processors and microprocessors because of some characteristics such as power consumption, speed of operation and die-area.

Data path contains complex operations are subtraction, addition, division and multiplication [2]. The main important factor is data path performance which is affected by efficient hardware units of complex computations. In the data path addition is the important executed operation, addition operation contains binary adder to add given numbers. In complex computations such as decimal operations, multiplication and division, adders has important task [3]. To get data path efficiently, the implementation of binary adder should be efficient. In central processing unit (CPU) crucial element is ALU (Arithmetic logic unit). In ALU and general processors to get better performance, efficient adder is needed. From 1950s, for hardware implementation of VLSI arithmetic circuits, research started on efficient adder implementation. In control systems and digital signal processing main operation is the addition.

The properties of system or processor like accuracy and speed depends upon the performance of adder. To execute the addition of numbers, adder is used which is a digital circuit. Different processors and computers contains ALU in which adder is used. To reduce different parameters, different designs have been implemented based on parallel and serial structures. Four elementary operations are performed in binary addition [4].

The designers often look forward to fast adders while optimizing their design, because for most of the computations they often contribute in setting the critical path. The carry chain of the binary addition is the major stumbling block, it increases with increasing input operands. The worst case comes into picture when the carry covers the farthest distance (LSB to MSB). Hence the prime concern for efficient adder design is to have accelerated carry chain, because elimination of carry chain is not practical. In the last decade different types of adder architectures have been studied for performance improvement. For lower number of bits, adders like Ripple Carry Adder, Carry Lookahead Adder (CLA) are sufficient [5]. However, for higher bit count, the delay increases due to longer carry chains, so Parallel Prefix Adders are preferred. Parallel Prefix Adders are high speed adders as they incur small delay and are also area efficient. Its prime advantage is parallel carry generation, because of which, the number of logic levels (N) is lessened.

II. EXISTING DESIGN

The functional unit of VLSI systems and application specific DSP architectures performance is totally depends upon adders. The filters are widely used in DSP for removing unwanted features from a signal in order to improve the quality of the signal and it is used in communication system applications such as echo cancellation, noise reduction, speech and waveform synthesis etc. Adders are widely used in the different types of the digital filter applications. The design performance will be degraded, when adders are consumes large energy (or) processed as too slow. Approximation addition has been carried out for achieving area, power and speed improvements at the accuracy in the field.

Approximate computing is one of the emerging compute techniques that is considered to be a potential alternative to accurate computing to achieve a greater energy efficiency in computing [6]. However, this would be realized at the expense of an acceptable compromise in the computational accuracy. For many multimedia applications, a slight deviation from the correct result is often considered to be acceptable and this is due to the inherent limitations of human perception. For example, minor distortions in an image, minor aberrations in video frames, and a feeble noise in an audio are not discernible by humans. This has opened up the possibility for computing to be made less accurate (i.e., approximate) rather than accurate while being deemed acceptable for a practical application. Thus far, approximation has been successfully considered for digital image, audio and video processing, neuromorphic computing, big data analytics and data mining, low power graphics processing, and software engineering etc. to explore its practical viability. Research on approximate computing hardware has predominantly focused on the designs of approximate arithmetic circuits [7] such as approximate adders and multipliers, and approximate logic circuits [8].

This With the continuous scaling of physical dimension of CMOS to a few tens of nanometres, it is becoming increasingly difficult to improve circuit performance and/or to enhance power. Approximate computing has been advocated as a new emerging approach for saving area and power dissipation, as well as increasing performance at a limited loss in accuracy [9]. While in general computation errors are not desirable, applications such as multimedia processing, wireless communications, recognition, machine learning and data mining are tolerant to some error. Due to the statistical nature of digital signal processing, small errors in computation would not impose noticeable degradation in performance.

Basically, there are two types of methodologies for improving speed and energy efficiency by approximation. The first one is voltage-over-scaling (VOS) technique for CMOS circuits to save power. While the VOS technique is applicable to most circuit for error tolerant application the problem with VOS technique is that errors mostly occur at the timing-critical path associated with the most significant bits (MSBs), i.e., errors are often large. The second technique is based on redesigning a logic circuit into its an approximate version. An approximate redesign pertains to the functionalities of different logic circuit. Many approximate adder designs have been developed.

Approximate Adders for approximate multiplication Document The gap between capabilities of CMOS technology scaling and requirements of future application workloads is the so-called normalized error distance) can meet with respect to circuit-based figures of merit of a design (number of transistors, delay and power consumption. There are several promising design approaches that jointly can reduce this gap significantly. Approximate computing is an attractive paradigm for digital processing at anemometric scales. Inexact computing is particularly interesting for computer arithmetic designs [10].

III. PROPOSED DESIGN

The below figure (1) shows the block diagram of proposed accurate adder. The proposed adder technique is a parallel prefix adder. However, it has three-stage structures to compute the addition of binary input operands such as propagate and generate block stage, black and gray cell, and post processing stages. The logical expressions and operations of all these four stages are described as follows.

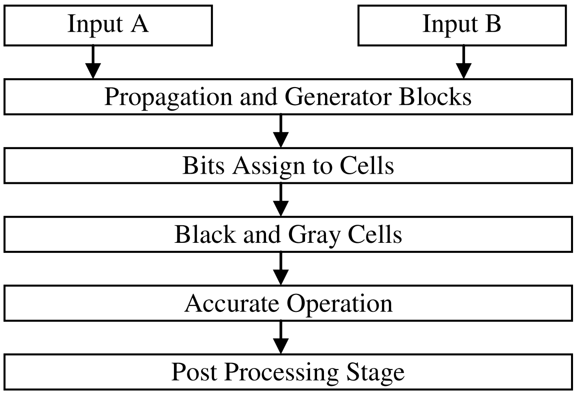

Fig. 1: BLOCK DIAGRAM OF HYBRID ADDER

In this propagator and generator signals are generated by using propagator and generator blocks by taking input A and Input B. Then result is assigned to the cell structure. In the cell structure gray cell and black cells are used to perform addition operation on propagator and generator signals and generates the carry. Then the accurate operation is performed while carry generation. Finally Post processing stage performs XOR operation on carry with propagate signal and generates the output of accurate adder sum as output. Three stages are presented in the accurate adder structure is explained in detail manner.

3.1 Propagator and Generator Stage

This stage consists of computation of propagate and generate bits with respect to each pair of input operands (A_i and B_i). According to prefix computation G_i (generate) and P_i (propagate) signals are defined first by the equations below:

$$P_i = A_i \oplus B_i \text{ -------- (1)}$$

$$G_i = A_i \cdot B_i \text{ ------ (2)}$$

3.2 BLACK CELL & GARY CELL

Then in prefix computation, all carry signals are computed in parallel. In this stage, generate and propagate carries are computed corresponding to each bit and are used as intermediate signals for further computation. Carry generation network consists of the processing elements and buffer elements. Figure (4.2) shows the block diagram of gray cell and black cells. The overall network delay is directly proportional to the number of black cells present. The output is same as that of input for the gray cell. The output of black cell is characterized as:

$$P_{out} = P_{in1} \cdot P_{in2} \text{ ------- (3)}$$

$$G_{out} = G_{in1} + (P_{in1} \cdot G_{in2}) \text{ ------- (4)}$$

3.3 Accurate Operation

In a conventional adder circuit, the delay is mainly attributed to the carry propagation chain along the critical path, from the Least Significant Bit (LSB) to the Most Significant Bit (MSB). Meanwhile, a significant proportion of the power consumption of an adder is due to the glitches that are caused by the carry propagation. Therefore, if the carry propagation can be eliminated or curtailed, a great improvement in speed performance and power consumption can be achieved. In this study, we propose for the first time, an innovative and novel addition arithmetic that can attain great saving in accuracy, speed and power consumption

To minimize error due to the elimination of the carry chain every bit position is being checked from left to right (MSB -LSB) starting from right of demarcation line. If both input bits are "0" or different, normal one-bit addition is performed and the operation, Proceeds to next bit position. The checking process is stopped when both input bits are encountered as high i.e., 1, and from this bit onwards, all sum bits to the right (LSB) are set to "1." This is how this adder attains accuracy by reducing errors and saves carry propagation delay and enhances the overall performance.

3.4 Post Processing Stage

In post processing stage the calculation is performed based on the input bits. From post processing stage sum and carry is generated. This stage is where the overall adder operation is completed, the carry signals of the second stage will pass through to the final stage (i.e.,) Post-Processing Stage. The final result of the entire adder operation is obtained. Using the intermediate signals propagate and the carry signals a sum result can be found by using another exclusive-OR gate. Fig. 2 shows the way of calculating the prefix.

$$S_i = P_i \oplus G_{i-1} \text{ ----- (5)}$$

In applications of high speed circuits, very useful adder is PPA. PPA is designed based on the power and area.

Structure delay= $\log_2 n$
Number of computation nodes= $[(n)(\log_2 n)-n+1]$

IV. RESULTS

The Xilinx design environment was used to implement and examine the developed algorithm. The FPGA architecture of proposed accurate adder design is shown in Fig. 3 and Fig. 4. The below Fig. 3 and Fig. 4 show the RTL schematic and technology schematic of Proposed accurate adder. RTL schematic is the combination of inputs and outputs.

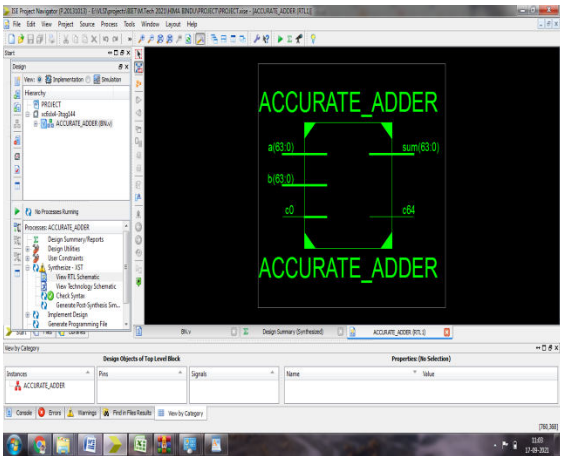

Fig. 3: RTL SCHEMATIC OF PROPOSED ADDER

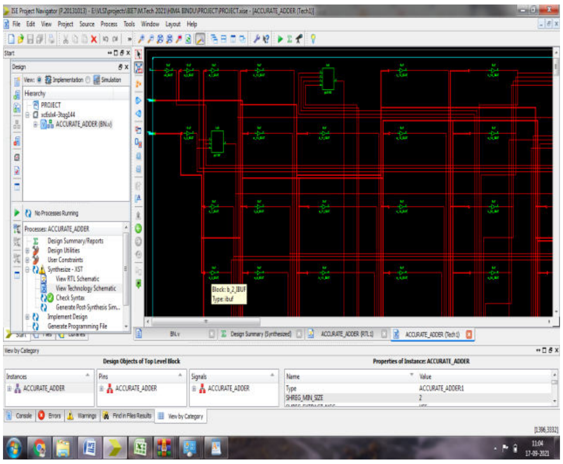

Fig. 4: TECHNOLOGY SCHEMATIC OF PROPOSED ADDER

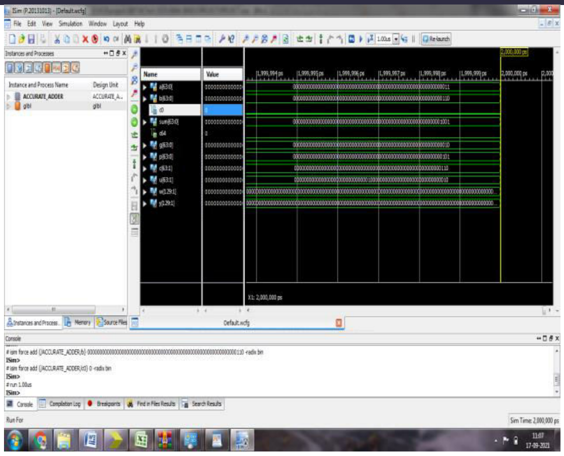

Fig. 5: OUTPUT WAVEFORM OF PROPOSED ADDER

V. CONCLUSION

The design and implementation of VLSI architecture for accurate adder is presented in this document. Generate and propagate signals are generated to increase the speed of operation. The proposed adder design was implemented with the help of black cell and gray cell operations for carry generation and propagation. The accurate operation stage plays important role in entire operation. This design is simulated in Xilinx software. Hence from simulation results, it can observe that accurate adder gives effective result.

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