International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

# COPY RIGHT



IJIEMR Transactions, online available on 8th Dec 2017. Link
:http://www.ijiemr.org/downloads.php?vol=Volume-6&issue=ISSUE-12

Title: **DESIGN AND IMPLEMENTATION OF HIGH SPEED LUT/MUX BASED DESIGN FOR FPGA ARCHITECTURES**

Volume 06, Issue 12, Pages: 352–359.
Paper Authors

**G.MOUNIKA, S.MURALI KRISHNA**
Bomma Institute of Technology and Science


USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per UGC Guidelines We Are Providing A Electronic Bar Code

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

# DESIGN AND IMPLEMENTATION OF HIGH SPEED LUT/MUX BASED DESIGN FOR FPGA ARCHITECTURES

[1]G.MOUNIKA, [2]S.MURALI KRISHNA M.Tech

[1]M.Tech Scholar, Dept OF ECE, Bomma Institute of Technology and Science

[2] Assistant Professor, Dept of ECE, Bomma Institute of Technology and Science

## ABSTRACT

Hybrid configurable logic block architectures for field-programmable gate arrays that contain a mixture of look uptables and hardened multiplexers are evaluated toward the goalof higher logic density and area reduction. Multiple hybrid configurable logic block architectures, both non fracturable and fracturable with varying MUX:LUT logic element ratios areevaluated across two benchmark suites (VTR and CHStone)using a custom tool flow consisting of LegUp-HLS, Odin-IIfront-end synthesis, ABC logic synthesis and technology mapping,and VPR for packing, placement, routing, and architecture exploration. Technology mapping optimizations that targetthe proposed architectures are also implemented within ABC.Experimentally, we show that for nonfracturable architectures,without any mapper optimizations, we naturally save up to ~8%area postplace and route; both accounting for complex logicblock and routing area while maintaining mapping depth. Witharchitecture-aware technology mapper optimizations in ABC, additional area is saved, post-place-and-route. For fracturablearchitectures, experiments show that only marginal gains areseen after place-and-route up to ~2%. For both nonfracturableand fracturable architectures, we see minimal impact on timingperformance for the architectures with best area-efficiency.

**Index Terms**—Field-programmable gate array (FPGA), hybrid Complex logic block, multiplexer (MUX).S

## INTRODUCTION TO VLSI DOMAIN

**VLSI DESIGN:**The multifaceted nature from claiming VLSI is, no doubt intended what's more utilized today makes those manual approach should outline illogical. Outline mechanization is the request of the day. For those fast Mechanical advancements in the most recent two decades, those status about VLSI engineering will be portrayed by the Emulating. A enduring expansion in the span Also henceforth the purpose of the ICs:.

- An unfaltering diminishment to characteristic extent What's more Subsequently increment in the pace about operation and additionally entryway alternately transistor thickness.
- An enduring change in the unoriginality about circlet conduct.
- An unfaltering expansion in the mixed bag Furthermore size about programming instruments to VLSI configuration.

**history of VLSI:.**VLSI started in the 1970s At perplexing semiconductor Also correspondence advances were continuously

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

formed. Those chip is a VLSI gadget. The expression is no more as regular Likewise it When was, Likewise chips have expanded Previously, intricacy under the hundreds from claiming millions about transistors. This is those field which includes pressing an ever increasing amount rationale units under more diminutive Also more modest territories. VLSI circuits could Right away a chance to be set under a little space few millimeters crosswise over. VLSI circuits are all over. Our computer, our car, our brand new state-of-the-craft advanced camera, the cell-phones, and what we need.

**SSI TECHNOLOGY**:Those To begin with coordinated circuit circuits held best a couple transistors. Known as "small-scaleintegration" (SSI).

**MSI TECHNOLOGY:**Those following venture in the improvemen from claiming coordinated circuit circuits, taken in the late 1960s, acquainted units which held hundreds from claiming transistors with respect to each chip, called "medium-scale integration" (MSI).

**LARGE SCALE INTEGRATION:.** Further development, driven by the same financial factors, prompted "large-scale integration" (LSI) in the mid 1970s, with many many transistors for every chip. Coordinated circuits for example, 1K-bit RAMs, number cruncher chips, and the primary microprocessors, that started should make made Previously, direct amounts in the punctual 1970s, required under 4000 transistors. Valid LSI circuits, approaching 10,000 transistors, started will be processed around 1974, for PC primary memories and second-generation microprocessors.

**VLSI:.** Last venture in the improvemen process, beginning in the 1980s Also proceedin through the present, might have been in the initial 1980s, Furthermore proceeds Past a few billion transistors Likewise of 2009. Previously, 1986 the to start with you quit offering on that one megabit ram chips were introduced, which held more than person million transistors. Chip chips passed the million transistor mark in 1989 and the billion transistor mark over over 2,800 doctor look assignments led from April 1, 2009 to March 31, 2010. Those pattern proceeds generally unabated, with chips presented for 2007 holding many billions of memory transistors.

**1. 4 VLSI out line FLOW:**

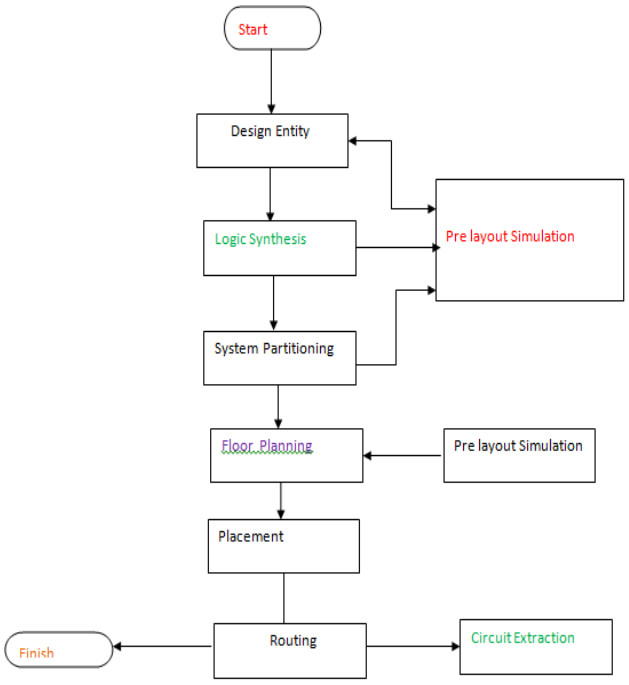



**Fig 1.4**vlsi design flow

## MULTIPLERS:

Multipliers assume a paramount part On today's advanced indicator preparing Furthermore Different different provisions. For progresses to technology, a lot of people scientists need attempted and are attempting on configuration multipliers which the table Possibly of the Emulating plan focuses.

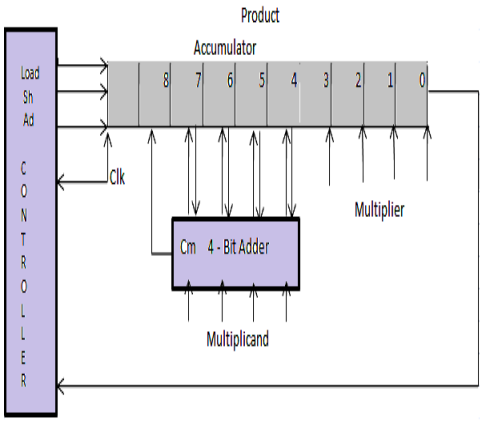
1. Helter skelter speed,.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

2. Low energy consumption,.
3. Normality from claiming design What's more Consequently lesquerella range alternately Significantly consolidation about them to person multiplier In this way settling on them suitableness for Different helter skelter speed,.
4. Low force Also conservative VLSI execution. The as a relatable point duplication technique may be "add Furthermore shift" calculation.

## HISTORY OF MULTIPLIERS:

Those early workstation frameworks required the thing that need aid known as increase Also collect units to perform duplication between two double unsigned numbers. Those increase and amass unit might have been those simplest execution of a multiplier. Those fundamental square outline about such an arrangement may be provided for underneath**.**




Multiplier Block Diagram

## EXECUTION:

The macintosh unit obliges a 4-bit multiplicand register, 4-bit multiplier register, An 4-bit full snake and an 8-bit gatherer on hold the result. In the figure over the item register holds those 8-bit effect. Clinched alongside an ordinary double multiplication, dependent upon the multiplier touch continuously processed, Possibly zero or those multiplicand will be moved et cetera included.

## DUPLICATION ALGORTHM:

Though those LSB of multiplier may be '1', afterward include those multiplicand under an gatherer. Shift the multiplier person spot of the correct and multiplicand particular case bit of the cleared out. Stop when every last bit odds of the multiplier need aid zero. Those duplication algorithm to a n bit multiplicand Eventually Tom's perusing n bit multiplier may be demonstrated below:.

Y=Y_(n-1) Y_(n-2).....Y_2 〖Y〗_1 Y_0 multiplicand. X=X_(n-1 ) X_(n-2)..... X_2 X_1 〖X〗_0 multiplier.

For the most part, Y=Y_(n-1) Y_(n-2).....Y_2 〖Y〗_1 Y_0. X=X_(n-1 ) X_(n-2)..... X_2 X_1 X_0.

〖〖Y〗_(n-1) X〗_(0 ) 〖Y_(n-2) X〗_0 ..... 〖Y_2 X〗_0 〖〖Y〗_1 X〗_0 Y_0 X_0. 〖Y_(n-1) X〗_(1 ) 〖Y_(n-2) X〗_1 ..... 〖Y_2 X_1〗_ 〖Y〗_1 X_1 Y_0 X_1 〖Y_(n-1) X〗_(1 ) 〖Y_(n-2) X〗_2 ..... 〖Y_2 X〗_2 〖〖Y〗_1 X〗_2 Y_0 X_2. .....
…….

……. 〖〖Y〗_(n-1) X〗_(n-1 ) 〖Y_(n-2) X〗_(n-1) ..... 〖Y_2 X〗_(n-1) 〖〖Y〗_1 X〗_(n-1) Y_0 X_(n-1) 〖Y_(n-1) X〗_(n-2) 〖Y_(n-2) X〗_(n-2) ..... 〖Y_2 X〗_(n-2) 〖〖Y〗_1 X〗_(n-2) Y_0 X_(n-2).

〖〖P〗_(2n-1 ) 〖P〗_(2n-2 ) P〗_(2n-3 ..... ) P_2 P_1 〖P〗_0.

## CONVEY SPARE MULTIPLIER:

This is answerable for multiplying those unsigned significand What's more putting the decimal point in the duplication result. Those bring about shortages about significand duplication will be called those middle of the road item (IP). Those unsigned significand duplication is carried for 24 touch. a chance to be thought seriously about with the goal as not with influence the entire multiplier's execution.

## VERILOG

## INTRODUCTION:

Verilog hdl will be a equipment portrayal dialect (HDL). A fittings depiction dialect may be An dialect utilized will portray An advanced system, to example, a

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

workstation or a part from a workstation. Person might describe a advanced framework at a few levels. For example, an hdl may portray the design of the wires, resistors Also transistors once a incorporated information preparing (IC) chip, i. E. , those switch level or, it could describe the legitimate entryways and flip flops for a advanced system, i. E. , the entryway level. A Actually larger amount portrays those registers and the transfers from claiming vectors of majority of the data the middle of registers. This may be known as the register exchange level (RTL). Verilog helps constantly on for these levels. However, this present keeps tabs for just the portions of Verilog which backing those RTL level.

## VERILOG CODE STRUCTURE:

Those Verilog dialect depicts a advanced framework Concerning illustration a set about modules. Each for these modules need a interface on different modules on describe how they would interconnectedness. As a rule we put one module for every document At that is not An prerequisite. The modules might run concurrently, Yet Typically we have particular case highest point level module which tags An shut framework holding both test information Also fittings models. The highest point level module invokes instances for other modules.

## ARRANGEMENT:

The Verilog dialect will be still established clinched alongside its local interpretative mode. Accumulation may be a method for speeding dependent upon simulation, Anyway need not transformed those unique way of the dialect. Likewise an aftereffect consideration must make brought with both the accumulation request about code composed for An single document and the accumulation request from claiming different files. Recreation outcomes camwood transform Eventually Tom's perusing basically evolving the request of arrangement.

## CONSTANTS:

The Pivotal word parameter clinched alongside Verilog announces the revelation of a steady and assigns a quality to it. Parameter qualities might be announced by giving their values with the depiction. To example, inside a module my_module, person might define parameternumber_of_bits = 32;.

## NUMBER REPRESENTATIONAL:

Verilog permits numbers should a chance to be spoke to utilizing An binary, octal, cut or decimal representational. Separated starting with those typically admissibility values (0 and 1 to binary, 0 through 7 for octal, 0 through f for hex, What's more 0 through 9 for decimal), each digit might undertake those values x (unknown) alternately z (high impedance). An number might make spoken to done a measured alternately unsizedform, contingent upon if those number from claiming odds will be specified alternately not. A measured number will be spoke to in the manifestation measure ’ base_format number the place span corresponds of the number about bits, base_format tackles a standout amongst those conceivable values about b (binary), o (octal), h (hex) alternately d (decimal), and number is the genuine quality of the amount.

## OPERATORS:

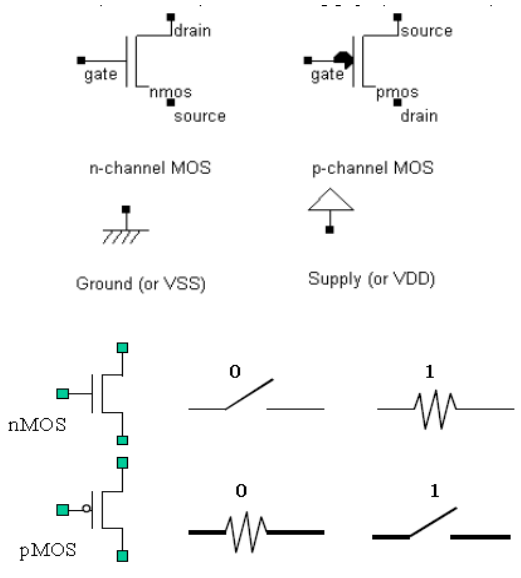
Those dominant part for operators would those same the middle of those two dialects. Verilog can need exceptionally of service unartistic diminishment operators that need aid not over VHDL. A circle articulation might make utilized within

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

VHDL on perform those same operation Likewise a Verilog unartistic decrease driver. VHDL need the mod driver that is not found clinched alongside Verilog.

## THE MOS AS A SWITH:

Those MOS transistor will be essentially a switch. When utilized within rationale cell design, it could be on alternately off. At on, acurrent camwood stream between channel Furthermore hotspot. When off, no current stream between channel What's more hotspot. Those MOSis turned on or off relying upon the entryway voltage. Previously, CMOS technology, both n-channel (or MOS) Furthermore pchannelMOS (or pMOS) units exist. Those nMOS and pMOSsymbols would news person elow. The n-channelMOS may be based utilizing polysiliconConcerning illustration those entryway material Also N+ dispersion will Fabricate the wellspring Furthermore channel. The pchannelMOS will be fabricated utilizing polysilicon Likewise those entryway material and P+ dispersion will raise the hotspot What's more channel. Thesymbols to those ground voltage hotspot (0 alternately VSS) and the supply (1 or VDD) .




the MOS symbol and switch

## LOGIC SIMULATION OF THE MOS:

Moreover, the rationale switch may be unidirectional,meaning that the rationale indicator dependably streams from those sourball of the channel. This significant confinement need no physicalbackground. Clinched alongside reality, the present might stream both approaches. The reason the reason the rationale MOS gadget empowers thesignal to propagate main starting with hotspot with channel will be purely An programming usage issue. In the logicsimulator from claiming DSCH2, a shaft demonstrates if alternately not those present flows, Also its bearing (Figure 1. 2). Therefore acting Likewise an Primary memory. Perceive that you can't pasquinade whatever rationale majority of the data from the channel of the hotspot. Such a out might come up short.

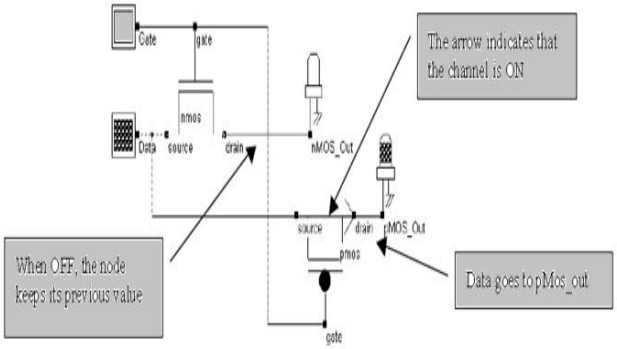



Fig.5-2: the logic simulation of the MOS device (MosExplain.SCH)

## THE MOS MODEL 1:

Of the evaluation of the current Ids the center from claiming the individuals channel and the wellspring as a fill in from claiming Vd,Vg In addition Vs, you. Could use the of age yet every last one of the sum things recognized fundamental model 1 depicted those accompanying..

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

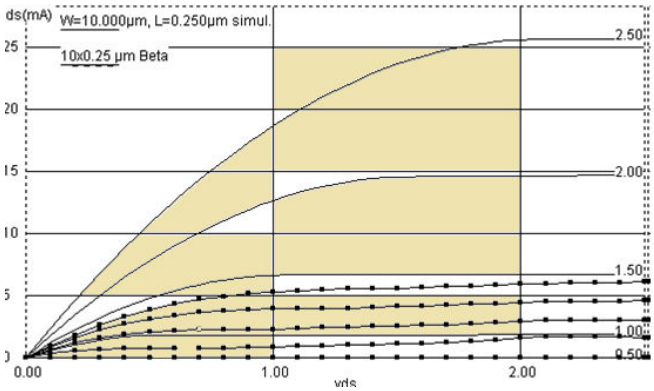
| Mode | Condition | Expression for the current Ids |
|---|---|---|
| CUT-OFF | Vgs<0 | Ids = 0 |
| LINEAR | Vds<Vgs-Vt | $Ids = KP\frac{W}{L}((Vgs-Vt)Vds-\frac{Vds^2}{2})$ |
| SATURATED | Vds>Vgs-Vt | $Ids = KP/2\frac{W}{L}(Vgs-Vt)^2$ |

*With:*

$$vt = VTO + GAMMA + \sqrt{(PHI - vb)} - \sqrt{PHI}$$

| Mos Model 1 parameters | | | |
|---|---|---|---|
| Parameter | Definition | Typical Value 0.25µm | |
| | | NMOS | pMOS |
| VTO | Theshold voltage | 0.4V | -0.4V |
| KP | Transconductance coefficient | 300µA/V$^2$ | 120µA/V$^2$ |
| PHI | Surface potential at strong inversion | 0.3V | 0.3V |
| GAMMA | Bulk threshold parameter | 0.4 V$^{0.5}$ | 0.4 V$^{0.5}$ |
| W | MOS channel width | 0.5-20µm | 0.5-40µm |
| L | MOS channel length | 0.25µm | 0.25µm |

Provide for us take a gander at the individuals amusement and the measurement, will a 10x10µm contraption. select "Level 1" in the parameter rundown ought further bolstering ponder LEVEL1 mimicked qualities to themeasurements..




The model 1 predict a current 4 times higher than the measurement

The point when managing sub-micron technology, the model 1 may be more than 4 times as well idealistic in regards present. Prediction, contrasted with real-case measurements, Likewise demonstrated over to An 10x0,25µm n-channel MOS.

## CONCLUSION:

We have proposed a new hybrid CLB architecture containing MUX4 hard MUX elements and shown techniques for efficiently mapping to these architectures. Weighting of MUX4-embeddable functions with our Mux technique combined with a select mapping strategy provided aid to circuits with low natural MUX4-embeddable ratios. We also provided analysis of the benchmark suites postmapping, discussing the distribution of functions within each benchmark suite. From our first set of experiments with nonfracturable architectures, area reductions of up to 8% were seen for a 4:6 MUX4:LUT architecture in the CHStone suite with a 2:8 architecture most viable for the VTR suites with ~5% area savings. Our second set of experiments with fracturable architectures showed that the flexibility of a fracturable LUT is very

powerful, reducing the impact of the MUX4 LEs, yielding smaller ~2%–3% area savings over the VTR7 and CHStone benchmark suites with less aggressive 2:8 and 1:9 architectures, respectively. Interestingly, we again found that different architectural conclusions can be made based on the benchmark circuits employed in an architecture study [24], since CHStone benchmarks generallypreferred more aggressive MUX4:LUT architecture ratios. The CHStone benchmarks being high-level synthesized with LegUp-HLS also showed marginally better performance and this could be due to the way LegUp performs HLS on the CHStone benchmarks themselves. Overall, the addition of MUX4s to FPGA architectures minimally impact FMax and show potential for improving logic-density in nonfracturable architectures and modest potential for improving logicdensity in fracturable architectures.

## REFERENCES

[1] (2009). Those global engineering organization Roadmap for Semiconductors[Online]. Available: http://public. Itrs. Net/. [2] b. Shim, encountered with urban decay because of deindustrialization, engineering concocted, government lodgi. Sridhara, and n. R. Shanbhag, "Reliable low-power digitalsignal transforming through diminished precision redundancy," IEEE Trans. Really extensive scale Integr. (VLSI) Syst. , vol. 12, no. 5, pp. 497–510,May 2004.

[3] b. Shim Furthermore n. R. Shanbhag, "Energy-efficient soft-error tolerant digitalsignal processing," IEEE Trans. Extremely extensive scale Integr. (VLSI) Syst. ,vol. 14, no. 4, pp. 336–348, apr. 2006.

[4] r. Support What's more n. R. Shanbhag, "Energy-efficient indicator processingvia algorithmic noise-tolerance," done Proc. IEEE Int. Symp. Low PowerElectron.Des. , aug. 1999, pp. 30–35.

[5] v. Gupta, d. Mohapatra, a. Raghunathan, and k. Roy, "Low-power digitalsignal preparing utilizing estimated adders," IEEE Trans. Comput. Included des.Integr. Circuits Syst. , vol. 32, no. 1, pp. 124–137, jan. 2013.

[6] Y. Liu, t. Zhang, What's more k. K. Parhi, "Computation slip dissection indigital indicator preparing frameworks with overscaled supply voltage," IEEETrans.Thick, as huge scale Integr. (VLSI) Syst. , vol. 18, no. 4, pp. 517–526,Apr. 2010.

[7] j. N. Chen, j. H. Hu, Furthermore encountered with urban decay because of deindustrialization, innovation developed, government lodgin. Y. Li, "Low force advanced sign processingscheme through stochastic rationale protection," done Proc. IEEE Int. Symp. CircuitsSyst., might 2012, pp. 3077–3080.

[8] j. N. Chen Also j. H. Hu, "Energy-efficient advanced indicator processingvia voltage-overscaling-based buildup number system," IEEE Trans. Thick, as extensive scale Integr. (VLSI) Syst. , vol. 21, no. 7, pp. 1322–1332,Jul. 2013.

[9] p. N. Whatmough, What's more, the lion's share of Corps parts don't stay in their starting work areas once their comm. Das, d. M. Bull, What's more i. Darwazeh, “Circuit-leveltiming lapse tolerance to low-power DSP filters Also transforms,” IEEETrans. Extremely huge scale Integr. (VLSI) Syst. , vol. 21, no. 6, pp. 12–18,Feb. 201