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Title: **PERFORMANCE EVALUATION OF PHOTO VOLTAIC CELL FED THREE-PHASE SWITCHED CAPACITOR MULTI LEVEL INVERTER USING MULTIPLE DC-LINKS**

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PERFORMANCE EVALUATION OF PHOTO VOLTAIC CELL FED THREE-PHASE SWITCHED CAPACITOR MULTI LEVEL INVERTER USING MULTIPLE DC-LINKS

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Abstract: This workuses multilevel inverter by using switching capacitor for PV grid. Now a day'smultilevel inverters have become more popular over the years in electric high power application with the promise ofless disturbances and the possibility to function at lower switching frequencies than ordinary two-level inverters. Soby cascading multilevel inverter the output voltage will be increases. By using multilevel inverter the cost will beless. It will be required less space. Modulation strategies, component comparison and solutions to the multilevelvoltage source balancing problem will also be presented in this work. By using the multilevel inverter we can reducethe total harmonic distraction compare to the other sources in PV grid for DC to AC converter. Switched-capacitor multilevel inverters (SCMLIs) are knownas another alternative which do not need the charge balancingoperations for eliminating the extra dc power supplies and asa result reducing the overall cost. Multilevel inverters find its wide applications in medium andhigh power industries for producing the staircase outputvoltage with less amount of distortion. The significance ofusing the multilevel inverters is to produce improved qualityof the output voltage with the reduced ratings of powersemiconductor switches; the commutation of the switches provides the additionof the capacitor voltages, thus reaching high voltage atthe output, while the power devices must withstand only reduced voltages. These multilevel inverters (MLI)have become an effective solution for increasing powerand reducing harmonic.

Index Terms—Boosted voltage, multilevel inverter, multiple dclinks, switched-capacitor converter.

(1). INTRODUCTION

Renewable Energy is characterized as vitality that is gathered from assets which are actually recharged ona human timescale, for example, daylight, wind, downpour, tides, waves, and geothermal warmth.Photovoltaic (PV) power structure is involving a critical part in the progression of appropriated electricforce frameworks a Micro lattices. So as to accomplish minimal effort and smallness, and also expandeddependability and proficiency, the idea of the transformer less PV network

associated inverter was proposed.The possibility of new Multi Level Inverter (MLI) is to utilize the accessible dc voltage sources to producea different yield voltage level discussed. In this paper another decreased switch topology form ofMLI by supplanting dc sources with split capacitors is proposed. The arrangement capacitors are associatedwith a solitary dc source. It performs taking into account a Time Frame Switching Scheme (TFSS) that willattempt to copy the predefined parameter of a reference sine wave (i.e., adequacy and recurrence) or thenetwork voltage (Vg) .The possibility of Multi Level Inverter (MLI) is to utilize the accessible dc voltagesources to create a various yield voltage level discussed. Subsequently enhances symphonious twistingelement by diminishing the lower request sounds. In this paper another decreased switch topology variantof MLI by supplanting dc sources with split capacitors is proposed. The arrangement capacitors are associatedwith a solitary dc source. It performs in view of a Time Frame Switching Scheme (TFSS) that will attemptto mirror the predefined parameter of a reference sine wave (i.e., adequacy and recurrence) or the frameworkvoltage (Vg).The proposed topology receives decreased number of semiconductor exchanging gadgets andsymphonious element is enhanced when contrasted and the traditional strategies discussed. Thereproduction results are confirmed by equipment execution utilizing a dsPIC30F4011 controller. A solitarystage seven-level inverter for matrix associated photovoltaic frameworks, with a novel heartbeat width adjusted (PWM) control plan presented. In another multilevel converter topology that has numerousprogressions with less power electronic switches. The circuit comprises of arrangement associated submultilevel converters squares. The ideal structures of this topology are examined for different destinations,for example, least number of switches and capacitors, and least standing voltage on switches for delivering most extreme yield voltage steps. Another calculation for determination of dc voltage source extents has likewise been introduced in [6]. In [7] expressed a novel multilevel inverter with a little number of exchanging gadgets. It comprises of a H-span and an inverter which yields multilevel voltage by exchanging the dc voltage sources in arrangement and in parallel. In [8] &[9] expressed a control strategy connected to a three-stage shunt dynamic channel taking into account a NPC inverter, demonstrating the displaying method expected to complete the proposed control. The inverter advancements for interfacing photovoltaic (PV) modules to a solitary stage framework examined in [10]. In [11] expressed that another unbiased pointclipped heartbeat width regulation (PWM) inverter made out of primary exchanging gadgets which workas switches for PWM and helper changing gadgets to cinch the yield terminal potential to the impartialpoint potential has been produced. In [12] & [13] expressed that the multilevel inverter innovation has developed as of late as a critical option in the range of high power medium-voltage vitality control. This paper exhibits the most

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imperative topologies like diode-braced inverter (nonpartisan point cinched), capacitor-clipped (flying capacitor), and multi cell with isolated DC sources. Developing topologies like awry half and half cells and delicate exchanged multilevel inverters are additionally talked about.

2 PROPOSED SCC

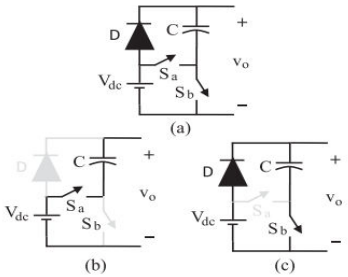

Fig. 1. (a) Presented basic series–parallel unit in [33]. (b) Capacitor discharging mode (c) Capacitor charging mode.

Fig. 1(a) shows the basic circuit of the proposed SCC. This proposed circuit is called basic unit [33] which contains one dc power supply, one capacitor, one passive power diode, and two active power switches which have complementary operation with each other. PV cells, batteries and fuel cells can be used as power supply in this structure. Fig. 1(b) and (c) shows the charging and discharging operations for capacitor C. Switches Sa and Sb are used in series and parallel conversion operation, respectively. As it can be seen, when the switch Sb turns ON, the capacitor C is charged to Vdc and when the switch Sa turns ON, the diode becomes reverse biased and capacitor is discharged. In this mode, the energy stored in power supply and capacitor C is transferred to the output. It is obvious that the proposed basic unit does not require any extra charge balancing control circuits which is the major advantage of this structure.

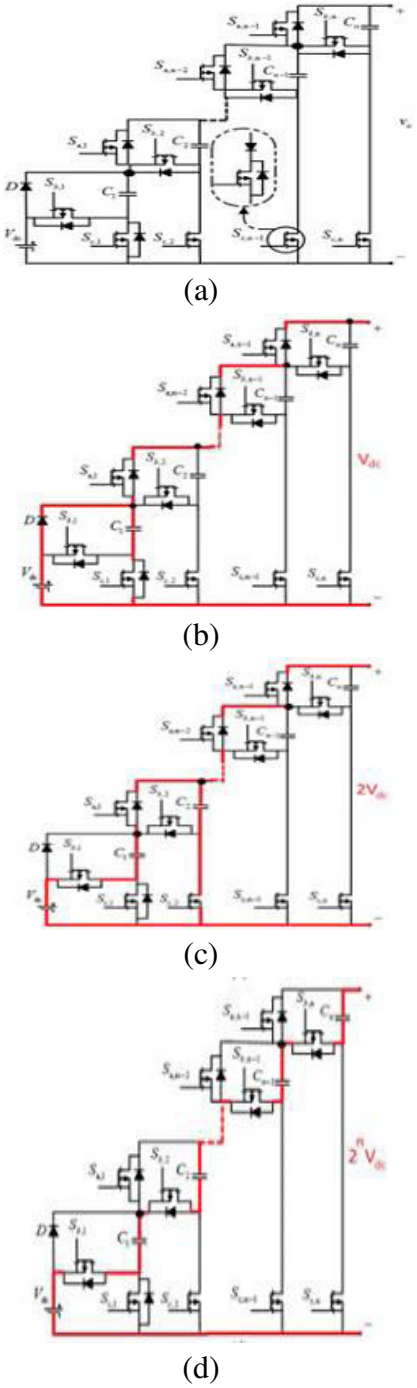

Fig.2. (a) Proposed switched-capacitor dc/dc converter (SCC). (b) Current flow path of first output voltage level. (c) Current flow path of second output voltage level. (d) Current flow path of 2^n output voltage level

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Table I

ON Switching States of Proposed SCC

ON switches	Output voltage	Capacitor states				
		C_1	C_2	C_3	...	C_n
$S_{a,1}, S_{a,2}, \ldots, S_{a,n-1}, S_{c,1}$	V_{dc}	C	NE	NE	...	NE
$S_{a,1}, S_{a,2}, \ldots, S_{a,n-1}, S_{b,1}, S_{c,2}$	$2V_{dc}$	D	C	NE	...	NE
$S_{a,2}, S_{a,3}, \ldots, S_{a,n-1}, S_{b,2}, S_{c,1}$	$3V_{dc}$	C	D	NE	...	NE
$S_{a,2}, S_{a,3}, \ldots, S_{a,n-1}, S_{b,1}, S_{b,2}, S_{c,2}$	$4V_{dc}$	D	D	C	...	NE
$S_{a,1}, S_{a,3}, S_{a,4}, \ldots, S_{a,n-1}, S_{b,3}, S_{c,1}$	$5V_{dc}$	C	NE	D	...	NE
$S_{a,1}, S_{a,3}, S_{a,4}, \ldots, S_{a,n-1}, S_{b,1}, S_{b,3}, S_{c,1}$	$6V_{dc}$	D	C	D	...	NE
...	...	...	...	...	...	...
$S_{b,1}, S_{b,2}, \ldots, S_{b,n}$	$2^n V_{dc}$	D	D	D	...	D

NE: No Enter

Fig. 2(a) shows circuit configuration of the proposed switched capacitor dc/dc converter and also Fig. 2(b) to (d) illustrates the current flow path of first, second and 2^nth voltage level for proposed SCC, respectively. This topology is yielded from series combination of several basic units of Fig. 1. In order to charge all the capacitors and generate output voltage waveform, switches Sai(i =1,2,...,n−1), Sbi, and Sci(i =1,2,...,n) are driven by series–parallel conversion or combination of them. It should be noted that, switches of Sci (i =2, 3... n) are unidirectional power switches without anti-parallel diode and other switches are also unidirectional with internal anti-parallel diode which can pass the reverse current for inductive loads. Table I indicates the different ON switching and capacitor states of proposed SCC. In this Table, C and D refer to charging and discharging modes for capacitors, respectively. In order to generate more output voltage levels with optimum number of components, all of the capacitors should be charged by Binary asymmetrical algorithm, according to this Table. For example, in state (1) when switchSc,1 turns ON, capacitor C_1 is charged to Vdc and this voltage level is transferred to the output through Sa,i(i=1,2, ..n−1). Also in state (2), C_2 is charged toVdc+Vc1through switchSc,2 and with discharging of C_1, second voltage level generates at the output through Sa,iandSb,1, simultaneously which is equaled to $2V_{dc}$. After this moment, without entering other capacitors, voltage level of $3V_{dc}$ can be transferred to the output by stored voltage of C_2 and constant dc voltage source. In this moment, C_1 is again charged by dc voltage source directly and for next voltage level, this stored voltage beside the voltage of C_2 and constant dc voltage source are transferred to the output which is equaled to 4Vdc and this consecutive operations continues on. The prominent feature of the proposed circuit is that by entering the next capacitors to the circuit and also continuing the series–parallel switching strategy, the number of output voltage levels is enhanced as binary manner from Vdc to 2^n Vdc. It is important to note that, always at each voltage step, the related capacitor of previous steps must be connected in parallel to keep on the charging operation. Therefore, if we assume the number of capacitors equal ton, the stored voltage of each capacitor is equal to

$$V_{C,k} = 2^{k-1} V_{dc} \qquad for \quad k = 1,2,\ldots,n \tag{1}$$

Also from this Table it is obvious that, proposed SCC is able to generate different number of positive output voltage levels by self-balancing ability. Now with considering the proposed overall structure [see Fig. 2(a)], the number of required power switches or isolated gate bipolar transistor (IGBT) (NIGBT, u) or gate drivers

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(NDriver, u), power diodes (Ndiode, u), and output voltage levels(N-level, u)are calculated by the following equations, respectively

$$N_{\mathrm{IGBT},u} = N_{\mathrm{Driver},u} = 3n - 1 \quad (2)$$

$$N_{\mathrm{diode},u} = n \quad (3)$$

$$N_{\mathrm{level},u} = 2^n \quad (4)$$

According to (4), the proposed circuit has a very good boost capability without using the transformer. This feature reduces the size and cost of the system and in ceases the efficiency. The factor can be defined as

$$\beta = \frac{V_{o,\max,u}}{\sum \mathrm{V_{dc}}} = 2^n \quad (5)$$

Moreover, this structure is able to mitigate the total blocked voltage. The low blocked voltage will lead in reduced conduction losses, efficiency, and cost. In this case, total value of blocked voltage is formulized as

$$V_{\mathrm{block},u} = [3(2^n - 1) - 1]\,V_{\mathrm{dc}} \quad (6)$$

3.3 PROPOSED SCMLI

In order to convert the output polarity of SCC and create output voltage levels (even and odd), a full H-bridge cell can be added to the proposed SCC block similar to other existing structures, however using the full H-bridge cell may increase the number of required semiconductor devices and current path components. In the presented circuit of Fig. 3, instead of using full H-bridge unit a novel structure has been proposed in order to create the maximum number of output voltage ,levels with fewer number of switches in compared to which is quite different with FCMCs topologies. In the proposed basic SCMLI topology indicated by Fig. 3, pair stage of SCC units and six unidirectional power switches are required to change the polarity of the output voltage.

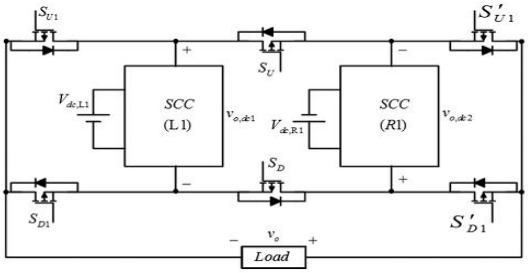

Fig.3. Proposed SCMLI topology

The switching pattern of proposed SCMLI is summarized in Table II by seven different switching states. From this Table and proposed SCMLI topology, it is clear that to avoid the short-circuit problem, switches SU and SD should not to be turned ON simultaneously even though they are in current path in positive and negative half cycles of output voltage, respectively. Also note that, switches SU1, SD1 and S'U1, S'D1 have complementary operation with each other.Therefore, number of required IGBTs and also required power diodes for basic structure of proposed SCMLI can be expressed as following equations, respectively:

$$N_{\mathrm{IGBT}} = 6n + 4 \quad (7)$$

$$N_{\mathrm{Diode}} = 2n \quad (8)$$

On the other hand, because of using two similar SCC units in the proposed SCMLI, two isolated dc voltage sources and 2^n capacitors are needed. The two utilized dc voltage sources can be symmetric (equal) or asymmetric (asymmetric). However, to achieve the maximum number of voltage levels at the output, the second isolated dc power supply should be adopted by

$$\mathrm{V_{dc,R1}} = (1 + 2^n)\,\mathrm{V_{dc,L1}} \quad (9)$$

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Therefore, maximum number of output voltage levels in asymmetric form is equal to

$$N_{\text{level}} = 1 + 2^{n+2} + 2^{2n+1} \quad (10)$$

In order to avoid some constraints in proposed SCMLI concerned with existing spikes across the capacitors in each of SCC units, especially in high power ratio and also to suggest a practical structure with minimum number of switches, the boost factor (β) for each of SCC units is chosen to be two. Therefore with respect t_{on}=1, proposed basic SCMLI can generate 17 voltage levels at the output condition, respectively. So the proposed topology requires two isolated dc voltage sources, two capacitor, ten power switches, and two power diodes. According to (9) and with considering n=1, in order to generate all of the voltage levels at the output based on asymmetric form, the magnitude of dc voltage sources for SCCL,1 and SCCR,1 should be set on Vdc and 3Vdc, respectively.

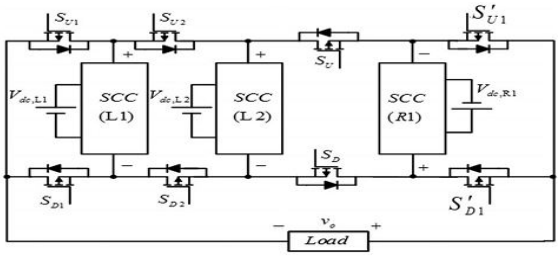

Fig.4. Proposed 49-level SCMLI

So the output voltage of SCC units can be selected as Vdc and 3Vdc (by parallel switching mode) and 2Vdc and 6Vdc (by series switching mode) as mentioned in the previous section. In order to extend the number of output voltage levels in proposed SCMLI and also define a general structure based on n=1, the third SCC unit (SCCL,2) is inserted into the proposed basic SCMLI topology as shown in Fig. 4. So to achieve the maximum number of output voltage levels, the magnitude of third dc voltage source can be calculated by (11).Thus, with proper series–parallel switching in third SCC unit, 9Vdc and 18 Vdc can be generated at the output of it

$$V_{\underset{L,2}{\text{dc,scc}}} = 2\left(V_{\underset{L,1}{\text{dc,scc}}} + V_{\underset{R,1}{\text{dc,scc}}}\right) + 1 \quad (11)$$

Therefore, 49-level voltage (24 positive levels, 24 negative levels, and one zero level) is generated at the output with 14 power switches and 3 isolated dc voltage sources. Table III indicates, the ON switching states beside the number of positive desired output voltage levels for proposed 49-level SCMLI in positive half cycles. In this Table, the internal switching states of each SCC block have not been considered.

Table II
Different Switching States for Basic Structure of Proposed SCMLI

		ON Switches	v_o
Switching States	1	S_{D1}, S_U, S'_{D1}	$v_{o,\text{dc1}} + v_{o,\text{dc2}}$
	2	S_{U1}, S_U, S'_{D1}	$v_{o,\text{dc2}}$
	3	S_{D1}, S_U, S'_{U1}	$v_{o,\text{dc1}}$
	4	S_{U1}, S_U, S'_{U1}	0
		S_{D1}, S_D, S'_{D1}	
	5	S_{U1}, S_D, S'_{D1}	$-v_{o,\text{dc1}}$
	6	S_{D1}, S_D, S'_{U1}	$-v_{o,\text{dc2}}$
	7	S_{U1}, S_D, S'_{U1}	$-v_{o,\text{dc1}} - v_{o,\text{dc2}}$

According to this Table, for instant, to generate 24th level of output voltage in positive half cycle, the switches (SD1, SD2, SU, S'D1) beside the internal series active

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switches ofSCCL,2 and SCCR,1 and also internal parallel active switch of SCCL,1 must be ON. Also an another example, in order to generate 23rd level of output voltage, according to Table III, switches of (SU1, SD2, SU, S'D1) besides internal series switches of SCCR,1 and SCCL,2 and also internal parallel switch of SCCL,1 must be ON. It is clear that, in order to generate negative half cycle of output voltage levels, in each output voltage level, the switches that were in OFF state must be in ON state.

Table III
List Of On Switching States for the Proposed 49-Level Inverter in Positive Half Cycle

States	ON Switches	Number of desired Output Voltage Levels
1	$S_{D1}, S_{U2}, S_U, S'_{U1}$	1,2
2	$S_{U1}, S_{U2}, S_U, S'_{D1}$	3,6
3	$S_{D1}, S_{U2}, S_U, S'_{D1}$	4,5,7,8
4	$S_{D1}, S_{D2}, S_U, S'_{U1}$	9,18
5	$S_{U1}, S_{D2}, S_U, S'_{D1}$	10,11,13,14,19,20,22,23
6	$S_{D1}, S_{D2}, S_U, S'_{D1}$	12,15,21,24
7	$S_{U1}, S_{D2}, S_U, S'_{U1}$	16,17

Table, for instant, to generate 24th level of output voltage in positive half cycle, the switches (SD1, SD2, SU, S'D1) beside the internal series active switches of SCCL,2 and SCCR,1 and also Internal parallel active switch of SCCL,1 must be ON. Also an another example, in order to generate 23rd level of output voltage, according to Table III, switches of (SU1, SD2, SU, S'D1) besides internal series switches of SCCR,1 and SCCL,2 and also internal parallel switch of SCCL,1 must be ON. It is clear that, in order to generate negative half cycle of output voltage levels, in each output voltage level, the switches that were in OFF state must be in ON state.

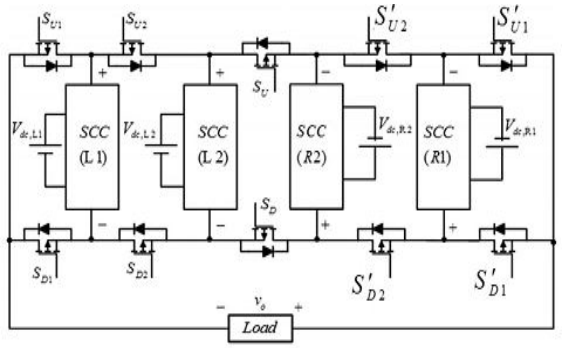

Fig.5. Proposed 137-level SCMLI topology

With similar manner, by entering the fourth SCC unit (SCCR, 2) to the proposed 49-level structure, 137-level SCMLI can be generated by regarding Fig. 5 which requires only 18 power switches and 4 isolated dc power supplies. In this case, to generate all of the voltage levels at the output (68 positive levels, 68 negative levels, and one zero level), the magnitude of fourth added dc voltage source can be calculated as follows:

$$V_{\underset{R,2}{\text{dc,scc}}} = 2\left(V_{\underset{L,2}{\text{dc,scc}}} + V_{\underset{R,1}{\text{dc,scc}}}\right) + 1 \quad (12)$$

Regarding n=1 and (9), (11), and (12), the output voltage of fourth added SCC unit can be selected as 25 Vdc and 50 Vdc by parallel and series switching operations, respectively. Similarly, by inserting the m number of proposed SCC units (with n=1) into the proposed 137-level structure, a general topology is made according to Fig. 6. It is clear from figure that, m proposed SCC units have been drawn with each other from left and right sides by added upper and lower unidirectional power switches (SUm, SDm and S'Um, S'Dm).

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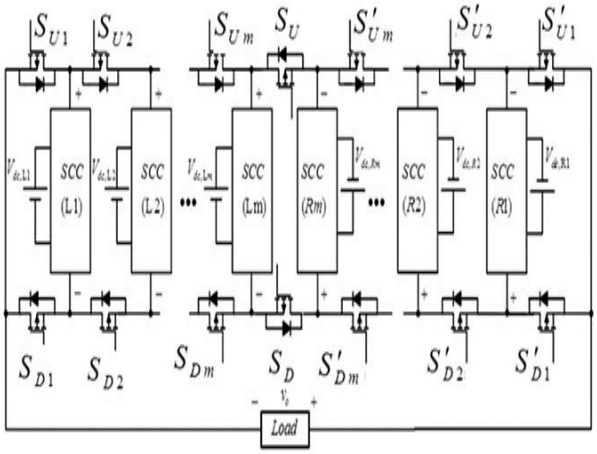

Fig.6. Proposed general topology of SCMLI

To generate maximum number of output voltage levels with respect to all of the steps, the magnitude of added dc voltage sources for each SCC unit should be adopted by the following iterative equations:

$$V_{L,i}^{dc,scc} = 2(V_{L,(i-1)}^{dc,scc} + V_{R,(i-1)}^{dc,scc}) + 1 \; i = 1,2,\ldots m \quad (13)$$

$$V_{R,i}^{dc,scc} = 2(V_{L,i}^{dc,scc} + V_{R,(i-1)}^{dc,scc}) + 1 \; i = 1,2,\ldots m \quad (14)$$

Based on Fig. 6, the number of required IGBTs, capacitors, power diodes, and also maximum number of current path components are obtained by the following equations, respectively:

$$N_{IGBT} = 8m + 2 \quad (15)$$

$$N_{Capacitors} = N_{Diode} = 2m \quad (16)$$

$$N_{current\ path} = 4m + 1 \quad (17)$$

Where m is assumed to be half of isolated dc power supply numbers. Therefore, the number of output voltage levels, maximum value of output voltage, and also total value of blocked voltage are summarized by the following equations, respectively:

$$N_{level} = 2(V_{L,m}^{dc,scc} + V_{R,m}^{dc,scc}) + 1 \quad (18)$$

$$V_{O,\max} = 2(V_{L,m}^{dc,scc} + V_{R,m}^{dc,scc}) = 4 + 6V_{L,m-1}^{dc,scc} + 8V_{R,m-1}^{dc,scc} \quad (19)$$

$$V_{blocked,T} = V_{blocked,S_U} + V_{blocked,S_D} + 2\sum_{i=1}^{m}(V_{S_{U,i}}^{blocked} + V_{S_{D,i}}^{blocked} + V_{S_{scc,i}}^{block})\, i = 1,2,\ldots m$$

$$V_{blocked,T} = 10(V_{L,m}^{dc,scc} + V_{R,m}^{dc,scc}) \quad (20)$$

3.4 DETERMINATION OF CAPACITANCE

In this section, the capacitance of two utilized capacitors for proposed basic SCMLI based on asymmetric condition is calculated. For this reason, details of circuit diagram for proposed 17-level inverter is shown by Fig. 7. Also, Table IV indicates the switching and capacitor states of this structure. From this table, it can be taken that to generate each of voltage steps at the output, only five switches are involved in current path which is counted as a great advantage of proposed circuit. Because, the number of current path components is proportional to the total voltage drop and can impose on overall efficiency. In addition, it should be pointed out that the switching pattern can be chosen based on fundamental switching frequency because of lower creating switching loss and simplicity. In this modulation technique, the sinusoidal reference voltages are compared with some of available dc voltage levels and create the related gate switching pulses. Details of modulation strategy are not objective of this paper. To determine the capacitance ofC1andC2, two assumptions are considered in which one is related to output sinusoidal

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load current with phase difference between output voltage and current (ϕ) and the other is concerned to same duration in each step of staircase output voltage.

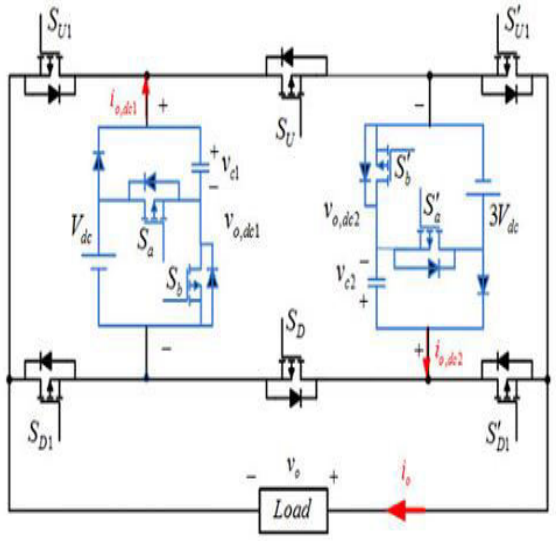

Fig.7. Proposed 17-level inverter structure

Thus, the maximum discharging amount for each of capacitors can be defined as (21) in one half cycles

$$Q_{Ci} = \int_{t_j}^{\frac{T}{4}-t_j} I_{out} \sin(2\pi f_S t - \varphi) dt = 1,2 \quad (21)$$

Where T, fS, and Iout are period of one cycle, frequency of output voltage, and amplitude of load current, respectively, and also [tj, T4 –tj] is time interval corresponded to the longest discharging cycle (LDC) of each capacitor. By regarding the cut of the sinusoidal reference voltage to the some available dc voltage levels the amounts of tj can be derived by following equation

$$t_j = \frac{1}{2\pi f_{ref}} \sin^{-1}\left(\frac{2j-1}{16}\right) \quad j = 1,2,\ldots,8 \quad (22)$$

$$C_{opt,i} \geq \frac{Q_{Ci}}{kV_{in}} \quad (i = 1,2) \quad (23)$$

Table IV

Different switching and capacitors states for proposed basic 17-level inverter

		ON Switches	v_o	C_1	C_2
Switching States	1	$S_{D1}, S_a, S_U, S'_a, S'_{D1}$	$4V_{dc} + v_{c,1} + v_{c,2}$	D	D
	2	$S_{D1}, S_b, S_U, S'_a, S'_{D1}$	$4V_{dc} + v_{c,2}$	C	D
	3	$S_{U1}, S_b, S_U, S'_a, S'_{D1}$	$3V_{dc} + v_{c,2}$	C	D
	4	$S_{D1}, S_a, S_U, S'_b, S'_{D1}$	$4V_{dc} + v_{c,1}$	D	C
	5	$S_{D1}, S_b, S_U, S'_b, S'_{D1}$	$4V_{dc}$	C	C
	6	$S_{U1}, S_b, S_U, S'_b, S'_{D1}$	$3V_{dc}$	C	C
	7	$S_{D1}, S_a, S_U, S'_b, S'_{U1}$	$V_{dc} + v_{c,1}$	D	C
	8	$S_{D1}, S_b, S_U, S'_b, S'_{U1}$	V_{dc}	C	C
	9	$S_{D1}, S_b, S_D, S'_b, S'_{D1}$ $S_{U1}, S_b, S_U, S'_b, S'_{U1}$	0	C	C
	10	$S_{U1}, S_b, S_D, S'_b, S'_{D1}$	$-V_{dc}$	C	C
	11	$S_{U1}, S_a, S_D, S'_b, S'_{D1}$	$-V_{dc} - v_{c,1}$	D	C
	12	$S_{D1}, S_b, S_D, S'_b, S'_{U1}$	$-3V_{dc}$	C	C
	13	$S_{U1}, S_b, S_D, S'_b, S'_{U1}$	$-4V_{dc}$	C	C
	14	$S_{U1}, S_a, S_D, S'_b, S'_{U1}$	$-4V_{dc} - v_{c,1}$	D	C
	15	$S_{D1}, S_b, S_D, S'_a, S'_{U1}$	$-3V_{dc} - v_{c,2}$	C	D
	16	$S_{U1}, S_b, S_D, S'_a, S'_{U1}$	$-4V_{dc} - v_{c,2}$	C	D
	17	$S_{U1}, S_a, S_D, S'_a, S'_{U1}$	$-4V_{dc} - v_{c,1} - v_{c,2}$	D	D

It is worth noting that, according to (23), two utilized capacitors of the proposed topology can have different capacitances, and however choosing unequal capacitances will lead to different value of voltage ripple across the capacitors. In fact, it is preferred to select same capacitors with respect to (23) instead of using two different capacitors.

5 POWER LOSS ANALYSIS FOR PROPOSED 17-LEVEL INVERTER

For this kind of converters, always three major types of associated losses should be considered which include: switching losses Psw, conduction losses of semiconductor devices P_{Con}, and ripple losses of two utilized capacitors P_{Rip}. All of the calculations are done based on fundamental switching frequency strategy.

A. Switching Losses

Switching loss occurs during the ON and OFF period of switching states. For simplicity, a linear approximation between voltage and current of switches in the switching period is considered. Based on this assumption, the following equations can be expressed for i^{th}switch:

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$$P_{\mathrm{sw,on},i} = f\int_0^{t_{\mathrm{on}}} v_{\mathrm{sw},i}(t)i(t)dt$$
$$= f\int_0^{t_{\mathrm{on}}} \left(\frac{V_{\mathrm{sw},i}}{t_{\mathrm{on}}}t\right)\left(-\frac{I_i}{t_{\mathrm{on}}}(t-t_{\mathrm{on}})\right)dt$$
$$= \frac{1}{6}f\,V_{\mathrm{sw},i}I_i t_{\mathrm{on}} \quad (24)$$
$$P_{\mathrm{sw,off},i} = f\int_0^{t_{\mathrm{off}}} v_{\mathrm{sw},i}(t)i(t)dt$$
$$= f\int_0^{t_{\mathrm{off}}} \left(\frac{V_{\mathrm{sw},i}}{t_{\mathrm{off}}}t\right)\left(-\frac{I'_i}{t_{\mathrm{off}}}(t-t\right.$$
$$= \frac{1}{6}f\,V_{\mathrm{sw},i}I'_i t_{\mathrm{off}} \quad (25)$$

Where I_i and I'_I are the currents through i^{th} power switch after turning ON and before turning OFF, respectively, f is switching frequency which is equaled to reference frequency and Vsw,i is the OFF-state voltage of i^{th} power switch. In order to calculate the total switching loss, the number of ON Non and the number of OFF Noff switching states per one cycle should be multiplied by (24) and (25) as follows:

$$P_{\mathrm{sw}} = \sum_{i=1}^{10}\left(\sum_{k=1}^{N_{\mathrm{on}}} P_{\mathrm{sw,on},ik} + \sum_{k=1}^{N_{\mathrm{off}}} P_{\mathrm{sw,off},ik}\right) \quad (26)$$

B. Conduction Losses

In order to calculate the total conduction losses of each component, a straightforward method based on pure-resistance load is presented. By regarding the Table IV, four possible operating modes can be investigated which are included as zero states, discharging states for both capacitors (states number of 1 and 17), charging states for both capacitors (states number of 5, 6, 8, 10, 12, and 13) and discharging states for one capacitor and charging states for another one or vice versa (other remaining states). Fig.8(a)–(c) demonstrates the equivalent circuits of charging and discharging operation modes for capacitors.

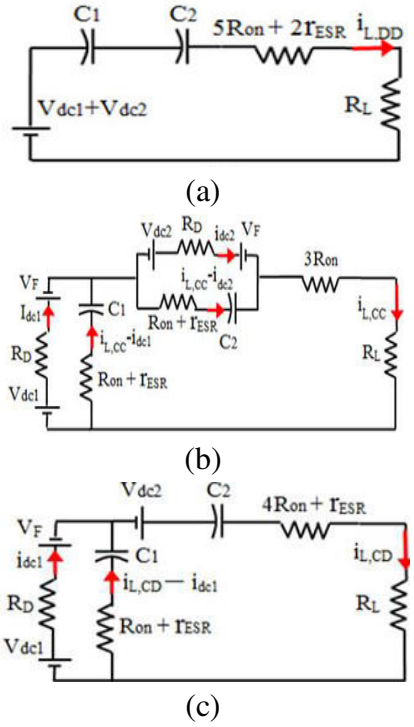

Fig.8. Equivalent circuit of proposed 17 level structures with a resistive load (a) In discharging modes (b) In charging modes (c) In combination of charging and discharging modes

In this figures, Ron... rESR, RL and VF are internal ON-state resistance of each switch, internal resistance of each diode, equivalent series resistance (ESR) of each capacitor, load resistance and forward voltage drop of each incurred diodes, respectively. According to Fig. 9(a), during the series connection of capacitors and the dc voltage sources, the value of load current can be written as

$$i_{L,DD} = \frac{4V_{\mathrm{dc}} + v_{c,1} + v_{c,2}}{5R_{\mathrm{on}} + 2r_{\mathrm{ESR}} + R_L} \quad (27)$$
$$p_{c,\mathrm{DD}} = (5R_{\mathrm{on}} + 2r_{\mathrm{ESR}})i^2_{L,\mathrm{DD}} \quad (28)$$
$$\overline{p_{c,\mathrm{DD}}} = \frac{2f}{\pi}\left(\frac{\pi}{2} - t_8\right)p_{c,\mathrm{DD}} \quad (29)$$

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$$p_{c,CC} = 3R_{on}i_{L,CC}^2 + R_D(i_{dc,1}^2 + i_{dc,2}^2) + (R_{on} + r_{ESR})\left[(i_{L,CC} - i_{dc,1})^2 + (i_{L,CC} - i_{dc,2})^2\right]$$

$$\overline{p_{c,CC}} = \frac{2f}{\pi}\left[(t_5 - t_3) + (t_2 - t_1)\right]p_{c,CC} \quad (31)$$

Where, idc,1 and idc,2 can be calculated by using the Kirchhoff voltage law according to following, equations, respectively:

$$i_{dc,1} = \frac{(r_{ESR} + R_{on})i_{L,CC} + V_{dc} - v_{c,1} - V_F}{R_D + r_{ESR} + R_{on}} \quad (32)$$

$$i_{dc,2} = \frac{(r_{ESR} + R_{on})i_{L,CC} + 3V_{dc} - v_{c,2} - V_F}{R_D + r_{ESR} + R_{on}} \quad (33)$$

$$P_{c,CD,i} = (4R_{on} + r_{ESR})i_{c,CD}^2 + R_D i_{dc,i}^2 + \text{for } i = 1,2 \quad (R_{on} + r_{ESR})(i_{c,CD} - i_{dc,i})^2 \quad (34)$$

$$\overline{p_{c,CD}} = \frac{2f}{\pi}\left[\left[(t_8 - t_6)\right]p_{c,CD,2} + \left[(t_6 - t_5) + (t_3 - t_2)\right]p_{c,CD,1}\right]. \quad (35)$$

Considering (29), (31), and (35), and the total conduction loss P_{Con} in one full cycle can be summarized by (36)

$$P_{Con} = \overline{p_{c,DD}} + \overline{p_{c,CC}} + \overline{p_{c,CD}} + 3R_{on}I_{rms,L}^2 \quad (36)$$

Where, $I_{rms,L}$ is the root mean square load current in the zero state.

C. Ripple Losses

When the capacitors are connected in parallel for charging operation, the ripple losses occur by the difference between the respected input voltage and the voltage of capacitors (vc, I (i= 1,2)). Therefore, the voltage ripple of capacitors Δ_{VCi} is taken by

$$\Delta V_{Ci} = \frac{1}{C_i}\int_{t'}^{t} i_{C_i}(t)dt \quad (37)$$

Where, i_{Ci} (t) is the current of capacitor and [t' −t] is the time interval for discharging modes which can be obtained by regarding to Table IV. Thus, the total value of ripple loss, for one full cycle of output waveform is equaled to (38)

$$P_{Rip} = \frac{f}{2}\sum_{i=1}^{2} C_i \Delta V_{Ci}^2 \quad (38)$$

From (37) and (38), it is clear that, P_{Rip} is inversely proportional to the capacitance C_i which means larger capacitance contributes to higher value of overall efficiency.

Considering (26), (36), and (38), the total losses of the proposed topology and overall efficiency can be calculated as (39) and (40), respectively

$$P_{Loss} = P_{Rip} + P_{Con} + P_{sw} \quad (39)$$

$$\eta = \frac{P_{out}}{P_{out} + P_{Loss}} \quad (40)$$

6. SIMULATION RESULTS

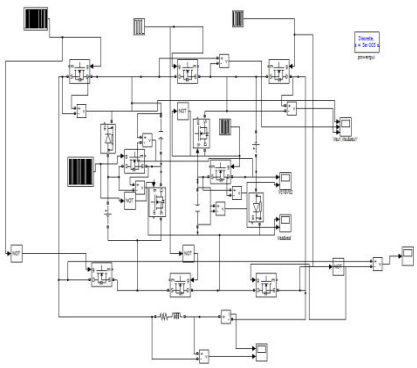

Fig 9 Single Phase Switched Capacitor of Simulation Diagram

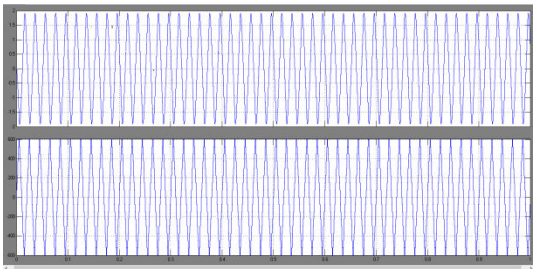

Fig 10 Simulation Output Voltage and No Load Condition

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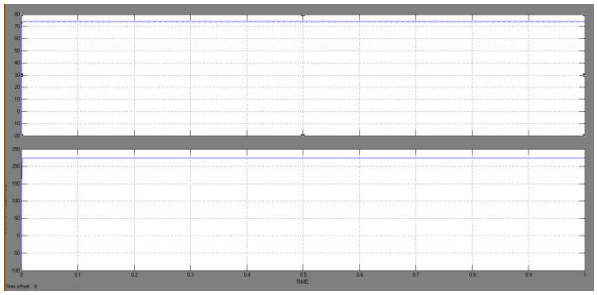

Fig 11 Simulation Wave Forms Under R-L Load Condition Across Voltage OF C1,C2

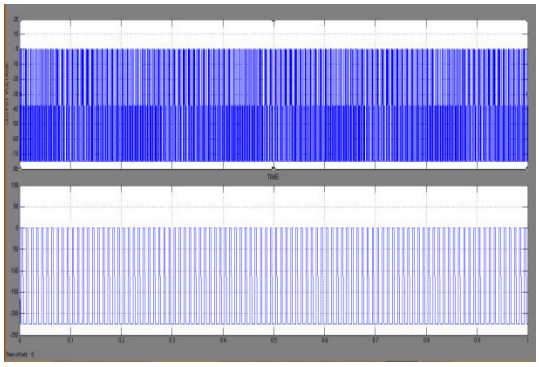

Fig 12 Blocking Wave Forms across Switches

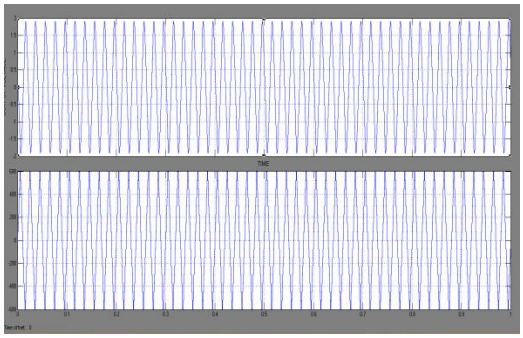

Fig 13 Output Wave Forms For Voltage And Current

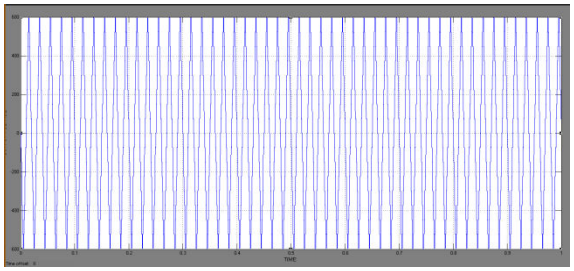

Fig 14 Output Wave Form for Voltage and Current

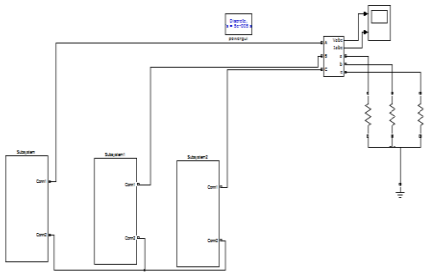

Fig 15 extension 3-phase inveter Simulation Diagram

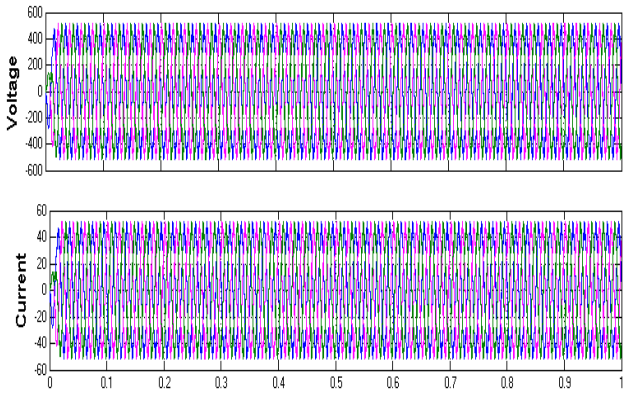

Fig 16 Three Phase Voltage and Current Output Wave Form

7. Conclusion

This study proposes a new SCC topology with minimum switches numbers. With optimum number of switches and isolated dc voltage sources, the input voltage has been boosted significantly. A new SCMLI topology uses the proposed SCC units as virtual dc link with only 10 active power switches, two isolated dc power supplies, and two capacitors with 17-level inverter has been presented. By adding only four and eight power switches to basic structure of proposed SCMLI and with one and two more SCC units, 49- and 137-level inverters will be obtained, respectively. Finally, the effectiveness and performance of proposed

17-level SCMLI topology have been verified by various simulation results. This study proposes a new SCC topology with minimum switches numbers. With optimum number of switches and isolated dc voltage sources, the input voltage has been boosted significantly. The pro-posed topology reduces the number of power switches, diodes, and the magnitude of total blocked voltage, size, and cost of the system in comparison with the conventional similar topologies

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