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Paper Authors

Dharmavaram Asha Devi, Muchukota Suresh Babu , Thirupari Sindhuja

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Design and Implementation of 64-bit Barrel Shifter with Reconfigurable SoC

Dharmavaram Asha Devi[1], Muchukota Suresh Babu[2], Thirupari Sindhuja[3]
[1,3] Sreenidhi Institute of Science and Technology,Ghatkesar, Yamnampet,Hyderabad, India- 501301
[2]Srikrishnadevaraya Engineering College, Gooty, Anantapur District, AP, India
ashadevi@sreenidhi.edu.in

Abstract— In majority of embedded system-based applications, RISC Processors are popular. In these processors, barrel shifters are used for performing arithmetic and logical operations like multiplication, division, shift and rotation operations. The reason behind this will be a great advantage of speed. Because, a barrel shifter can perform shift and rotate operations within a single clock cycle where as in a normal shifter 'n' number of clock cycles are required for n-shift or rotate operations. As per the today's need, in the design and development of 64-bit processors, 64-bit barrel shifters IPs are desired. Therefore, the RTL design of 64-bit barrel shifter, implementation and its verification process with an Artix 7 FPGA and front-end CAD tool is demonstrated in this paper. The main feature of the proposed work is power efficient design. It is implemented with 28nm technology and verified with 100MHz on board clock.

Keywords: Computer Aided Design, Field Programmable Gate Array, Reduced Instruction Set Computer, RTL Design, VIO block.

I. INTRODUCTION

The Barrel Shifter will perform different operations like arithmetic and logical shifts in left and right directions, rotational operations in left and right directions. The advantage of it is, it can shift and rotate a specified number of bits at an instant of time. Therefore, speed of operation is more when compared with conventional shifter [1]. It is mainly used in general purpose processors and digital signal processors. It also used in floating-point arithmetic units and multiplication operations by constant numbers. If we consider a RISC processor, it is mainly used as part of ALU (Arithmetic and Logical Unit). There are some designs for Barrel Shifters [2, 3, 4, 5] and their performance analysis has been done with certain extent. However, it's validation with VIO (Virtual Input / Output) verification has not been done for the correctness of the functionality. If there are a greater number of input and output ports, the verification process is a typical task for the designer. Hence, in the proposed design, it is clearly discussed about how to design and monitor the functionality with VIO concept.

The proposed design is a 64-bit Barrel Shifter implemented in mixer of behavioral and structural models using Verilog HDL (Hardware Description Language). The traditional front-end processing steps: RTL Design, Elaboration of the design along with design constraints creation, Synthesis analysis, Implementation analysis, Bit stream generation, programming FPGA and finally verification of the operations on target FPGA development board, Nexys 4 DDR. The proposed design can be used as an customized intellectual property for RICS based processor designs under 28nm technology.

II. LITERATURE SURVEY

In the earlier research, CMOS performance analysis was described on 4-bit barrel shifters. They have shown two design approaches, fully automatic and semicustom. They have stated that, the power improvement is 4.2 % and area improvement is 23 % in semi-custom design when compared to fully automatic design [1].

Designing of a barrel shifter using 180nm technology using Cadence software tool is shown in [2]. And also stated that, how designing of a barrel shifter with an ultra-low power multiplexer [2].

A design of a 32-bit barrel shifter that can be used in (ARM7) RISC processor and was implemented with VHDL [3]. After the RTL design, layout of the design had been verified by Tanner EDA 14.1 tool and Mentor Graphics (IC-Station) using 16 nm technology.

In [4], authors demonstrated the basic functionalities of a barrel shifter. In addition, they

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have done a research on MUX based and Mask based designs of barrel shifters and stated their comparisons.

Reference [5] shows a design of full custom 2-bit barrel shifter using 2x1 MUX in CMOS 45nm technology with virtuoso software. They have stated that their design using pass transistor logic is reduced 76.3% of power and 91.77% of time delay with respect to a conventional design.

The design of 4 bit and 8-bit barrel shifter circuits using Xilinx12.1 ISE software tools was shown in [6]. This design can be expanded to larger value of bits by using the same design by introducing slight changes.

The power and delay of barrel shifter design was shown at gate level, architecture level and an environment level was represented in [7].

References [8] & [9], demonstrated how virtual inputs and outputs can be applied and monitored with the incorporation of VIO block in the 32-bit processing design. It also showed the analysis of low power achievement with the structural design style and clock constraint.

Reference [10] demonstrated analysis of power for 64-bit ALCCU for the I/O standards LVCMOS12, LVCMOS 15, LVCMOS18, LVCMOS25 and LVCMOS33 verified with wide frequency range of up to 20GHz.

III. WORKING OF BARREL SHIFTER

The design, 64-bit barrel shifter will perform 4 different operations as listed in **Table 1.** The RTL module design has 4 inputs and 3 outputs. Inputs are clk, Din, OP_SEL, SRC and the outputs are shift_Leftright, rotate_Leftright, Dout as illustrated in **Figure 1**. In this design, clk, shift_Leftright, rotate_Leftright are scalar signals, Din is (n+1)-bit where n=63, OP_SEL is 2-bit, SRC is 6-bit and the Dout is (n+1)-bit lengths as shown in Figure 1. SRC is nothing but 6-bit count for shift or rotate operations. As it is a 64 bit barrel shifter, 26 = 64 positions can be either shifted or rotated.

As it is a sequential circuit design, it is synchronized with clock signal. And when the clk is at positive edge then only the barrel shifter can perform its operations. The OP_SEL is used for operation selection. If OP-SEL[1] is true, then it performs rotate operations else it will perform shift operations as shown in Figure 2. If OP-SEL[1]=1 and OP-SEL[0] =0 then it will perform rotate left operation else if OP-SEL[1]=1 and OP-SEL[0] =1 then it will perform right rotation operation. The number of rotations can be decided by the SRC count value as illustrated in **Figure 2**.

Table 1 Barrel Shifter Operations

OP-SEL		Mode of Operation	Description
S1	S0		
0	0	Shift left	Logic shift left, 0 is shifted through the rightmost (LSB) bit
0	1	Shift right	Logical shift right, 0 is shifted through the leftmost (MSB) bit
1	0	Rotate left	Left rotate, the rightmost bit is shifted back in from the right.
1	1	Rotate right	Right rotate, the rightmost bit is shifted back in from the left.

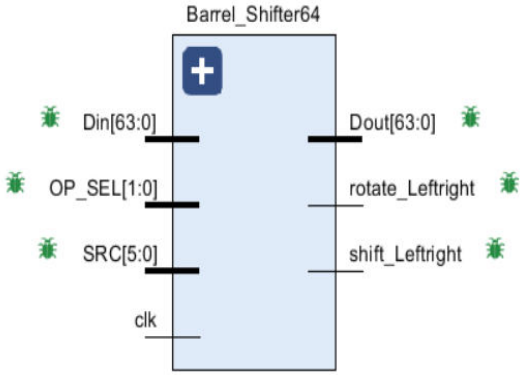

Figure 1 Input of Barrel Shifter 64-bit

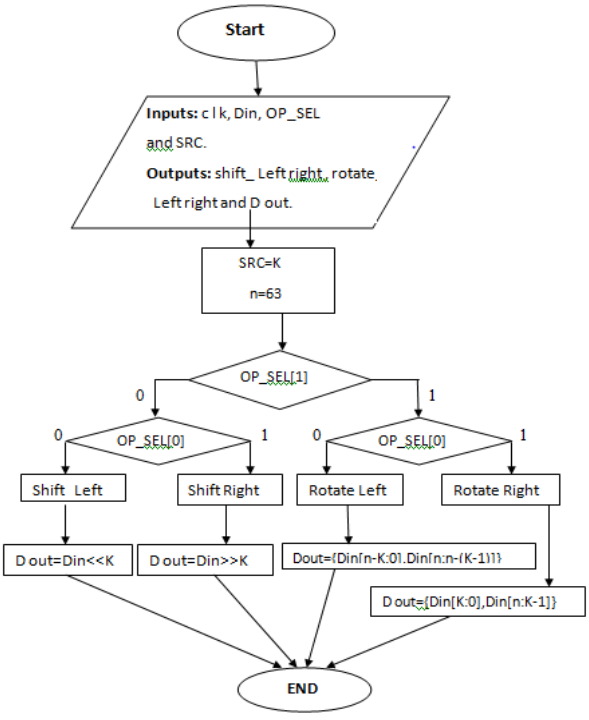

Figure 2 Flow Chart of 64-bit barrel shifter

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Similarly, If OP-SEL[1]=0 and OP-SEL[0] =0 then it will perform shift left operation else if OP-SEL[1]=0 and OP-SEL[0] =1 then it will perform shift right operation. The number of shifts can be decided by the SRC count value.

IV. FRONT END DESIGN FLOW AND VERIFICATION OF BARREL SHIFTER

The general traditional design and verification flow is illustrated in Figure 3. The design is implemented with a front end software tool, Vivado 2018.1. The following steps are to be used for the design and verification of HDL based design.

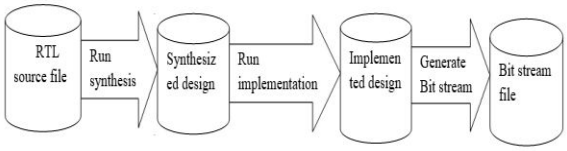

Figure 3 General FPGA Design Flow

Step-i: Create an RTL project with project name as Barrel_Shifter_VIO. At the time of project creation, target FPGA details will be selected, using which we have to verify our design.

Step-ii: Go to add sources and create a HDL file for 64 bit barrel shifter with ' .v' extension. The RTL design schematic for the created file can be viewed at elaboration process as shown in **Figure 4** in detail.

Step-iii: Simulate the design. To simulate the design, XSim, simulator was used. A test bench module is written, that provide a documented, and a required set of stimuli that has to be applied to a barrel shifter to verify the logical correctness of the design.

It consists of 73 cells, 139 I/O ports, 375 look up tables (LUTs), 67 registers, and 64 multiplers and one buffere control register. These details are obtained after synthesis process of the barrel shifter design. It gives the area of the design within the architecture of Artix 7 FPGA and the corresponding resources utilized by the design and the generated report is illustrated in **Table 2.**

Table 2 Utilization Report of 64-bit Barrel Shifter

Name	Slice LUTs (63400)	Slice Registers (126800)	F7 Muxes (31700)	Bonded IOB (210)	BUFGCTRL (32)
barrelshifter_64_bit	375	67	64	139	1

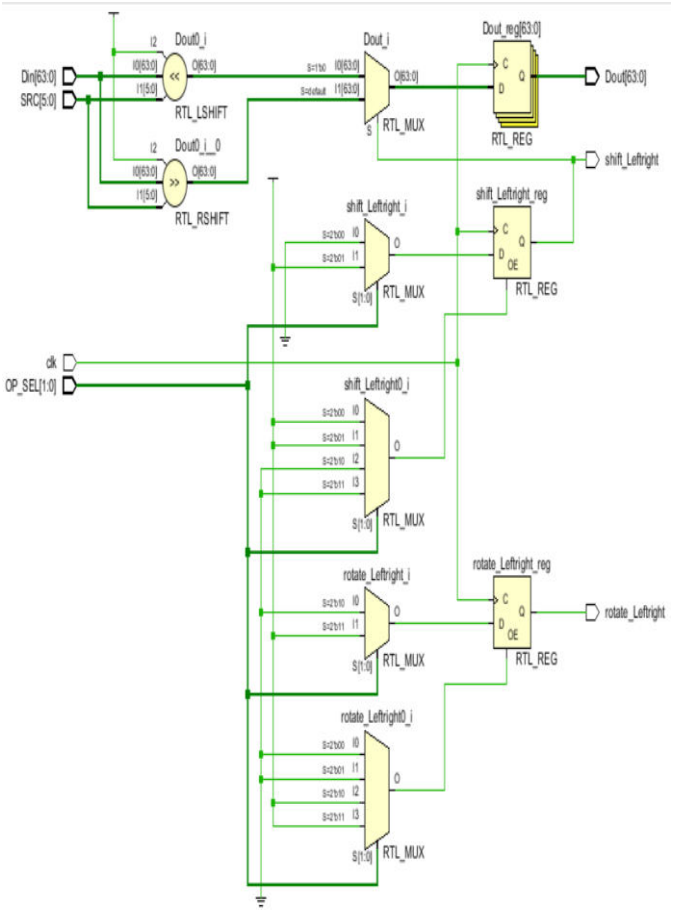

Figure 4 The hardware generated inside the barrel shifter-64 bit

Step-iv: Add an IP, VIO block to the design to verify the emulated results [8]. To do this, Go to catalog window, select "Debug and verification" and Open debug then Click on select VIO (Virtual Input Output). Then, Customized window will be opened.

Step-v: At this customized window, we can specify the required number of probes in both in and out directions of VIO module. The input direction of VIO probes are nothing but the outputs of the DUT. And the output probes of VIO are given to the inputs of DUT. With these settings, generate the VIO block [8, 9, 10].

Step-vi: Now create a top module, where it consists of both VIO and DUT are components and a common clock is applied to both VIO and DUT. For this top module, only one input that drives both VIO block and a DUT [8, 9, 10].

Step-vii: Create an XDC file. To do this step, go to elaborate design process, select I/O mapping or XDC (Xilinx Design Constraints) creation option and give scalar port clk to E3 pin of FPGA (Nexys DDR 4

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board). In this elaboration process, we can view the RTL for top design as shown in **Figure 5.**

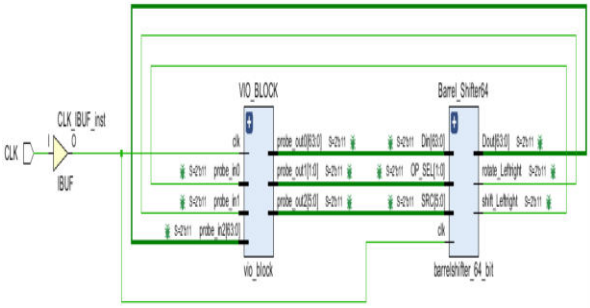

Figure 5 RTL View of Top-Level Design

Step-viii: Synthesize the design to generate the gate level net list and will generate .ngc file. It will be used in the implementation process.

Step-ix: Implement the design. It actually subdivided into three different sub tasks named as translation, mapping and placement and routing. In translation processing, it will merge the incoming netlist files and constraints files in to Xilinx design file [10]. Mapping is nothing but it is a technology mapping. It will fit the design in to a target device resource. Then the next step is, it will place and route the design with timing constraints [11, 12, 13, 14, 15].

Step-x: Generate bitstream of the implemented design and open hardware manager, auto connect the device and then program the target FPGA to verify the results [11, 15].

V. RESULTS AND DISCUSSION

A. *Simulation Results*

For testing the barrel shifter, given Din=ffff00000000000f, OP_SEL=00 and SRC=4 then the output will be shifted left by 4 times. Therefore, Dout= fff00000000000f0 as shown in **Figure 6.**

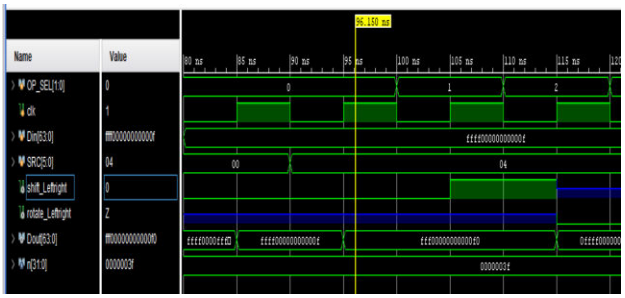

Figure 6 Simulation Results for Shift Left Operation

If Din=ffff0000ffff0000, OP_SEL=01 and SRC=4 then the output will be shifted right by 4 times. Therefore, Dout= 0ffff0000ffff000 as shown in **Figure 7**. Similarly, for OP_SEL=10, the output will rotate left, for OP_SEL=11, the output will rotate right.

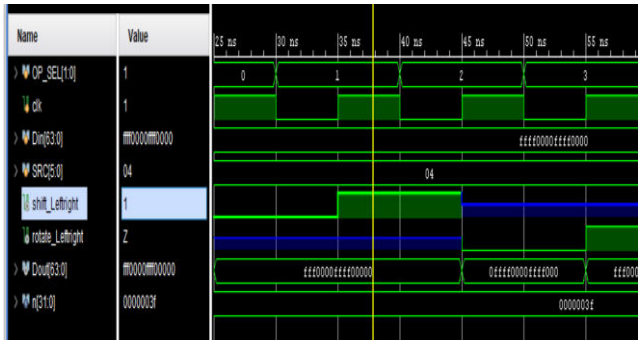

Figure 7. Simulation Results for Shift Right Operation

B. *Virtual I/O Verification*

After completion of the ten processing steps, specified in the design flow, hardware virtual input/output window will invoked by the tool. At this window, we can enter the virtual inputs and can observe the outputs instantaneously. The barrel shifter design inputs are driven by the VIO block and the outputs of the barrel shifter will be monitored in the VIO hardware block. Therefore, the outputs of barrel shifter are nothing but VIO inputs and inputs of the barrel shifter are nothing but outputs of VIO block. The tested value for Din = 0000_FFFF_0000_00FF and OP_SEL = 10 (rotate left operation) and SRC=04 then four times rotated bits will be observed at Dout = 000F_FFF0_0000_0FF0 as illustrated in Figure 8.

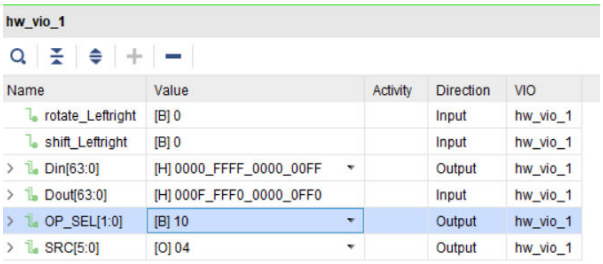

Figure 8. Virtual results for rotate_left operation

The power report of the 64-bit barrel shifter is illustrated in Figure 9. This power report generated is based on the I/O standard, LVCMOS12, and 100MHz clock consideration. The total on chip power consumption is 0.085W. It is a collective power of 21% due to I/Os, 23% due to logic and 57% is due to all the signals and clocks used in the design. Overall 98% of power is due to static and only 2% is due to dynamic power.

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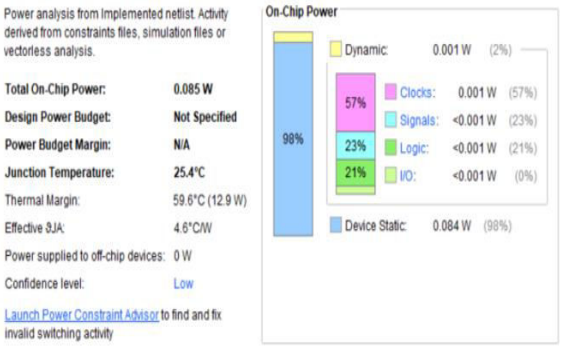

Figure 9. Power report of 64-bit Barrel Shifter

Figure 10. Timing Summary report of Barrel Shifter

The satisfactory timing report is generated in the implementation process as shown in **Figure 10**. Worst negative slack is 27.074ns at Setup time and worst negative slack = 0.094ns at hold time and worst pulse width slack = 15.250ns at a total pulse width.

Conclusions

The proposed design is a 64-bit barrel shifter, which was implemented and verified successfully with the target FPGA board, Nexys DDR4. The design has been verified with onboard clock of 100Mhz. The design can be enhanced to 128-bit also. However, the latest processing devices are of 64-bit and 32-bit size in today's technology. Majority of the earlier barrel shifter designs are with 32-bit sized. Therefore, the proposed design is implemented with 64-bit size. It has been achieved with satisfactory power and timing report as specified in **Figure 9 and 10**.

The future scope of this proposed research can be creation of custom IP design with 28nm and beyond 28nm technologies.

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Author Details:

Dharmavaram Asha Devi, Member IEEE, Fellow IETE.

The Author is working as a Professor in the Department of Electronics & Communication Engineering, SNIST, Hyderabad. She became an Associate Member of IETE in Dec-2000 from the Institute of Electronics and Telecommunication Engineering, New Delhi, India. She awarded M.Tech. Degree in Digital Systems and Computer Electronics from JNTU Anantapur in 2005. She achieved a Doctorate Degree from Sri Krishnadevaraya University, Anantapur in Dec 2011, for her research contribution in Embedded System based Soil Analysis under the supervision of Prof. K. Malakondaiah, from SKU, Anantapur.

She had 18 years of academic, including 8 Years of R & D Experience. She has published more than 35 papers in International Journals and presented 45+ research papers in National and International level conferences on behalf of her research work done in Embedded Systems and VLSI Designs.

M. Suresh Babu, has 22 years of teaching experience in MCA and Computer Science Engineering departments. He awarded PhD degree in Computer Science from Sri Krishnadevaraya University, Anantapur, for his contribution on "A study on forecasting stock market index value using data mining techniques" in 2012. He achieved M.Phil (Computer Science) from Bharthiar University in 2007 and

Master of Computer Applications from Osmania University, Hyderabad in 1997. He published papers around 90+ in various National and International level Journals and conferences. His area of research interest is data warehouse, DBMS & RDBMS and Ubiquitous computing.

Thirupari Sindhuja, graduated from Sreenidhi Institute of Science and Technology in 2019. She had completed a **VLSI-**Custom Layout Design training from the Institute of Silicon Systems Pvt. Ltd., Hyderabad from August 2019 to November 2019 using Cadence Tools. She worked as Project Assistant for 3 Months under TEQIP-III project under the guidance of Dr. D. Asha Devi. She had an experience of several layout designs and their verification and floor planning under GPDK 45nm, TSMC 130nm, Intel 7nm Technology nodes. At present she is working as a Layout Design Engineer in Sankalp Semiconductor-HCL Technologies.