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A MULTILEVEL INVERTER CAPABLE OF POWERFACTOR CONTROL BASED ON POD TECHNIQUE

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ABSTRACT: Due to the increasing demand on the renewable energy sources, grid connected electrical converter systems are getting additional and additional vital than ever before For grid - connected operation, the electrical converter ought to meet the sub sequent requirements. This paper proposes a replacement multi-level electrical converter topology supported a H-bridge structure with four switches connected to the dc- link. Supported a POD (Phase opposition disposition) modulation methodology, a replacement PWM methodology that requires just one carrier signal is recommended. The switch sequence to balance the electrical device voltage is additionally thought-about. In addition to those, the planned topology needs minimum number of element count to extend range the amount the quantity} of voltage level. Operational principle of the planned electrical converter is verified through simulation.

I.INTRODUCTION

With the advent of multilevel inverters, the overall performance of medium and excessive- voltage drives have changed substantially. As the range of voltage tiers increases, the output voltage is in the direction of sine wave with reduced harmonic content material, improving the performance of the force greatly as provided. One of the pioneering works in the field of multilevel inverters is the neutral factor clamped inverter. the alternative hand, the use of multiple isolated dc resources using H-bridges for plasma stabilization generating more than one voltage stages become presented. The work analyzes the problems with the scheme of cascading multiple rectifiers and proposes an answer for balancing the capacitors. The work provided generates more than one voltage levels by switching the load modern via capacitors. Here, the voltage through the capacitors may be maintained at favored fee by means of converting the route of load contemporary via the capacitor

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through choosing the redundant states for the identical pole voltage. The paintings combines the concepts of labor provided.Here, the floating capacitor H-bridges are used to generate a couple of output voltages. The voltages of the capacitors are maintained at their meant values via switching via redundant states for the same voltage stage. The works cope with factors of the use of cascaded H-bridges and suggest diverse efficient manage algorithms. Modular multilevel converters that are very famous in HVDC programs are another style of multilevel converters which can be used for motor power applications as supplied. The concept of cascading flying capacitor inverter with impartial factor clamped inverter is presented. Similar concept has been made available commercially as ABB ACS 2000. The concept of growing the variety of levels using flying capacitor inverter with cross linked capacitors has been supplied.An thrilling configuration to generate 17 voltage levels using a couple of capacitors. However the capacitor voltages can't be balanced instantaneously. They can be balanced simplest on the fundamental frequency. A single-phase seventeen-degree inverter configuration is presented uses huge variety of energy materials and has a floating load. This is more suitable for STATCOM programs. An appealing set of rules for running seventeen degree inverter has been offered . In the prevailing task, we suggest a new 17- stage inverter formed with the aid of cascading three-degree flying capacitor inverter with floating capacitor H-bridges which makes use of a unmarried dc deliver and derives all of the required voltage levels from it. The performance of the proposed configuration is experimentally validated each for consistent country operation and at some point of transients and the effects are supplied.

II.POWER CIRCUIT TOPOLOGY:

The proposed converter is a hybrid multilevel topology employing a 3-stage flying capacitor inverter and cascading it with 3 floating capacitor H-Bridges. The three-phase strength schematic is proven in Fig. 1. The voltages of capacitors AC1, BC1, and CC1 are maintained at Vdc/2. Capacitors AC2, BC2, and CC2 are maintained at voltage degree of Vdc/4. Similarly capacitors AC3, BC3, and CC3 are maintained at voltage degree of Vdc/eight and capacitors AC4, BC4, and CC4 are maintained at voltage stage of Vdc/16. Each cascaded H-bridge can either add or subtract its voltage to the voltage generated by using its preceding stage. In addition to that, the CHBs also can be bypassed. The resulting inverter pole voltage is the mathematics sum of voltages of each level. The schematic diagram for one

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section of the proposed converter is shown in Fig. 2. The switch pairs (AS1, AS1'), (AS2, AS2'), (AS3, AS3'), (AS4, AS4'), (AS5, AS5'), (AS6, AS6'), (AS7, AS7'), and (AS8, AS8') are switched in complementary fashion with appropriate dead time. Each switch pair has wonderful good judgment states, namely top device is ON (denoted by using 1) or the bottom tool is ON (denoted through zero). Therefore, there are 256 (28) wonderful switching combos possible. Each voltage level may be generated the use of one or more switching states (pole voltage redundancies). By switching through the redundant switching combos (for the same pole voltage), the current thru capacitors may be reversed and their voltages may be managed to their prescribed values. This technique of balancing the capacitor voltages at all load currents and strength factors instantaneously has been determined for 17 pole voltage ranges. They are 0, Vdc/16, Vdc/8, three Vdc/16, Vdc/four, five Vdc/16, three Vdc/eight, 7 Vdc/16, Vdc/2, nine Vdc/sixteen, five Vdc/eight, eleven Vdc/sixteen, 3 Vdc/4, thirteen Vdc/sixteen, 7 Vdc/8, 15 Vdc/sixteen, and Vdc. However, through switching thru all the viable pole voltage switching mixtures, 31 wonderful pole voltage degrees can be generated the use of the proposed topology. In the additional 14 ranges, the voltages of capacitors may be balanced simplest in a essential cycle.

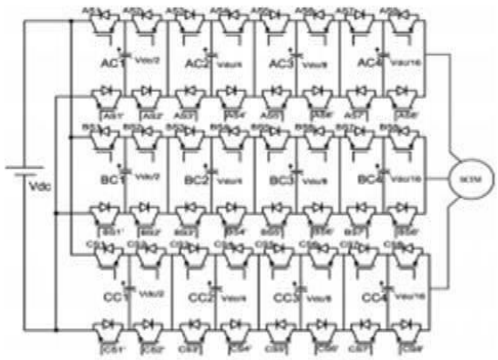

Figure.1. Three-phase power schematic of the seventeen-level inverter configuration formed by cascading three-level flying capacitor inverter with three H-bridges using a single dc link.

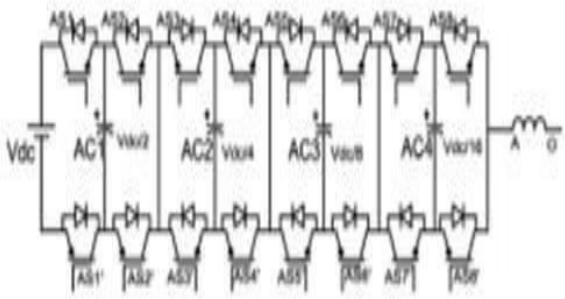

Figure 2. One phase of the 17-level inverter configuration formed by cascading three-level flying capacitor inverter with three H-bridges using a single dc link.

II.SPACE VECTOR CONTROL REGION :

Each pole of the three-phase inverter can generate one of the 17 discrete pole voltage tiers particularly zero, Vdc/16, Vdc/8, three Vdc/sixteen, Vdc/4, five Vdc/sixteen, three

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Vdc/eight, 7 Vdc/16, Vdc/2, nine Vdc/sixteen, 5 Vdc/eight, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16, and Vdc. For the proposed 3-phase inverter, there is a total of 4913 (173) pole voltage mixtures. while marked on a area vector plane spread throughout 817 awesome space vector places. Each of the 817 space vector locations could have more than one pole voltage combination (segment voltage redundancy) with special not unusual mode voltages.

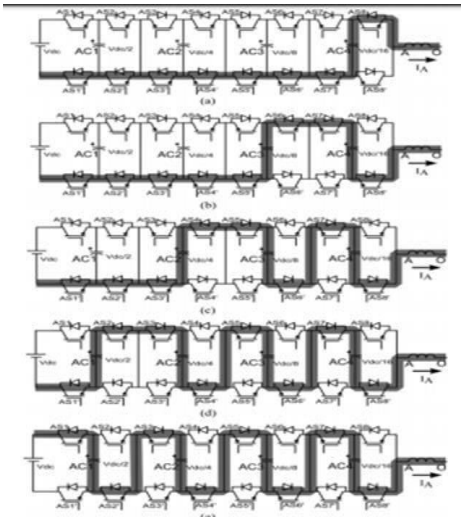

Figure 3. Switching Redundancies for pole voltage of Vdc/16.

III.IMPLEMENTATION:

Signals for the inverter is provided in Fig. The control algorithm may be whatever like V/f or vector manipulate or any other set of rules which demands a selected set of reference voltage tiers for the three levels. These voltage stages are despatched to degree-shifted provider primarily based area vector PWM technology algorithm carried out in DSP as defined in [24], the output of that is (fed to FPGA) a set of level information and the PWM signal for each section. This facts is fed to a stage synthesizer which generates the instant stage primarily based on the PWM signal and Fig. 4. Capacitor voltage version with utility of redundant states for pole voltage of Vdc/16 for nice modern-day. Fig. 5. Space vector polygon fashioned with the proposed 5-level inverter. The extent records. The instantaneous degree statistics is fed to a switching nation generator which generates the perfect switching country primarily based at the demanded degree, the country of capacitor voltages and current. This is accomplished by using implementing the logic described in Table I as a look up table in FPGA.

IV.SIMULATION RESULTS

A)EXISTING RESULTS

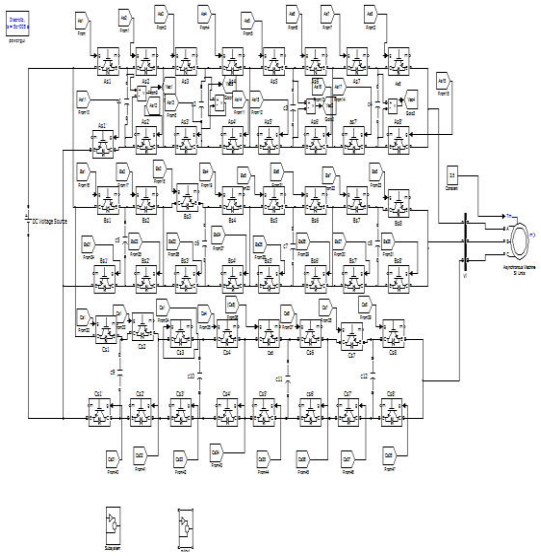

Figure 4.
MATLAB/SIMULINK diagram of the existing 17 level inverter

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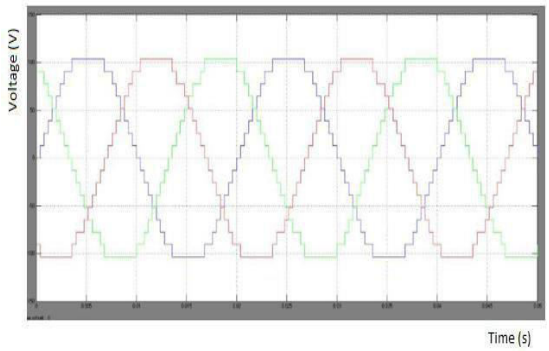

Figure 5. Three phase out put voltage of inverter

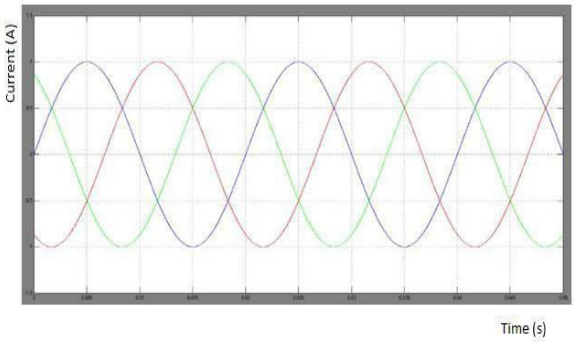

Figure 6. Three phase current wave form

B) EXTENSION RESULTS

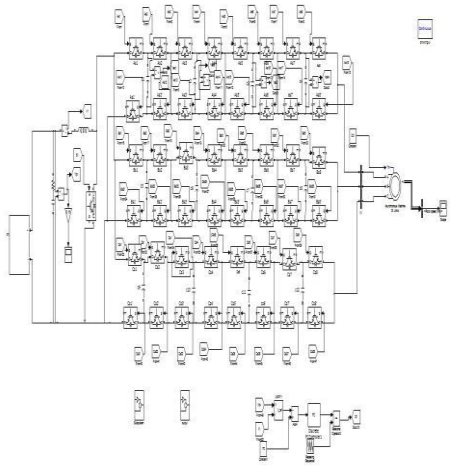

Figure 7 MATLAB/SIMULATION diagram of proposed17 level inverter with PV system Based POD technique

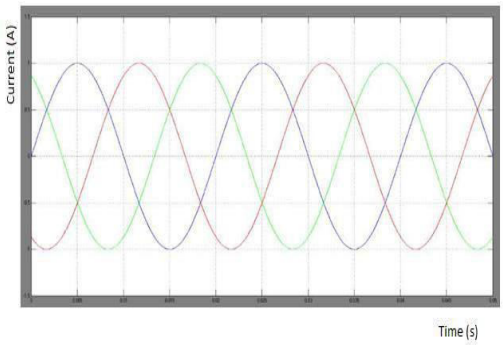

Figure 8.Out put current wave form

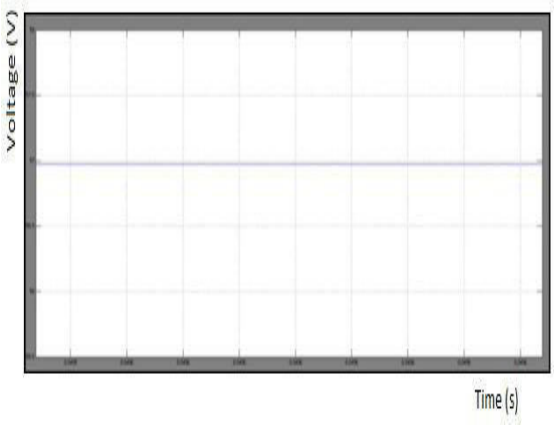

Figure 9. pv voltage

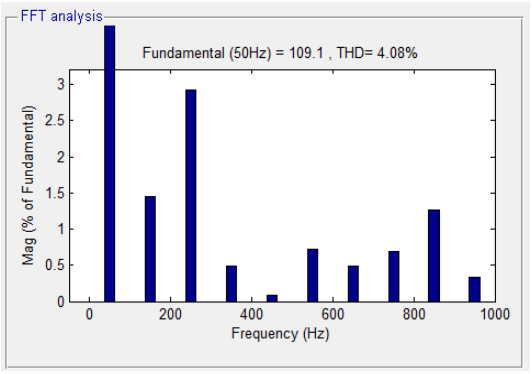

Figure 10 FFT analysis of proposed17 level inverter with PV system Based POD technique

CONCLUSION

A new 17-stage inverter configuration formed via cascading a 3-stage flying capacitor and 3 floating capacitor H-bridges has been proposed for the first time. The voltages of every of the

capacitors are managed without delay in few switching cycles in any respect loads and energy factors obtaining high performance output voltages and currents. The proposed configuration uses a unmarried dc hyperlink and derives the alternative voltage tiers from it. This allows returned-to-back converter operation in which power may be drawn and furnished to the grid at prescribed energy element. Also, the proposed PV related 17-degree inverter has advanced reliability as well as advanced strength element of the grid primarily based POD technique. Another advantage of the proposed configuration is modularity and symmetry in shape which permits the inverter to be extended to extra number of phases like 5-phase and 6-phase configurations with the same manipulate scheme.

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