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A VOLTAGE CONTROLLED DSTATCOM FOR POWER QUALITY IMPORVEMENT

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ABSTRACT
In this Project, a new PV connected DSTATCOM topology with reduced dc link voltage is proposed. The main aim of PV is to supply the dc to storage device or capacitor. The distribution static compensator (DSTATCOM) is used for load compensation in power distribution network. In the presence of feeder impedance, the inverter switching distorts both the PCC voltage and the source currents. In this situation, the source is termed as nonstiff. In this paper, a new topology for DSTATCOM applications with non stiff source is proposed. The compensation performance of any active filter depends on the voltage rating of dc-link capacitor. In general, the dc-link voltage has much higher value than the peak value of the line-to-neutral voltages. This is done in order to ensure a proper compensation at the peak of the source voltage. A new PV connected DSTATCOM topology with reduced dc link voltage is proposed.

KEY TERMS: PV, DSTATCOM, Power quality,

I.INTRODUCTION
Both electric utilities and end users of electrical power are becoming increasingly concerned about the quality of electric power. The term power quality has become one of the most prolific buzzword in the power industry. The issue in electricity power sector delivery is not confined to only energy efficiency and environment but more importantly on quality and continuity of supply or power quality and supply quality. Electrical Power quality is the degree of any deviation from the nominal values of the voltage magnitude and frequency. Power quality may also be defined as the degree to which both the utilization and delivery of electric power affects the performance of electrical equipment. From a customer perspective, a power quality problem is defined as any power problem manifested in voltage, current or frequency deviations that result in power failure or disoperation of customer equipment. Power quality is certainly a major concern in the present era, it

becomes especially important with the introduction of sophisticated devices, whose performance is very sensitive to the quality of power supply. Modern industrial processes are based a large amount of electronic devices such as programmable logic controllers and adjustable speed drives. The electronic devices are very sensitive to disturbances and thus industrial loads become less tolerant to power quality problems such as voltage dips, voltage swells, harmonics, flickers, interruptions and notches..

II.LITERATURE SURVEY

Power Quality:

Our technological world has become deeply dependent upon the continuous availability of electrical power. In most countries commercial power is made available via nationwide grids, interconnecting numerous generating stations to the loads. The grid must supply basic national needs of residential, lighting, heating, refrigeration, air conditioning and transportation as well as critical supply to governmental, industrial, financial, commercial, and medical and communications communities. Commercial power literally enables today's modern world to function at its busy pace. Many power problems originate in the commercial power grid, which with its thousands of miles of transmission lines is subject to weather conditions such as hurricanes, lightning storms, snow, ice and flooding along with equipment failure, traffic accidents and major switching operations. Also power problems affecting today's technological equipment are often generated locally within a facility from any number of situations such as local construction, heavy start up loads, faulty distribution components and even typical background electrical noise. Widespread use of electronics in everything from home electronics to the control of massive and costly industrial processes has raised the awareness of power quality. Power quality or more specifically a power quality disturbance is generally defined as any change in power (voltage, current or frequency) that interferes with the normal operation of electrical equipment.The study of power quality and ways to control it is a concern for electric utilities, large industrial companies, businesses and even home users. The study has intensified as equipment has become increasingly sensitive to even minute changes in the power supply voltage, current, and frequency.

Definition: "Power Quality is the degree to which both the utilization and delivery of electric power affects the performance of electric equipment".In general there is no unique definition of power quality. The power quality problem can be viewed from two different angles related to each side of the utility meter, namely the Utility and Consumer. An alternative definition of PQ is adopted.A perfect power supply would be one that is always available always within voltage and frequency tolerances and has a pure

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noise-free sinusoidal wave shape. Power Quality means the ability of utilities to provide electric power without interruption.Mainly the seven types of Power Quality problems are there. They are

1. Transients.
2. Interruptions.
3. Voltage Sag.
4. Voltage Swell.
5. Waveform distortion.
6. Voltage fluctuations.
7. Frequency variations.

III.PROPOSED DSTATCOM CONCEPT

This section provides description of power circuit diagram of a three-phase traditional and proposed DSTATCOM topology employed in distribution system. Fig. is considered as traditional topology throughout this project. It contains a three-phase, four-wire, and two-level, neutral-point-clamped voltage source inverter. It requires two dc storage capacitors but each leg of the VSI can be controlled independently [8]. V_{sabc} and I_{sabc} are source voltages and source currents of phases a, b, and c respectively. Feeder impedance in each phase is composed of resistance Rs and inductance Ls. V_{tabc} and I_{labc} are the load terminal voltages and load currents in phases a, b, and c respectively. Loads used here have both linear and non-linear elements which may be balanced or unbalanced. Interfacing inductance and resistance of VSI in each phase are L_f and R_f respectively. DSTATCOM injected currents are I_{fabc} in respective phases. The dc link capacitors are represented by $C_{dc1} = C_{dc2} = C_{dc}$, whereas voltages maintained across them are $V_{dc1} = V_{dc2} = V_{dc} = V_{dcref}$ respectively. Proposed topology, shown in Fig., integrates DSTATCOM conventional topology with front end L filter replaced by LCL filter, followed by a series capacitor C_{se}. Introduction of LCL filter significantly reduces the size of the passive component of the VSI and improves the reference tracking performance. Addition of series capacitor to interfacing filter significantly reduces the dc link voltage and therefore the rating of the VSI. Here, R_1 and L_1 represent the resistance and inductance respectively at the filter side, R_2 and L_2 represent the resistance and inductance respectively at the grid side, and C is the filter capacitance forming LCL filter part in all three phases.I_{f1abc} and I_{f2abc} are currents at filter and grid side in phase a, b, and c respectively. A damping resistance R_d is used in series with C to damp out resonance and to provide passive damping to the overall system. V_{cabc} and I_{cabc} are voltages across and currents through the branch containing series C and R_d in three phases respectively.

4.3 GENERATION OF REFERENCE CURRENTS:

DSTATCOM is operated in such a way that the source currents are balanced, sinusoidal, and in phase with respective terminal voltages. Also, average load power and losses in the VSI are supplied by the source. Since, source considered

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here is non-stiff in nature, direct use of terminal voltages to calculate reference currents will not provide satisfactory compensation.

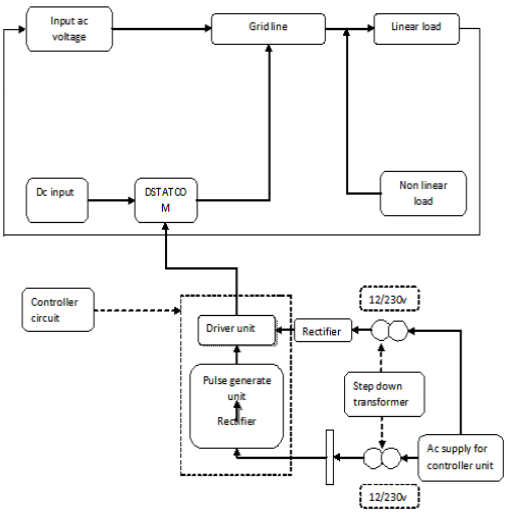

Fig.1 Traditional DSTATCOM topology in distribution system

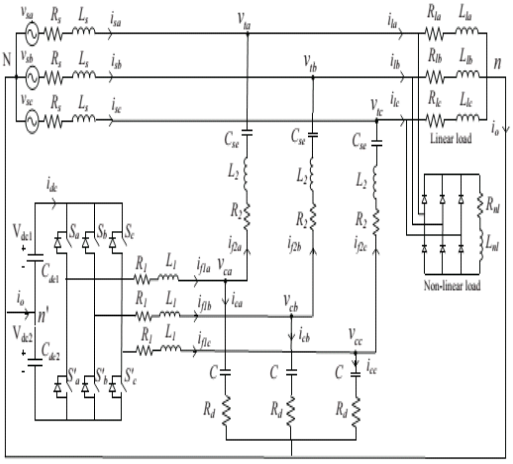

Fig.2. Proposed DSTATCOM topology in distribution system

$$i^*_{f2a} = i_{la} - i^*_{sa} = i_{la} - \frac{v^+_{ta1}}{\Delta^+_1}(P_{lavg} + P_{loss})$$

$$i^*_{f2b} = i_{lb} - i^*_{sb} = i_{lb} - \frac{v^+_{tb1}}{\Delta^+_1}(P_{lavg} + P_{loss})$$

$$i^*_{f2c} = i_{lc} - i^*_{sc} = i_{lc} - \frac{v^+_{tc1}}{\Delta^+_1}(P_{lavg} + P_{loss})$$

where, , , and are fundamental positive sequence voltages at the respective phase load terminal and $\Delta+1 = ()^2+()^2+()^2$. Here, P_{lavg} represents average load power and P_{loss} represents the total looses in the inverter. Average load power is calculated using a moving average filter for better performance during transients and can have a window width of half cycle or full cycle depending upon the type of harmonics present in the load currents. Total losses in the inverter P_{loss}, computed using a proportional integral (PI) controller, helps in maintaining the dc link voltage ($v_{dc1}+v_{dc2}$) at a predefined reference value ($2V_{dcref}$) by drawing a set of balanced currents from the source and is given as follows:

$$P_{loss} = K_p\, e + K_i \int e\, dt \qquad (4.2)$$

where, K_p, K_i, and $e=2V_{dcref} - (V_{dc1}+V_{dc2})$ are proportional gain, integral gain, and voltage error of the PI controller respectively.

IV.DESIGN OF PROPOSED DTATCOM TOPOLOGY:

1) Design of LCL Filter: While designing optimal values of LCL filter components, constraints such as cost of inductor, resonance frequency (f_{res}), choice of damping resistor (R_d), and attenuation at switching frequency (f_{sw}) must be considered [14]. At higher frequencies, impedance offered by C_{se} will be much lower than that of L_2 and

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can be neglected while designing LCL filter parameters. Consider only L_1 of LCL filter is used. Small ripple in current will lower the IGBT switching frequency and lowers the losses. It can be seen that smaller ripple current results in higher inductance and so more core losses. Therefore, a current ripple of 20% is taken while compromising ripple and inductor size. Use of series capacitor has allowed us to reduce the dc link voltage as low as 110 V. Therefore, placing new value of ripple current and dc link voltage Vdc new in (4.4), while keeping f_{max} constant at 10 kHz, value of L_1comes out to be 2.75 mH. To restrict switching frequency below 10 kHz, L_1 is taken more than calculated value and 3 mH is chosen. Once L_1 is chosen to attenuate lower order harmonics, L_2 and C need to be designed for elimination of higher order harmonics. Following transfer functions provide the information of LCL filter behaviour at the higher frequencies:

$$\frac{I_{f1}(s)}{V_{inv}(s)} = \frac{s^2 + 1/L_2C}{s\,L_1(s^2 + (L_1 + L_2/L_1\,L_2\,C))}$$

$$\frac{I_{f2}(s)}{V_{inv}(s)} = \frac{1/L_1\,L_2C}{s(s^2 + (L_1 + L_2/L_1\,L_2\,C))}$$

$$\frac{I_{f2}(s)}{I_{f1}(s)} = \frac{1/L_2C}{s^2 + (1/L_2\,C)}$$

Expressions relating pole (p) and zero (z) are given in below, whereas resonance frequency is given by

$$p = z\sqrt{1+k}$$

$$f_{res} = \frac{1}{2\,\pi}\sqrt{\frac{1+k}{k\,L_1C}}$$

where, z = $1/L_2C$ and k = L_2/L_1. Resonance frequency must be greater than the highest order of harmonics current to be compensated. If highest harmonics order to be compensated is 40 and taking a safety factor of 20%, f_{res} turns out to be 2400 Hz. L_2 greater than L_1 reduces distortion in current but again at the price of more loss and cost. Therefore, to ensure low loss and high efficiency, a lower value of k is selected. A lower k ensures that the poles are not far away from zero as seen. Consequently, it ensures decrease in overshoot. A higher C will provide a low impedance path for harmonics, but will draw more reactive current from VSI which further increases loss inL1and IGBT switch, whereas a smaller capacitance will not provide sufficient attenuation which in turn is compensated by selecting larger inductor. As a trade off between these requirements, C=10μF is chosen. Finally k, computed is found to be 0.172, results in approximately L_2=0.6Mh.At f_{res}, equivalent impedance of the LCL filter approaches to zero and system may become unstable. But, it can be prevented by inserting a resistance

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(R_d) in series with the capacitor. It is chosen in proportion to capacitive reactance at f_{res} such that losses are minimum. At f_{res}, reactance offered by C is 6.63 Ω. Since losses in R_d are compensated by taking current from source, it must be minimized. Taking these into account, a resistance of 15 Ω, which is nearly two times reactance offered by C at resonance, is chosen.

2) Series capacitor (Cse): Main criterion for designing of C_{se} is that it should provide a low impedance path for the fundamental frequency current component . While designing C, it was ensured that it provides a high impedance path for the lower order harmonics. Therefore, negligible fundamental current will be drawn by C and can be neglected at the fundamental frequency. So, in simplified circuit, R1, L1, R2, L2, and C_{se} are connected in series. In this case, fundamental current supplied by the filter is given as

$$I_{f1} = \frac{V_{inv1} - V_{t1}}{R_f + j\left(X_{l1} - X_{se1}\right)}$$

where, $R_f = R_1+R_2$, $X_{l1} = \omega / (L_1+L_2)$, $X_{se1} = 1/\omega_1 C_{se}$, V_{t1} is fundamental rms PCC voltage, and V_{inv1} is fundamental rms voltage per phase available at VSI terminal

V.MATLAB / SIMULATION RESULTS

PROPOSED PV CONNECTED DSTATCOM for PQ Improvement Features using PI Controller

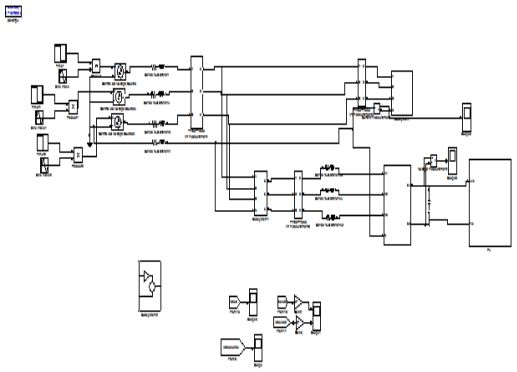

Fig.3 Matlab/Simulink Model of PV CONNECTED DSTATCOM for PQ Improvement Features using PI Controller

Fig. shows the Matlab/Simulink Model of Conventional DSTATCOM for PQ Improvement Features using PI Controller.Advantages of proposed topology over traditional topology are that it uses lower rating of the VSI, smaller value of interfacing filter inductor, lower overall size, cost and weight. All these advantages are verified in digital environment using power system computer aided design software. In both topologies, a sampling time of 27.77μs is chosen which corresponds to720 samples/cycle. System parameters used for performance demonstration, are given in Table I.

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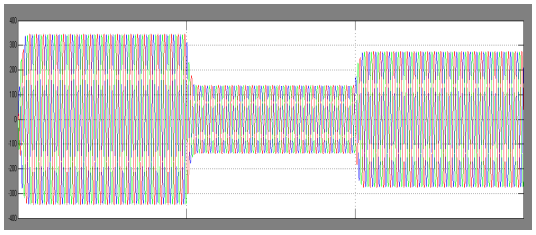

Fig 4 Source voltage under sag condition

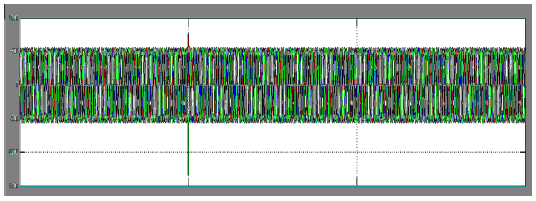

Fig 5 Load voltage

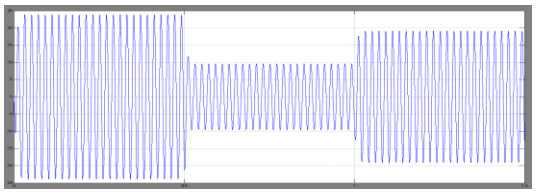

Fig 6 Single phase voltage under sag condition

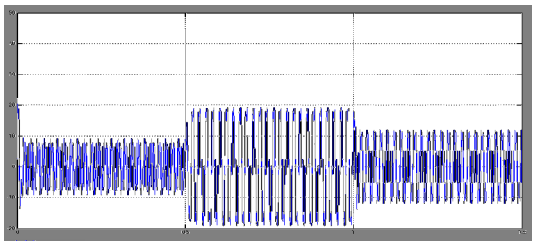

Fig 7 Compensated voltage

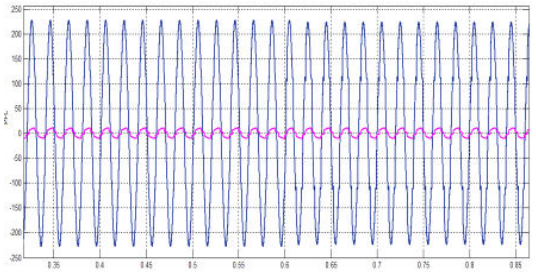

Fig 8. Power factor correction

CONCLUSION

The performance of the proposed scheme is compared with the traditional voltage controlled DSTATCOM. The proposed method provides the following advantages- at nominal load, the compensator injects reactive and harmonic components of load currents, resulting in UPF; nearly UPF is maintained for a load change; fast voltage regulation has been achieved during voltage disturbances and losses in the VSI and feeder are reduced considerably, and have higher sag supporting capability with the same VSI rating compared to the traditional scheme. Different types of voltage sag conditions should applied compensated in simulink environment. Additionally power factor correction and voltage regulation the harmonics are also checked, 20% voltage sag eliminated under t=0.5 to 1sec, thus the simulation results show that the proposed scheme provides DSTATCOM, a capability to improve several Power Quality problems (related to voltage and current).

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