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DESIGN OF LOW POWER LINEAR FEEDBACK SHIFT REGISTERS USING PULSED LATCHES

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Abstract
This paper focuses on the design of linear feedback shift register (LFSR) using pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. The functionality of the proposed architectures is verified through SPICE simulations using 0.27 µm CMOS technology parameters. The performance of the proposed architectures is compared on the basis of highest frequency and power consumption. The proposed shift register saves power compared to the conventional shift register with flip-flops.

Index Terms— digital, low power, area-efficient, flip-flop, pulsed clock, pulsed latch, shift register

I.INTRODUCTION

A SHIFT register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers, and image processing ICs. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register. A 16-megapixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations.The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.This paper proposes a low-power linear feedback shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock

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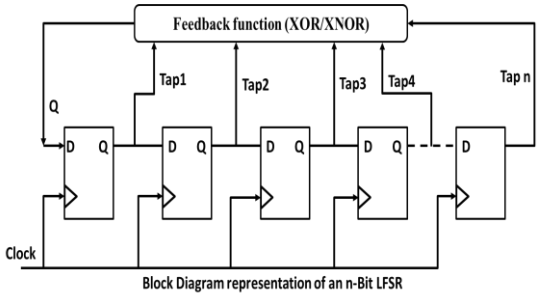
signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.This paper is structured as follows. In section II, the fundamentals of LFSR are briefly reviewed. The blocks used for the construction of LFSR are put forward in section III. Section IV describes the experimental results. Finally, conclusions are drawn in Section IV.

II.LINEAR FEEDBACK SHIFT REGISTERS

A linear feedback shift register (LFSR) is a shift register with feedback from some or the entire individual flip flops. The feedback network consists of exclusive-OR (XOR) or exclusive-NOR (XNOR) gates. The block diagram representation of LFSR. The outputs of flip flops are fed as input to the feedback network whose output serve as the input to the leftmost flip flop. The inputs to the flip flops are called taps and referred to as Tap1, Tap2, and so on in the diagram.



Block Diagram representation of an n-Bit LFSR

III.PROPOSED LFSR ARCHITECTURES

After a brief description to the circuit realization of the structural components in LFSR, in this paper proposes a low-power linear feedback shift register using pulsed latches. A master-slave flip-flop using two latches in Fig. 1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b). All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption.

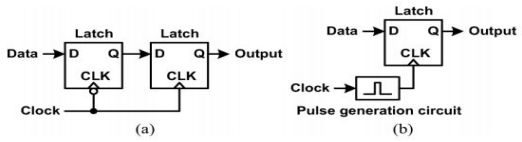


Fig. 1. (a) Master-slave flip-flop. (b) Pulsed latch.

The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 2. The shift register in Fig. 2(a) consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. 2(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width (T_{PULSE}). But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

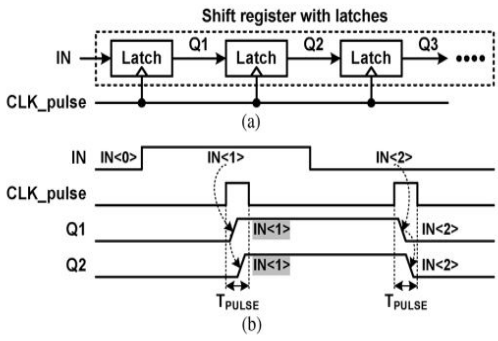


Fig. 2. Shift register with latches and a pulsed clock signal. (a) Schematic. (b) Waveforms.

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One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 3(a). The output signal of the latch is delayed (T_{DELAY}) and reaches the next latch after the clock pulse. As shown in Fig. 3(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between the latches. However, the delay circuits cause large area and power overheads.

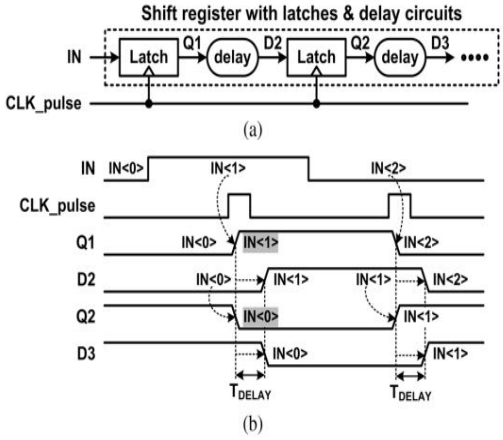

Fig. 3. Shift register with latches, delay circuits, and a pulsed clock signal. (a) Schematic. (b) Waveforms.

Another solution is to use multiple non-overlaps delayed pulsed clock signals, as shown in Fig. 4(a). The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits.

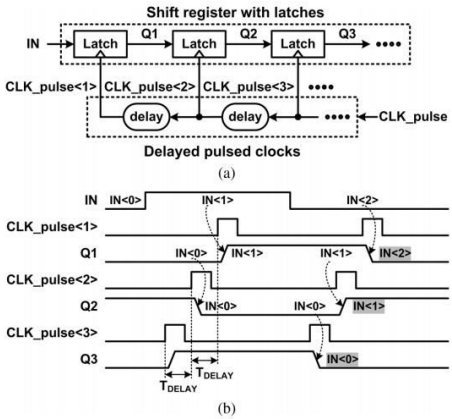

Fig. 4. Shift register with latches and delayed pulsed clock signals. (a) Schematic. (b) Waveforms.

Fig. 5 shows an example the proposed shift register. A 5-bit linear feedback shifter register consists of six latches and it performs shift operations with six non-overlap delayed pulsed clock signals (CLK_pulse<1:5> and CLK_pulse<T>). In the 5-bit lfsr, five latches store 5-bit data (Q1-Q5) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q6) of the 5-bit lfsr. Six non-overlaps delayed pulsed clock signals are generated by the delayed pulsed clock generator in Fig. 6. The sequence of the pulsed clock signals is in the opposite order of the six latches. Initially, the pulsed clock signal CLK_pulse<T> updates the latch data T1 from Q5. And then, the pulsed clock signals CLK_pulse<1:5> update the four latch data from Q5 to Q1 sequentially. The latches Q2–Q5 receive data from their previous latches Q1–Q4 but the first latch

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Q1 receives data from the input of the shift register (IN). The operations of the other sub shift registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous shift register.

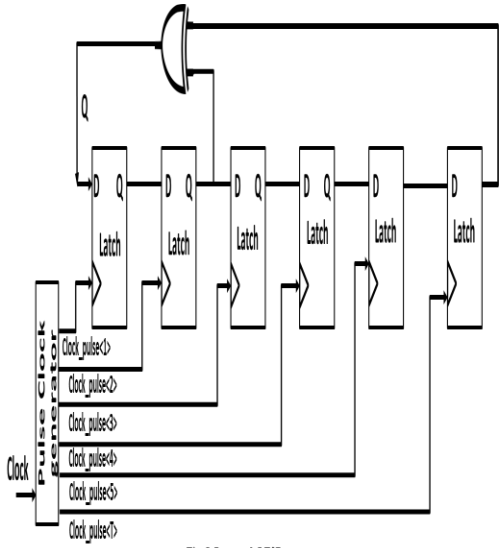

Fig.5.Proposed LFSR

The conventional delayed pulsed clock circuits in Fig. 4 can be used to save the AND gates in the delayed pulsed clock generator in Fig. 6. In the conventional delayed pulsed clock circuits, the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuits to keep the shape of the pulsed clock. However, in the delayed pulsed clock generator in Fig. 6 the clock pulsed width can be shorter than the summation of the rising and falling times because each sharp pulsed clock signal is generated from an AND gate and two delayed signals. Therefore, the delayed pulsed clock generator is suitable for short pulsed clock signals.

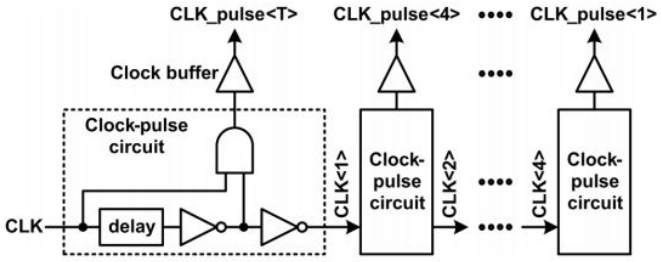

Fig. 6. Delayed pulsed clock generator.

The numbers of latches and clock-pulse circuits change according to the word length of the shift register (K). K is selected by considering the area, power consumption, speed.In a long shift register, a short clock pulse cannot through a long wire due to parasitic capacitance and resistance. At the end of the wire, the clock pulse shape is degraded because the rising and falling times of the clock pulse increase due to the wire delay. A simple solution is to increase the clock pulse width for keeping the clock pulse shape. But this decreases the maximum clock frequency. Another solution is to insert clock buffers and clock trees to send the short clock pulse with a small wire delay. But this increases the area and power overhead. Moreover, the multiple clock pulses make the more overhead for multiple clock buffers and clock trees.The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there is no delay between flip-flips. Therefore, the area and power consumption are more important than the speed for selecting the flip-flop. The proposed shift register uses latches instead of flip-flops to reduce the area and power consumption. In chip implementation, the SSASPL (static differential sense amp

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shared pulse latch) in Fig. 7, which is the smallest latch, is selected.

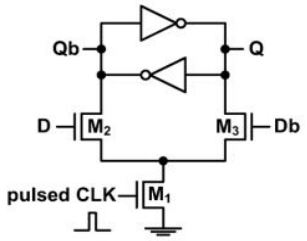
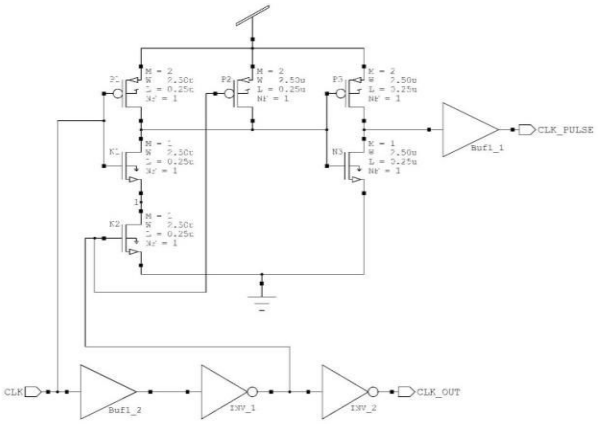


Fig. 8. Schematic of the SSASPL [6].

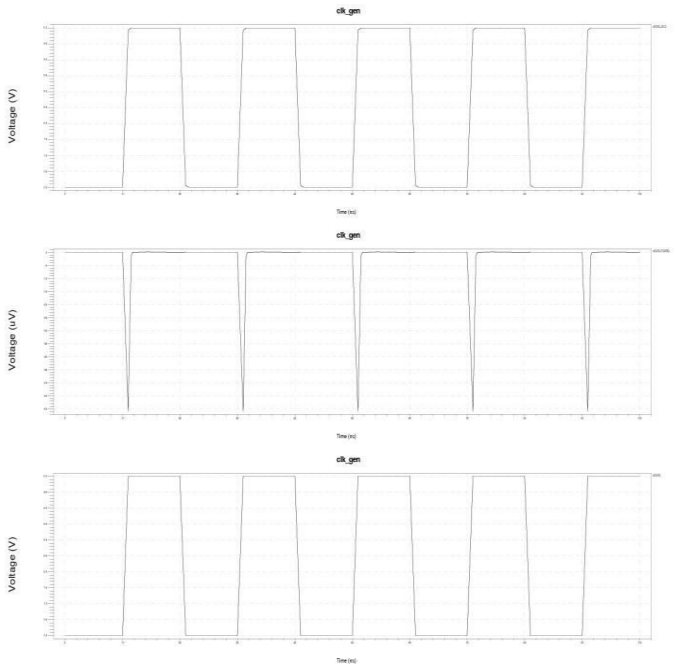
The original SSASPL with 9 transistors is modified to the SSASPL with 7 transistors in Fig. 7 by removing an inverter to generate the complementary data input (Db) from the data input (D). In the proposed shift register, the differential data inputs (D and Db) of the latch come from the differential data outputs (Q and Qb) of the previous latch. The SSASPL uses the smallest number of transistors (7 transistors) and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal.The SSASPL updates the data with three NMOS transistors (M_1-M_3) and it holds the data with four transistors in two cross-coupled inverters. It requires two differential data inputs (D and Db) and a pulsed clock signal. When the pulsed clock signal is high, its data is updated. The node Q or Qb is pulled down to ground according to the input data (D and Db). The pull-down current of the NMOS transistors (M_1-M_3) must be larger than the pull-up current of the PMOS transistors in the inverters.

IV.EXPERMENTAL RESULTS

The proposed linear feedback shift register with was fabricated using a CMOS process. In the simulations, the shift register with operates up to , but in the measurements, the clock frequency was 100 MHz due to the frequency limitation of the experimental equipment. Below Figures represents a clock signal of 100 MHz, an input signal. The schematic and output wave forms were given below. The below figures give the complete experimental results using Tanner v13.0 SPICE tool.



Schematic for single clock pulse generator



Output waveform for single clock pulse generator

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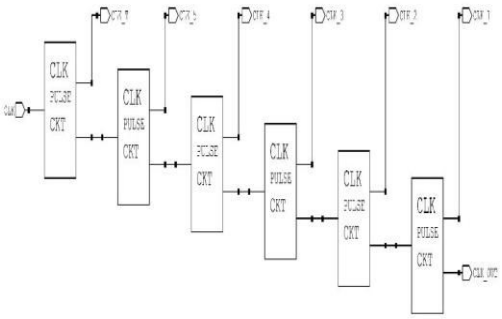
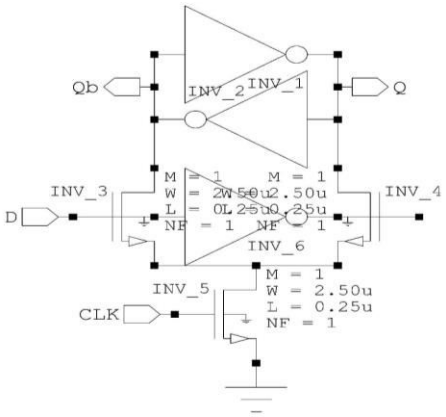
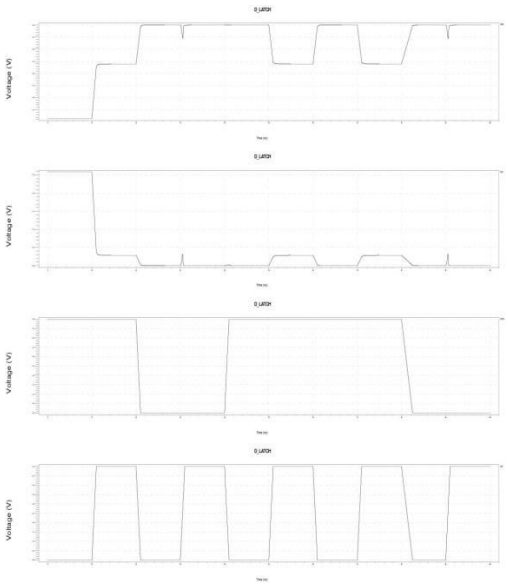


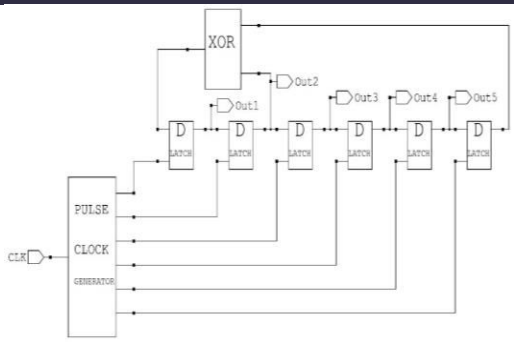
Schematic for 5-tap clock pulse generator



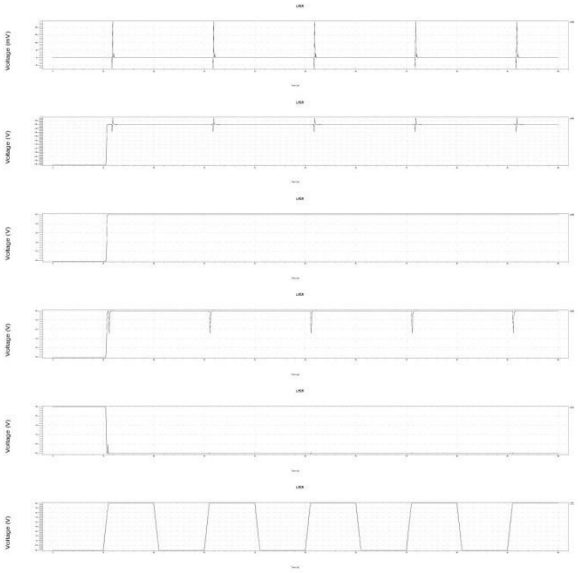
Schematic for D-Latch



Output waveform for D-Latch



Schematic for 5-tap LFSR



Output waveform for 5-tap LFSR

V.CONCLUSION

This paper proposed a low-power and area-efficient shift register using pulsed latches. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches. The proposed shift register saves 37% area and 44% power compared to

the conventional shift register with flip-flops. Thus, we see that the pulsed latches based LFSR architectures satisfy the major concern for low-power consumption in VLSI chips.

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