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A HIGH STEP-UP DC TO DC CONVERTER UNDER ALTERNATING PHASE SHIFT CONTROL FOR FUEL CELL POWER SYSTEM.

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Abstract: This paper examines a novel PWM plan for two phase interleaved help converter with voltage multiplier for power module power framework by consolidating Exchanging Stage Shift (APS) control furthermore, customary interleaving PWM control. The APS control is utilized to lessen the voltage weight on switches in light load while the customary interleaving control is utilized to keep better execution in substantial burden. The limit condition for swapping in the middle of APS and customary interleaving PWM control is inferred. Taking into account the above investigation, a full power reach control joining APS and customary interleaving control is proposed. Misfortune breakdown investigation is too given to investigate the proficiency of the converter. At long last, it is confirmed by test results.
Keywords: Boost Converter, Loss Breakdown, Fuel Cell Voltage Multiplier, Interleaved.

I. INTRODUCTION

With expanding worry about vitality and environment, it is important to investigate the renewable vitality including wind power, sun oriented, energy component, and so on. Energy unit is one of promising decisions because of its favorable circumstances of zero outflow, low commotion, higher force thickness and being effectively modularized for convenient force sources, electric vehicles, appropriated era frameworks, and so forth [1]. The network associated force framework in light of energy component is demonstrated in Fig. 1. For a run of the mill 10 kW Proton Trade Film Power device, the yield voltage is from 65 V to 107 V. In any case, the data voltage of the three stage DC/Air conditioning converter should be around 700 V, the voltage addition of the DC/DC converter between energy component and the DC/Air conditioning converter will be from 6 to 11. A high stride up DC/DC converter is required for the framework as demonstrated in Fig. 1. The DC/DC converter will produce a high recurrence info current swell, which will diminish the life time of the energy unit stack [2-4]. Also the hydrogen vitality usage diminishes with expanding the present swell of the energy component stack yield [5]. In this manner the DC/DC converter for the framework as demonstrated in Fig1 ought to have high stride up proportion with least information current swell. High stride up proportion can be accomplished by joining established support converter with exchanged inductors[6], coupled inductors[7-9], high recurrence transformer [10] or exchanged capacitor (SC) [19]. They

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can acquire high stride up proportion with high proficiency, low voltage push, and low EMI. In request to lessen yield power module stack yield current swell or the DC/DC converter info current swell, either an inactive channel [5] or dynamic channel [5] can be utilized, then again, this will expand the unpredictability of the framework. Truth be told, interleaving the DC/DC converter can decrease the data current swell of the DC/DC converter [6]. An interleaved help converter with voltage multiplier was proposed in [3, 4]. Its voltage pick up was expanded up to (M +1) times (M is the quantity of the voltage multiplier) of the established help converter with the same obligation cycle D and lower voltage stress.

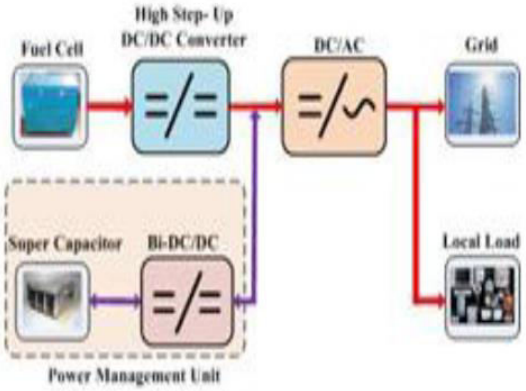

Fig. 1. Grid-connected power system based on Fuel Cell.

Other than it has lower information current swells and yield voltage swells in correlation to the traditional help converter. The interleaving help converter with voltage multipliers is demonstrated in Fig. 2. The converter indicated in Fig2 can accomplish low voltage stress in the force gadgets, which expands the transformation productivity. On the other hand, this is just valid in overwhelming burden while the voltage anxiety of the force gadgets increments when it lives up to expectations in intermittent mode (DCM) [7], which happens when power module just supplies a lightneighborhood load as demonstrated in Fig1. For thissituation, higher voltage power gadgets should be utilized,and hence its expense and force misfortune will be expanded. These creators proposed another PWM control system, named as Rotating Stage Shift (APS), to conquer the issue when the converter works in light load [7, 8].

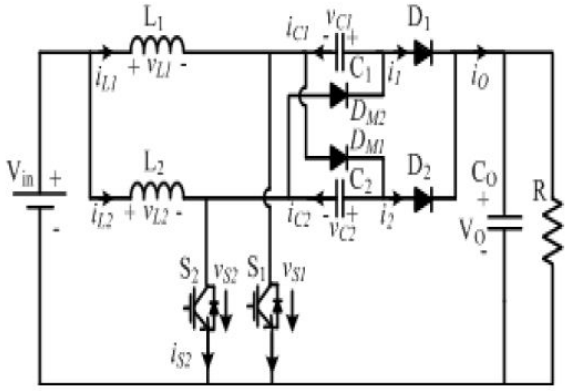

Fig2. The structure of two-phase interleaved boost converter with voltage multiplier [13, 14].

This paper explores a novel PWM plan for two phase interleaved support converter with voltage multiplier for Energy component Power Framework by joining APS and conventional interleaving PWM control. The APS control is utilized to diminish the voltage weight on switches in light load while the customary interleaving control is utilized to keep better execution in substantial burden. The limit condition for swapping between APS and customary interleaving PWM control is determined. In view of the above examination, a full power reach control consolidating APS and customary interleaving control is proposed. Misfortune breakdown examination is likewise given to investigate the proficiency

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of the converter. At long last, it is checked by test results.

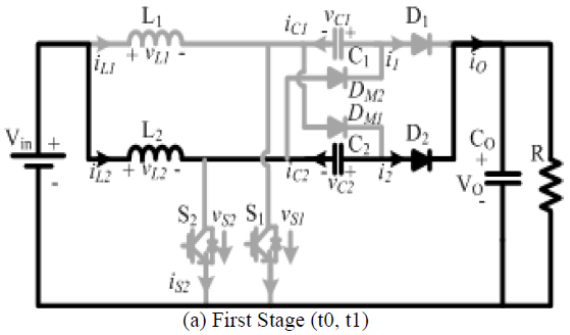
II. BOUNDARY CONDITION ANALYSIS WITH TRADITIONAL INTERLEAVING CONTROL FOR LOW POWER OPERATION

It is assumed that all components in the converter are ideal, both capacitor C1 and C2 are large enough, and duty cycle is less than 0.5. The operation of a switching cycle of the converter can be divided into six stages at boundary condition which the voltage stress on switch will be larger than half of the output voltage with traditional interleaving control, as shown in Fig. 3. Typical theoretical waveforms at boundary condition are shown in Fig. 4)

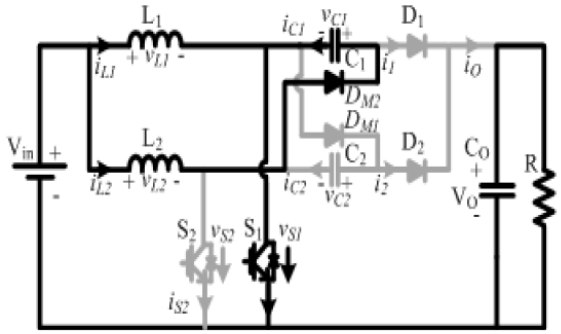
A. First Stage (t0, t1) At the moment of t0, both switch S1 and S2 are off, the energy stored in the inductor L2 and capacitor C2 in previous stage are transferred to the output capacitor CO through D2 as shown in Fig. 3(a). The voltage stress on switch S1 is the input voltage Vin, and the voltage stress on switch S2 is (VO-VC2), where VO is the output voltage and VC2 is the voltage of capacitor C2.

B. Second Stage (t1, t2)

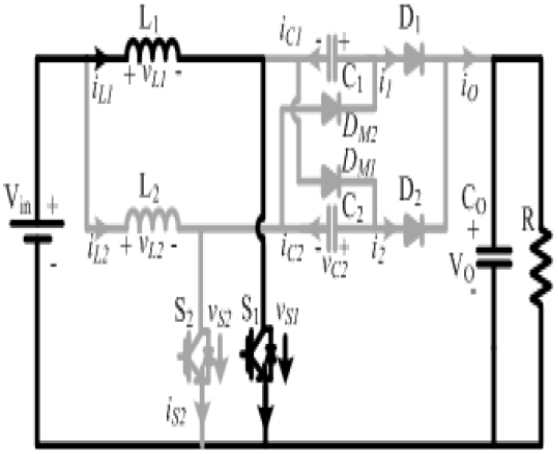
At the moment of t1, the switch S1 is turned on, the inductor L1 starts to store energy from zero as shown in Fig. 3(b). In the meantime, if (VC1+VC2)<VO, where VC1 is the capacitor C1 voltage, the diode D2 will be turned off , the diode DM2 will be turned on, therefore the energy in the inductor L2 will be transferred to the capacitor C1. If there is enough energy in the inductor L2, VC1 will be charged to the following state: VC1+ VC2_VO. Then the diode D2 will be turned on again, which is shown in Fig. 5. If there is not enough energy to charge VC1 to (VO- VC2), then it will come to Third Stage as shown in Fig. 3(c). If the energy in the inductor L2 is just discharged to zero and VC1+VC2=VO at the end of the stage, then we call the circuit operate in boundary condition state. During the stage, the voltage stress on switch S2 is VC1.



(a) First Stage (t0, t1)



(b) Second Stage (t1, t2)



(c) Third Stage (t2, t3)

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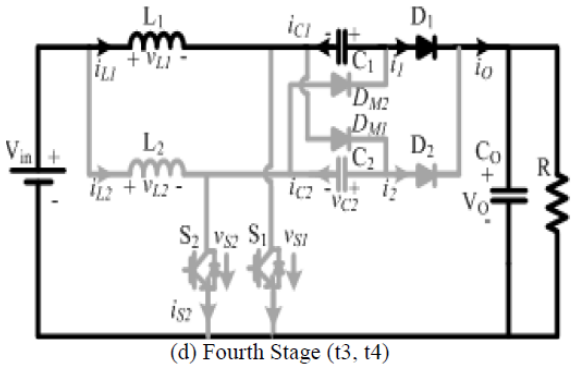
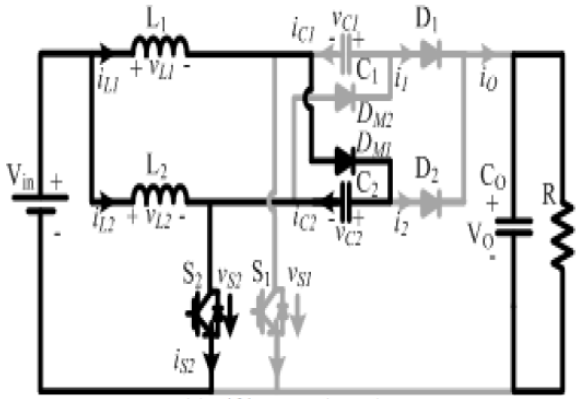
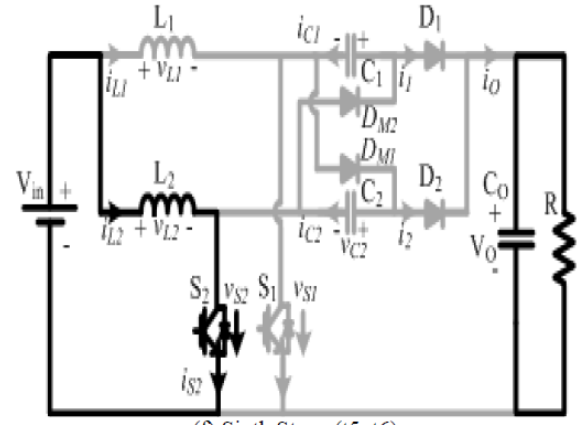


(d) Fourth Stage (t3, t4)



(e) Fifth Stage (t4, t5)



(f) Sixth Stage (t5, t6)

Fig 3. Stages at boundary condition.

C. Third Stage (t2, t3) At the moment of t2, the current in the inductor *L2* just falls to zero, all the diodes are in off state and the inductor *L1* is in charging state until the switch *S1* is turned off at the moment of t3. The voltage stress on switch *S2* is *Vin*. At the end of this stage, the current in the inductor *L1* comes to the peak value *IL1P* is

$$I_{L1P} = \frac{V_{in} D_m T_S}{L} \quad (1)$$

Where, Vin is the input voltage, L is the inductance of L1 and L2, Dm is the duty cycle at boundary condition, and TS is the switching period.

D. Fourth Stage (t3, t4)

At the moment of t3, switch S1 and S2 are in off state, the energy in the inductor L1 and the capacitor C1 will be transferred to the output capacitor CO through the diode D1, which is similar to First Stage. In this stage, the voltage stress on switch S1 is (Vo-Vc1), and the voltage stress on switch S2 is Vin. At the end of this stage, the current in the inductor L1 decreases to be IL1M,

$$I_{L1M} = I_{L1P} - \frac{V_O - V_{C1} - V_{in}}{L}(0.5 - D_m)T_S \quad (2)$$

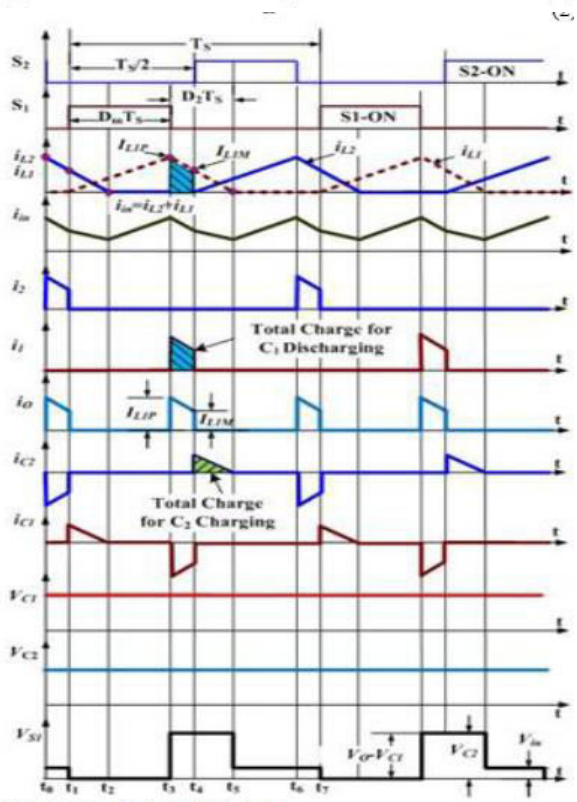


Fig 4: Theoretical Waveform.

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E. Fifth Stage (t4, t5) At the moment of t4, the switch S2 is turned on and the inductor L2 starts to store energy. This stage is similar to the Second Stage. In this stage, the voltage stress. on switch S1 is VC2. At the end of this stage, the current in the inductor L1 decreases to zero from I L1M . And thus

$$I_{L1M} - \frac{V_{C2} - V_{in}}{L}(D_2 - 0.5 + D_m)T_S = 0 \quad (3)$$

Where D is the duty cycle as shown in Fig. 4.

F. Sixth Stage (t5, t6) At the moment of t5, the current in the inductor L1 decreases to zero. All the diodes are in off state and the inductor L2 is in charging state until the stage comes to the end at the moment t6. A new switching period will begin with the next First Stage. From the above analysis, the voltage sum of capacitor C1and C2 will be VO at boundary condition. If it is less than VO, the voltage stress on switch S1 and S2 will be larger than VO/2, because the voltage stress on switch S1 is (VO-VC1) during fourth Stage and the voltage stress on switch S2 is (VO-VC2) during First Stage. The average value of the output current iO is equal to the DC component of the load current VO/R, then

$$\frac{V_O}{R} = \frac{1}{T_S}\int_0^{T_S} i_O dt = \frac{1}{T_S}\int_0^{T_S}(i_1 + i_2)dt = \frac{1}{T_S}\int_0^{T_S} i_1 dt + \frac{1}{T_S}\int_0^{T_S} i_2 dt \quad (4)$$

Considering the same parameters of the circuit in two phases as shown in Fig. 2, therefore

$$\frac{1}{T_S}\int_0^{T_S} i_1 dt = \frac{1}{T_S}\int_0^{T_S} i_2 dt \quad (5)$$

By combining equation (4) and (5), it is derived

$$\frac{V_O}{R} = \frac{2}{T_S}\int_0^{T_S} i_1 dt = \frac{2}{T_S}\int_{t_3}^{t_4} i_1 dt = \frac{2}{T_S}\cdot\left[\frac{1}{2}(I_{L1P} + I_{L1M})(0.5 - D_m)T_S\right] = (I_{L1P} + I_{L1M})(0.5 - D_m) \quad (6)$$

Where, R is the load. At boundary condition, the diode D2 (D1) approaches the conduction state during Second Stage (Fifth Stage), which is shown in Fig. 5.

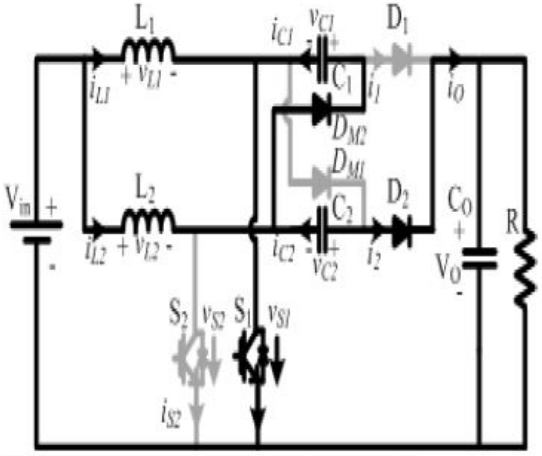

Fig. 5. One stage above boundary condition.

The following equation can be obtained

$$V_{C1} + V_{C2} = V_O \quad (7)$$

Considering both capacitor C1 and C2 are large enough, average voltage of the capacitor will keep equal. Otherwise, the converter will not operate at boundary condition, therefore

$$V_{C1} = V_{C2} = \frac{1}{2}V_O \quad (8)$$

By substituting equation (1) and (8) into equation (2), the current IL1M can be derived.

$$I_{L1M} = \frac{V_{in} - V_O/2 + V_O \cdot D_m}{2L}T_S \quad (9)$$

As shown in Fig. 4, the total discharge of capacitor C1 between t3 and t4 is

$$Q_{C1} = \int_{t_3}^{t_4} i_{L1} dt = \frac{1}{2}(I_{L1P} + I_{L1M})(0.5 - D_m)T_S \quad (10)$$

The total charge of capacitor C2 between t4 and t5 is

$$Q_{C2} = \int_{t_4}^{t_5} i_{L1} dt = \frac{1}{2} I_{L1M}(D_2 - 0.5 + D_m)T_S \quad (11)$$

According to the previous analysis, the total is charge of C1 is equal to the total charge of capacitor C2 at boundary condition. Therefore, there will be

$$Q_{c1} = Q_{c2} \quad (12)$$

By combining equation (10), (11) and (12), the following can be derived

$$D_2 = (0.5 - D_m)\left(\frac{I_{L1P}}{I_{L1M}} + 2\right) \quad (13)$$

By combining equation (3) and (6) and then substituting equation (1), (9) and (13) into them, the boundary condition can be derived as

$$\begin{cases} K = Kcrit = \dfrac{n-2}{2n(n-\sqrt{2})^2} & (a) \\ D_m = \dfrac{n-2}{2(n-\sqrt{2})} & (b) \end{cases} \quad (14)$$

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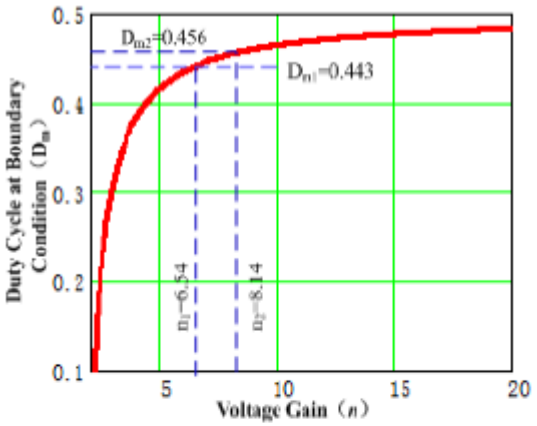
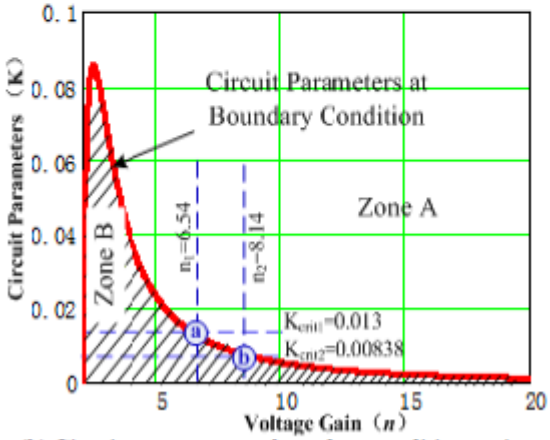
Where, n is the voltage gain of the converter, n = (Vo/Vin). K is the parameters of the circuit and 2 /( ) S K = L R ×T . The boundary constraint with traditional interleaving control decided by equation (14) is shown in Fig. 6. The constraint includes two parts: duty cycle D and the circuit parameters 2 /( ) S K = L R ×T. As the switching period TS and the input inductor L are designed at nominal operation in Continuous Conduction Mode (CCM), the constraint is determined by duty cycle D and the load R. The reason why there are two parts in the boundary constraint is that the duty cycle D varies with the load when the converter operates in Discontinuous Conduction Mode (DCM). For a given application, the voltage gain of the DC/DC converter is determined. And then the minimum duty cycle that can maintain low voltage stress in main power devices with traditional interleaving control will be given by equation (14)-(b) and as shown in Fig. 6(a). At the same minimum duty cycle, the converter operates at boundary condition when the circuit parameters 2 /( ) S K = L R ×T satisfy equation (14)-(a) and as shown in Fig. 6(b). When the converter operates above boundary condition, the circuit parameters are in Zone A of Fig. 6(b), i.e. K>Kcrit, the converter could achieve halved voltage stress on switches with traditional interleaving control with the duty cycle above the solid red line as shown in Fig. 6(a). When decreasing the load to the solid red line at boundary condition in Fig. 6(b), i.e. K= Kcrit, the duty cycle of the converter will be decreased to the solid red line in Fig. 6(a). When decreasing the load further in Zone B in Fig. 6(b), i.e. K<Kcrit, the duty cycle will be decreased further to be smaller than the minimum duty cycle that maintains low voltage stress on switches with traditional interleaving control. Then the APS control should be used to achieve halved voltage stress on switches in Zone B [17, 18]. In our 1 kW prototype design, the input voltage of the converter is 86-107 V, and the output voltage of the converter is 700 V.



(a) Duty cycle at boundary condition varies with voltage



(b) Circuit parameters at boundary condition varies with voltage Gain

Fig. 6. Boundary constraint varies with voltage gain.

The voltage gain will vary from n1=6.54 to n2=8.14, and then the circuit parameters at boundary conditions Kcrit will vary from Kcrit1=0.013 to Kcrit2=0.00838 as shown in

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Fig. 6(b), the duty cycle will vary from Dm1=0.443 to Dm2=0.456 in order to maintain the stable output voltage. When the circuit parameters 2 /( ) S K = L R ×T are below the solid red line from point ○a to point ○b at different voltage gain as shown in Fig. 6(b), the duty cycle will be decreased further to be less than the solid red line from Dm1=0.443 to Dm2=0.456 as shown in Fig. 6(a), and then the voltage stress on switches will be increased at this load. In order to achieve the halved voltage stress on switches at this load, APS control is needed.

III. CONTROL SCHEME OF ALL POWER RANGE WITH APS AND TRADITIONAL INTERLEAVING CONTROL

According to the principle of APS [25], APS control is proposed to solve the light load problem with duty cycle less than 0.5 as shown in Fig. 7(a). With the load increasing, the duty cycle will be increased as well. When the duty cycle is increased to 0.5, the APS control will be altered to be traditional interleaving control with halved switching frequency as shown in Fig. 7(b). According to previous analysis as shown in Fig. 6, the minimum duty cycle to achieve low voltage stress on switches with traditional interleaving control is less than 0.5. Therefore, it is possible to combine both APS control and traditional interleaving control to control the converter for full power range operation.

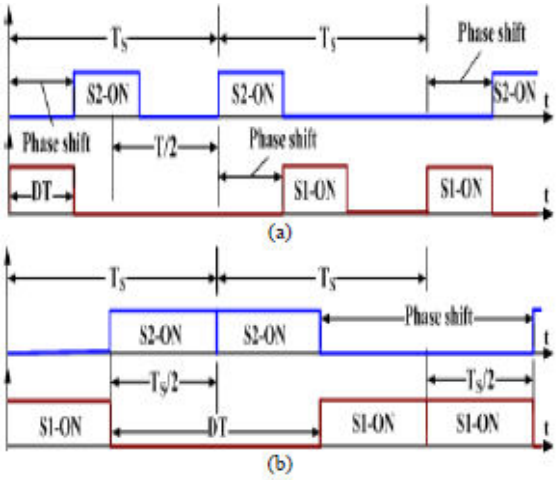

Fig.7. PWM waveform of APS with (a) D<0.5 and (b) D=0.5

Considering the variation of the input voltage from 86 V to 107 V for 1 kW fuel cell operation and the output voltage of the converter 700 V, the minimum duty cycle of traditional interleaving control varies from Dm1=0.443 to Dm2=0.456. The control scheme is shown in Fig. 8. The duty cycle is divided into three areas: D<Dm1, D>Dm2 and Dm1≤D≤Dm2. In the first area, i.e. D<Dm1, APS control will be used because traditional. interleaving control cannot be effective to maintain low voltage stress on switches. In the second area, i.e. D>Dm2, traditional interleaving control will be used. In the third area, i.e. Dm1≤D≤Dm2, either APS control or traditional interleaving control may be used. In the first area (D<Dm1) with APS control and the second area (D>Dm2) with traditional interleaving control, the capacitor voltage is half of the output voltage. Therefore the switches voltage stress is clamped to half of the output voltage [17, 18]. The swapping between APS control and traditional interleaving control in the area Dm1≤D≤Dm2 is achieved by detecting the voltage stress of the switch S1 as shown in

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Fig. 8. When the voltage stress of the switch S1 is higher than half of the output voltage, the control is changed from interleaving control to APS control. If the traditional control is initially used in the second area ($Dm1 \le D \le Dm2$) and once the switch S1 voltage stress is larger than half of the output voltage, the logic unit output CMP in Fig. 8 will be changed to CMP=1 and APS control will be enabled.

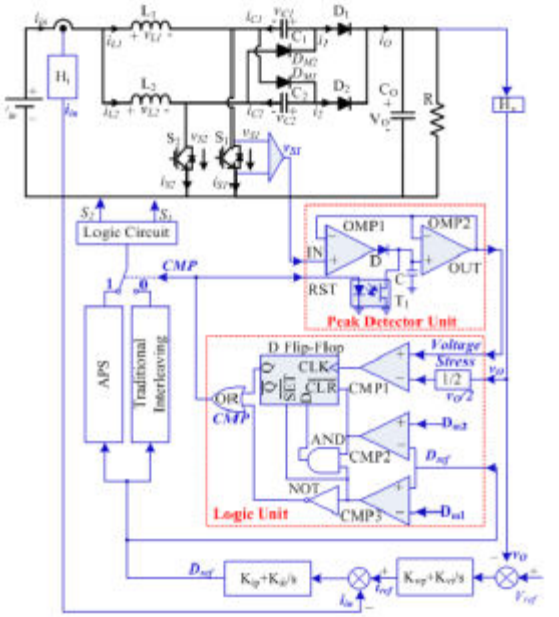

Fig8. Block diagram of the converter with the control scheme of all power range.

TABLE I: OPERATIONAL PRINCIPLE THE LOGIC UNIT IN FIG.9

$v_{S1}>0.5v_O$	$D_{ref}\ge D_{m1}$	$D_{ref}<D_{m2}$	Control Method
X	1	0	Traditional interleaving control
X	0	1	APS control
0	1	1	Keep the previous control mode
1	1	1	Swap from traditional interleaving control to APS control and stay in APS control until $D_{ref}\ge D_{m2}$

The above function for swapping between APS and traditional interleaving control is achieved by the Logic Unit as shown in Fig. 8. If APS control mode is used (i.e. CMP=1), the opt coupler transistor T1 is turned on, the voltage of capacitor C in the peak detector unit is resetted and the peak detector unit is disenabled. If the traditional interleaving control mode is used (i.e. CMP=0), the optocoupler transistor T1 will be turned off, and the peak detector unit is enabled and used to detect the voltage stress of switch S1. In order to achieve better dynamic performance operation, dual loop control is adopted as shown in Fig. 8, which inner current loop is to control the input inductor current while the outer voltage loop is to control the output voltage. Kip and Kii are the PI controller parameters of the inner current loop, while Kvp and Kvi are the PI controller parameters of the outer voltage loop. In our 1 kW prototype design, the circuit parameters are as follows, Vin=100 V, VO=700 V, C1=C2=40 μF, CO=195 μF, L1=L2=1158 μH, TS=100 μs, Hv=65.536, Hi=698.298, where Hv is the voltage feedback coefficient and Hi is the input current feedback coefficient. The bandwidth of the inner current loop is 1 kHz with PI parameters as follows: Kip=0.061, Kii=63.67. The bandwidth of the outer voltage loop is 100 Hz with PI parameters as follows: Kvp=4.25 Kvi=267.036.

IV. LOSS BREAKDOWN ANALYSIS

As the cost of fuel cell is still very high, it is important to maximize the efficiency of the power converter for fuel cell based power system in order to reduce its operation cost and increase the utilization of fuels.

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Therefore, loss breakdown analysis is needed. The nominal power of the converter is 1 kW for loss breakdown analysis and prototype setup, and the input voltage is 100V while the output voltage is 700 V with switching frequency fS=10 kHz. The power devices used are shown in Tab. II.

TABLE II: MAIN CHOICES OF POWER DEVICES

Symbol	Voltage Stress	Product Type
S_1,S_2	350V	IKW20N60H3
D_1,D_2	350V	DSEP15-06A IDW16G65C5
DM1,DM2	700V	DSEP15-12CR IDH15S120

The converter could operate in Continuous Conduction Mode (CCM) at nominal load with input current ripple ratio r= 0.37 and the inductor L1 and L2 is 1158µH. The inductor is built with the amorphous core. As shown in Fig. 9, the main parts of the loss are the conduction loss (Pcon_S) and switching loss of the IGBT. With the fast recovery diodes. (DSEP1512CR and DSEP1506A) and IGBT (IKW20N60NH3), the efficiency of the converter at nominal load can be 97.49%. As there is no reverse recovery loss (Prr_D) in Silicon Carbide (SiC) diode, the efficiency can be increased to be 97.86% with SiC diode (IDH15S120 and IDW16C65C5) and IGBT (IKW20N60NH3). The converter could also operate in Boundary Conduction Mode (BCM) at nominal load with input current ripple ratio (r= 0.6) and the inductor L1 and L2 is 714.3 µH. The inductor is built with the amorphous core. As shown in Fig. 10, the main parts of the loss are also the conduction loss (Pcon_S) and switching loss (PSW_S) of the IGBT. Compared with CCM as shown in Fig. 9, there is no fast recovery loss even with fast recovery diodes in BCM. However, the inductor loss including the core loss(P_Fe) and the wire loss (P_Cu) is increased in BCM as the current ripple is increased from 0.37 to 0.6. In BCM, the efficiency of the converter can be 97.09% with SiC diode and 97.06% with fast recovery diode. Comparing Fig. 9 and Fig. 10, the efficiency of the converter with IGBT and fast recovery diode in CCM is a bit higher than that in BCM. In CCM, the efficiency of the converter with fast recovery diode is only 0.37% less than that with SiC diode. Therefore, we use IGBT and fast recovery diode in CCM for experiments.

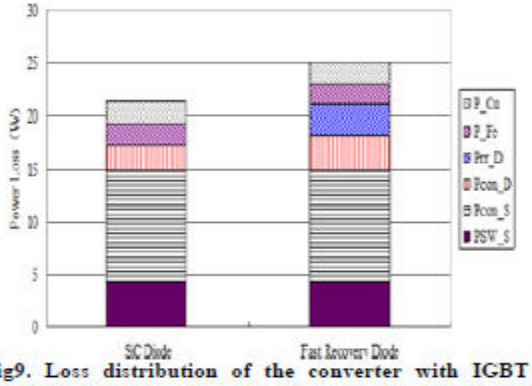

Fig9. Loss distribution of the converter with IGBT (IKW20N60NH3) in CCM (r=0.37) at 1 Kw (SiC Diode: IDH15S120 and IDW16G65C5 Fast Recovery Diode: DSEP1512CR and DSEP1506A).

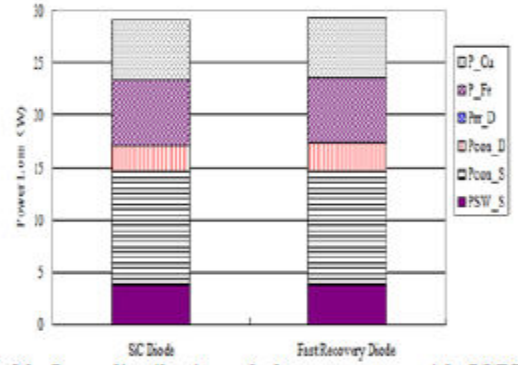

Fig10. Loss distribution of the converter with IGBT (IKW20N60NH3) in BCM (r=0.6) at 1 Kw (SiC Diode: IDH15S120 and IDW16G65C5 Fast Recovery Diode: DSEP1512CR and DSEP1506A)

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V. SIMULATION RESULTS

A. Static Experiments

In order to verify the previous analysis, prototype is built as shown in Fig. 11. The circuit parameters are as follows, Vin=100 V, VO=700 V, C1=C2=40 μF, CO= 195 μF, L1=L2=1158 μH, TS=100 μs. The load at boundary condition is RBC=2032 Ω and Kcrit=0.011 at boundary condition according to equation (14), the duty cycle Dm at boundary condition is 0.448, Fig.11.

Fig. 11. Prototype of the 1 kW Converter with Fuel Cell and Load.

The simulation results at boundary condition are shown in Fig.12 which are in accordance with the theoretical waveform in Fig. 4. The simulation results are given to verify the previous analysis. With R=478 Ω, the output power is a bit greater than 1 kW, and =0.049>Kcrit=0.013, the converter is design to operate in Zone and the traditional interleaving control can maintain the voltage stress on switches with half of the output voltage (i.e. 350V) as With R=1658 Ω, i.e. K=0.014>Kcrit=0.013, the converter will continue operating in Zone and the voltage stress on switches is still 350 V, which is about the half of the output voltage However, when decreasing the load to be 3460 Ω, i. e. K=0.0067<Kcrit, the converter will operate in Zone B of Here for comparison, two control methods are used and the results are respectively. In the traditional interleaving control is used, and we can see the voltage stress on the switch is 452 V which is higher than half of the output voltage. In Fig. 16, APS control is used, and we can see the voltage stress on the switch is 350 V which is about half of the output voltage. Therefore it is effective to use APS control when the converter operates in Zone B. With the control scheme as shown in Fig. 8, more experiments are conducted to measure the voltage stress on Power switches in all power range of the load. The voltage stress follows the variation of the output voltage, and almost keeps half of the output voltage in all power range. The reason why the output voltage is not stable comes from the voltage ripple of 20V in the output voltage. As the current ripple through capacitors C1 and C2 has bad effect on their lifetime and reliability, it is important to test whether the maximum current ripple is increased when utilizing APS control. Considering the symmetry of the converter, we only test the current through C1. As shown in Fig. 18, the peak current through capacitor C1 is 3.29 A with traditional interleaving control under the load R=3460 Ω, and the RMS of the current through capacitor C1 is 0.623 A. With APS control, the current ripple is not increased but reduced to be 3.21 A under the same load as shown in Fig. 19, and the RMS of the current through capacitor C1 is reduced to be 0.538 A. More experiments are conducted under different load as shown in Fig. 20, the current ripple with APS control is less than that with traditional interleaving

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control. Therefore, the proposed APS control can increase the lifetime and reliability of capacitors C1 and C2.The C1 and C2 are designed with film capacitor with the part number is SHB-500-40-4 from EACO Capacitor, Inc., and its maximum RMS current is 19 A, which is much greater than the above current ripple.

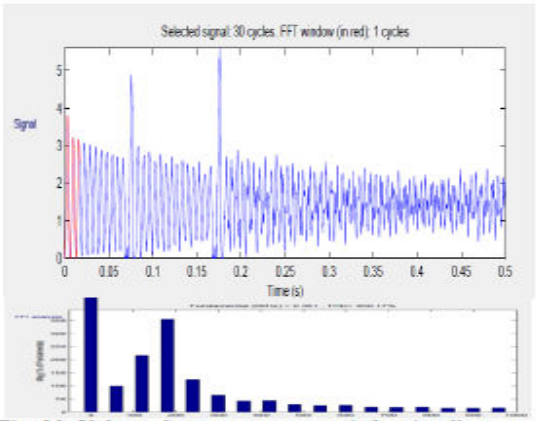
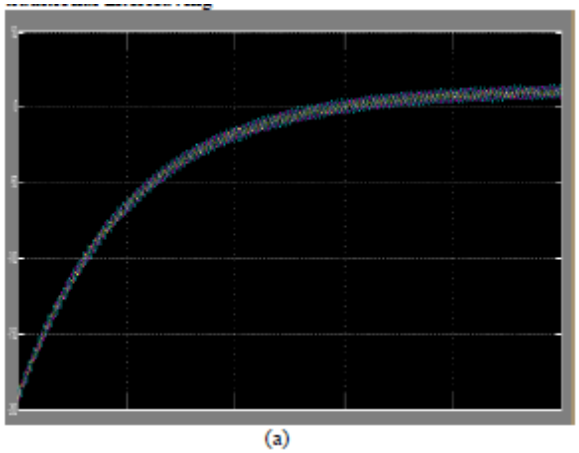
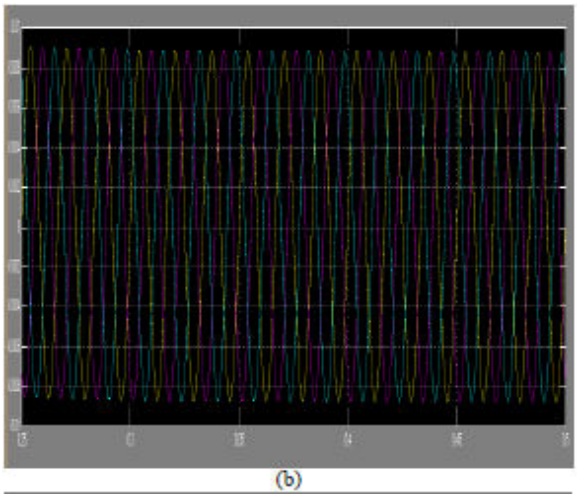


Fig. 12. Voltage Stress on power switches in all power range of the load.

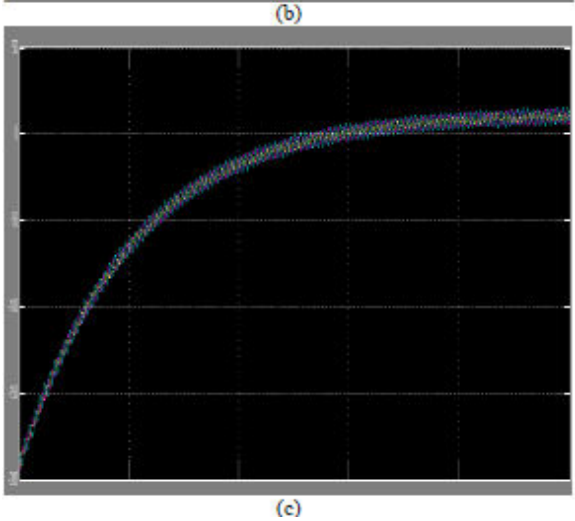
B. Dynamic Experiments In order to test the dynamic performance of the converter with fuel cell as input, the converter is connected to the output of the PEMFC shown in Fig. 11. When the load varies from 3478 _ to 1658 Ω as shown in Fig. 21, the output voltage of the fuel cell will varies from 99.1V to 93.7V, the control scheme will swap from APS control to traditional interleaving



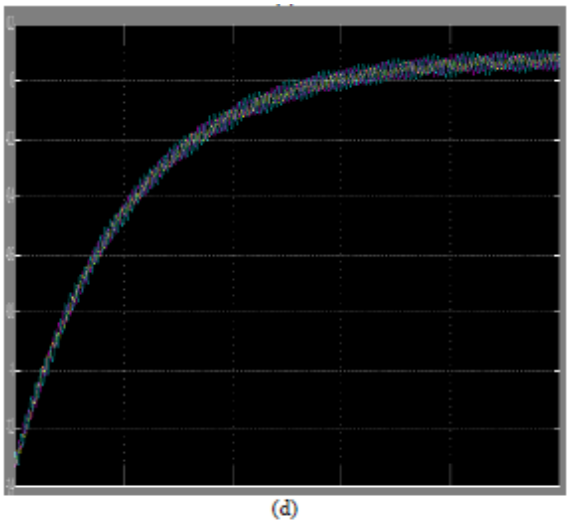
(a)



(b)



(c)



(d)

Fig 13: Efficiency Comparison of the Converter with Two Control Method.

during the period of load variation, and the voltage stress of power switches keeps half of the output voltage. When the load varies

from 1658 Ω to 3478 Ω as shown in Fig. 22, the output voltage of the fuel cell will varies from 93.7 V to 99.1 V accordingly; the control scheme will swap from traditional interleaving control to APS control, and the voltage stress of power switches keeps half of the output voltage as well. Therefore, the control scheme proposed in this paper could achieve halved voltage stress on switches when swapping between traditional interleaving control and APS control.

VI. CONCLUSION

The boundary condition is derived after stage analysis in this paper. The boundary condition classifies the operating States into two zones, i.e. Zone A and Zone B. In Zone A, the traditional interleaving control is used while APS control is used in Zone B. And the swapping function is achieved by a logic unit. With the proposed control scheme, the converter can achieve low voltage stress on switches in all power range of the load, which is verified by experimental results.

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