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LOW POWER AREA EFFICIENT ALU WITH LOW POWER FULL ADDER

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***Abstract*— In this paper implemented a low Power Area efficient ALU using XNOR logic. The 4bit ALU design. ALU is an Arithmetic and Logic Unit, which performs arithmetic operation like ADD, SUB, PASS THROUGH, TWO'S COMPLEMENT, etc. and logic operation like AND, OR, EXCLUSIVE OR, EXCLUSIVE NOR, etc. Full adder is the basic component for an ALU. By reducing the power of full adder, the ALU power also be reduced. Compared with Gate Diffusion Input Full Adder, 50% power reduced in the XNOR based Full Adder Technique. The simulation is carried out using Microwind DSCH3.**

I. INTRODUCTION

In the era of growing technology and scaling of devices up to nanometer regime, the arithmetic logic circuits are to be designed with compact size, less power and propagation delay. Arithmetic operations are indispensable and basic functions for any high speed low power application digital signal processing, microprocessors, image processing etc. Addition is most important part of the arithmetic unit rather approximately all other arithmetic operation includes addition[7]. Thus, the primary issue in the design of any arithmetic logic unit is to have low power high performance adder cell. Power has become one of the major important issues in the VLSI circuits. As the complexity increases and number of transistors in a chip increase, one has to consider the power dissipation. Higher power dissipation, increases the temperature and hence increases the chip temperature. As power dissipation goes on increasing, the battery life, reliability, cooling system and cost are affected [8]. Hence as a designer it is important to design circuits to consume less power by avoiding unwanted switching actions [9].

The majority of the power dissipation is due to dynamic power dissipation. That is due to switching action of the node and internal node capacitance of the circuit [10]. Other sources of power dissipation are static current and short circuit current. Static power dissipation is basically due to the reverse current and sub threshold current when the transistor is off [11]. Compared to dynamic power dissipation, static power is less around (20% - 50%) but increases as complexity increases. Short circuit current is due to non-zero rise time and fall time and is around (5% - 10%). Many techniques are used to reduce the leakage current and hence to reduce the static power dissipation such as power gating, multiple Vt, etc. There are many techniques involved to reduce the dynamic power dissipation by reducing the switching action such as Block enabling, Pre computation technique, etc... Clock gating technique is used to reduce the clock power. The dynamic power dissipation is around (40%-70%) and is relatively reducing with today's technology. An Arithmetic and Logic Unit (ALU) is a digital circuit that performs arithmetic and logic operations. The ALU is a fundamental building block of the central processing unit of a computer [12]. The power consumed by the ALU has a direct impact in the power dissipated from the processor. Hence, a design is required to implement the ALU in a fashion where the performance of the processor is improved and also the power consumed is less [13]. To be precise Power consumption of whole data path can be reduced by reducing power consumption of ALU. Adder is the basic building block for an ALU. To reduce the power consumption from ALU first we need to reduce through full adder. ALU (Arithmetic Logic Unit)

The heart of every computer is an Arithmetic Logic Unit (ALU). This is the part of the computer which performs

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arithmetic operations on numbers, e.g. addition, subtraction, etc. In this lab you will use the Verilog language to implement an ALU having 10 functions. Use of the case structure will make this job easy[14]. The ALU Design and Operation A 4 - bit ALU has been designed for 3.0 V operation in which, the full adder design has been implemented using MIFG CMOS inverters. The ALU has four stages, each stage consisting of three parts: a) input multiplexers b) full adder and c) output multiplexers. The ALU performs the following four arithmetic operations, ADD, and SUBTRACT INCREMENT and DECREMENT. The four logical operations performed are EXOR, EXNOR, AND and OR. The input and output sections consist of 4 to 1 and 2 to 1 multiplexers. The multiplexers were designed using the pass transistor logic. A set of three select signals has been incorporated in the design to determine the operation being performed the inputs and outputs being selected [15].

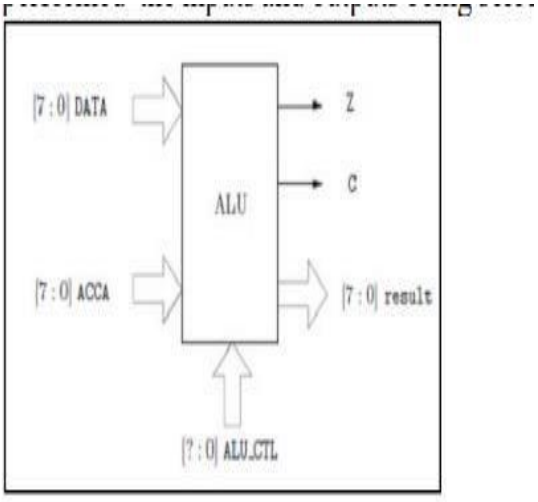

Fig 1: ALU Block Diagram

DESIGN OF ALU USING LOW POWER FULL ADDER

An arithmetic and logic unit is a fundamental block for many processors. It performs many processors [16]. It performs many operations like addition, subtraction, XOR, XNOR, buffer, NAND, OR etc. The 4 bit ALU operation can be implemented using eight 4x1 multiplexer, four full adder, four 2x1 multiplexer [17]. Depends upon the three selection line s2, s1, s0, the arithmetic and logic operation can be performed. The block of 4x1 multiplexer consists of four inputs, which is logic 0, logic 1, B and B'. Depends upon the s0 and s1 selection line; the desired output can be generated. These outputs[18]. The next stage of 4x1 multiplexer has the input of full adder sum, which is EXOR, EXNOR, AND, and OR. Depends on the s0 and s1 selection lines, the output can be generated. It acts as an input for the 2x1 multiplexer. Another input of 2x1 multiplexer is the full adder sum output. Finally, the output stage of 2x1 multiplexer can be generated by using s2 selection line.

Table: Operations of ALU

S2	S1	S0	OPERATIONS
0	0	0	Buffer
0	0	1	EXOR
0	1	0	EXNOR
0	1	1	OR
1	0	0	ADDITION
1	0	1	SUBTRACTION
1	1	0	BITWISE NAND
1	1	1	Inverter

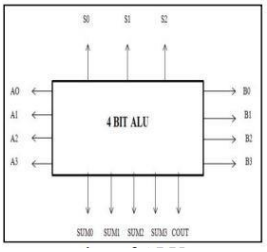

Fig.2: Logo representation of ALU

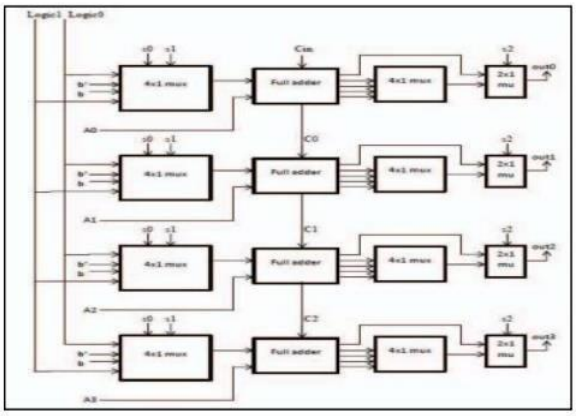

Fig 3: Process of 4bit arithmetic and logic unit

Multiplexer logic at the input stage consists of 4x1 multiplexer and 2x1 multiplexer. Depends upon the selection line of s0, s1 and s2, the output of full adder has been computed. Multiplexer logic at the output stage consists of 4x1 multiplexer and 2x1 multiplexer. Depends upon the selection line of s0, s1, and s2, the output of ALU has been computed. Input stage multiplexer consists of VDD, VSS, B and B'. The output stage multiplexer consists of EXOR, EXNOR, AND and OR input. Fig.8 shows input stage of multiplexer architecture and fig9 shows output stage of multiplexer architecture.

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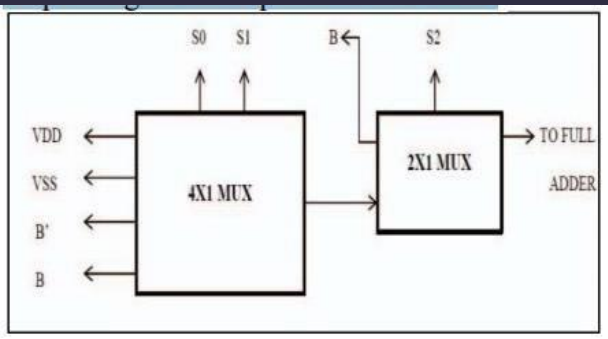


Fig 4: Architecture of multiplexer logic at the input stage

This paper presents a new technique of XNOR logic, to design the full adder is resolved by gate diffusion input technique which proven to have high power consumption and compared with XNOR logic. These new approach of XNOR logic gives excellent result then previous design in charge of power consumption, area as well as propagation delay.

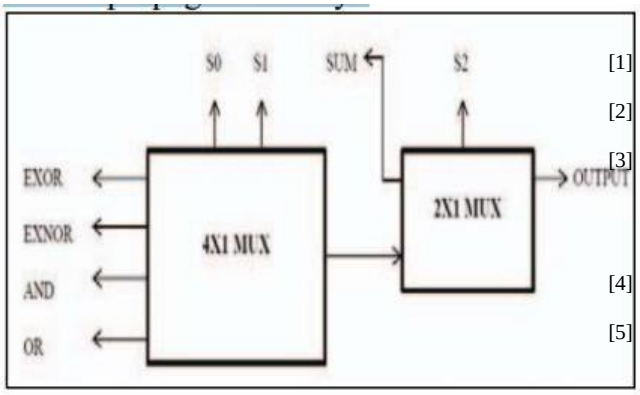
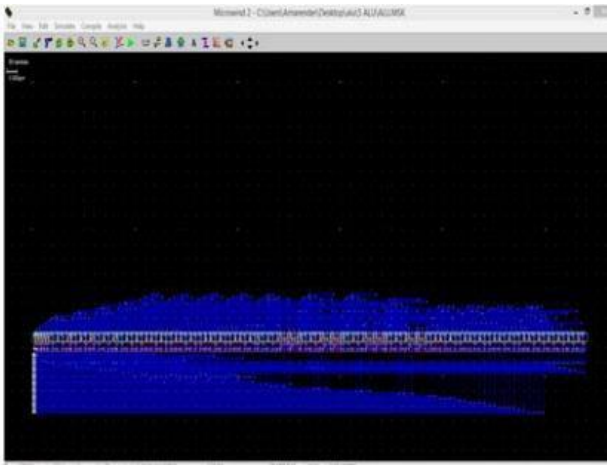
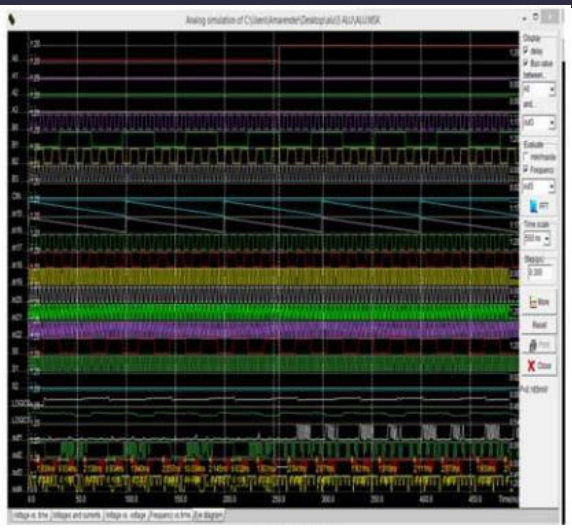


Fig.5: Architecture of multiplexer logic at the output stage

LAYOUT DESIGN LAYOUT DESIGN FOR ALU



SIMULATION RESULTS



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