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Paper Authors **Dr.K.Ranjith Kumar1 , Mr.Nagaraju Budidha2, Mr.K.Prakash Chary3**

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SIMULATION OF DUAL-T-TYPE CASCADED MULTILEVEL INVERTER WITH REDUCED COMPONENTS

Dr.K.Ranjith Kumar[1] , Mr.Nagaraju Budidha[2], Mr.K.Prakash Chary[3]
[1, 2 & 3] Asst. Professor in EEE Dept., Vaagdevi College of Engineering

ABSTRACT
This paper introduces a new Dual –-T-Type cascaded multilevel inverter with reduced components. The Dual –-T-Type CHB inverter is having more importance in power electronics application due to reduction in switching losses to other type of inverter. This inverter is adopted with level shifted carrier PWM (LSCPWM) technique. This MLI addresses two major drawbacks associated with the conventional and other recently proposed MLIs which are the high voltage stress of switches and higher power component counts. The proposed DTT-5L-CMI is capable of five levels generation with double voltage boosting gain. Overall this design can be modelled in MATLAB/Simulink software.

Index Terms — Cascaded multilevel inverter, dual-T-type topology, soft charging, switched-capacitor, voltage boosting.

1. Introduction

Multilevel inverters (MLIs) had been developed as one of the most cost-effective power electronic devices having an extensive variety of applications. These devices had been a center of consciousness for researchers currently seeing that they own various interesting features. These capabilities consist of excessive excellent output voltage, better performance, and small voltage strain on switches. MLIs have contributed notably within the area of electricity device with the aid of their huge range of applications [1–4]. They can be included with photovoltaic (PV) grid systems, can be carried out in wind farms and excessive voltage direct present day (HVDC) systems. MLIs are designed using unique association of electricity electric powered gadgets along with integrated gate bipolar transistor (IGBT) switches and DC substances to generate high voltage outputs. MLIs are traditionally categorized into three fundamental classes [5]: Neutral Point Clamped (NPC), Flying Capacitor (FC) and Cascaded H-bridge (CHB). NPC inverter become first introduced in 1981 and it was a three-degree inverter [6]. FC inverter become first proposed in 1992 and it changed into constructed using independent capacitors [7]. The essential idea of developing CHB inverters with several DC supplies turned into first proposed in 1998 [8]. The blessings and disadvantages of MLIs rely upon numerous elements. These factors consist of: wide variety of switches, DC elements, diodes, capacitors and voltage degrees, alongside fine of voltage, maximum voltage, switching stress, switching frequency, and total voltage stress (TVS). The classical MLI topologies have a few key obstacles based on these factors. Some commonplace boundaries of NPC MLI can be listed as follows: loss of modularity, necessity of high amount of clamping diodes, unequal electricity distribution, choppy usage of switches and unbalanced voltages. The key obstacles in FC MLIs are balancing the fees of capacitors at low switching frequency and requirement of too many clamping capacitors. Similarly, CHB MLIs have positive barriers which includes requirement of remote DC-deliver for every H-bridge module which could increase the general price of these topologies substantially [9]. These obstacles have advocated researchers to design new topologies of MLIs which can mitigate the troubles of classical inverters. T-type MLI became originally proposed by using [10] to cope with the drawbacks of NPC MLI. This MLI became an advanced amendment of popular NPC inverters and possessed some advantages which include lesser range of energy components and high efficiency as compared to NPC. The principal cause of designing this MLI turned into to lower the voltage pressure on semiconductor switches. The development of this MLI from NPC, alongside different current adjustments, are in brief studied in [11]. In 2013, following the fundamental of every other classical inverter (CHB), Babaei got here up with the idea of a crossed switched MLI [12]. This generalized topology became capable of inherit most of the blessings of the CHB inverters and reduced the full electricity digital additives extensively. The simplest drawback of this MLI changed into the excessive TVS of the cross connected switches. However, the invention of these inverters turned into now not sufficient to fulfill the researchers. To reach even higher stages of voltage output, researchers got here up with the idea of designing asymmetrical MLIs. These MLI topologies use DC sources of unequal magnitudes. Based on this idea, a few MLI

modules with decreased amount of switches are supplied in [13–15]. One of the most important hazards of asymmetrical MLIs is the excessive voltage pressure on the switches which can be related with excessive value DC assets. Therefore, those designs are normally avoided wherein unbalanced voltage output can motive severe results. All of these MLI topologies are capable of huge scale of packages. These inverters were to start with designed to feature as it should be in medium voltage (2.3 kV, three.3 kV, four.16 kV, 6.6 kV and 10 kV) and excessive energy (>1 MW) operations [15]. Therefore, it can be concluded that the important pursuits behind designing and developing MLIs were reaching medium voltage packages, lowering switching frequencies and voltage strain for better efficiency, and elevating the range of voltage levels for higher energy quality.

Voltage stress on the switches is a vital component that need to be considered whilst scheming any MLI topology. This article proposes a novel CMI topology that resolved the impulse current and non-uniform operation problems of SC-CMIs whilst maintaining the merits of self-balancing and voltage boosting.

The main contributions of the manuscript can be summarized by the following points;

1] The proposed topology has inherited the high-quality characteristics of two back-to-back T-type inverters shape. This MLI to decrease the entire voltage stress in addition to produce better voltage levels using decreased components.

2] The proposed topology can be extended to produce higher voltage levels following two types of arrangements depending on the application requirements.

3] The modularity and smart switching arrangements of the proposed MLI has enabled it to produce different voltage levels utilizing more than one switching path. This has given the MLI higher flexibility and reliability

II. PROPOSED DUAL-T-TYPE FIVE-LEVEL CASCADED MULTILEVEL INVERTER

The proposed topology is known as a “dual-T-type five-level enhance CMI” following its circuit structure, which contains two T-Type inverters, as depicted in Fig. 1. Considering that each one the power switches are metal-oxide-semiconductor field effect transistors (MOSFETs), the proposed inverter calls for most effective additional power switches to those within the previous take a look at [11]. Voltage boosting is gained by connecting a capacitor C in series with the enter dc source. To prevent the impulse charging current as within the case of SC-CMI, an inductor L this is managed via a half of bridge (S5 and S6) is included within the topology to reap soft charging. The rest of the switches represent T-type inverters for ac voltage magnitude generation.

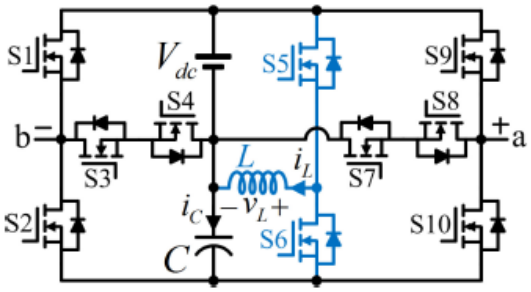

Fig. 1. Proposed DTT-5L-CMI.

TABLE I
Design Specifications

S.NO	DESCRIPTION	VALUE
1	Input voltage Vdc	100 v
2	Carrier frequency	5kHz
3	Capacitor C	1000μF
4	Inductor L	3mH
5	Load resistor	100Ω
6	Load inductor	0.1 H

A. Steady-State Analysis

The switching states of the proposed DTT-5L-CMI are analyzed and summarized in Fig. 2.With capacitor C charged to Vdc, the most voltage level is 2Vdc. Five symmetrical voltage ranges are generated in among 2Vdc and −2Vdc. Some switches are became ON despite they're now not engaging in load current if you want to offer a commutation path for the inductive load current at some point of dead time.

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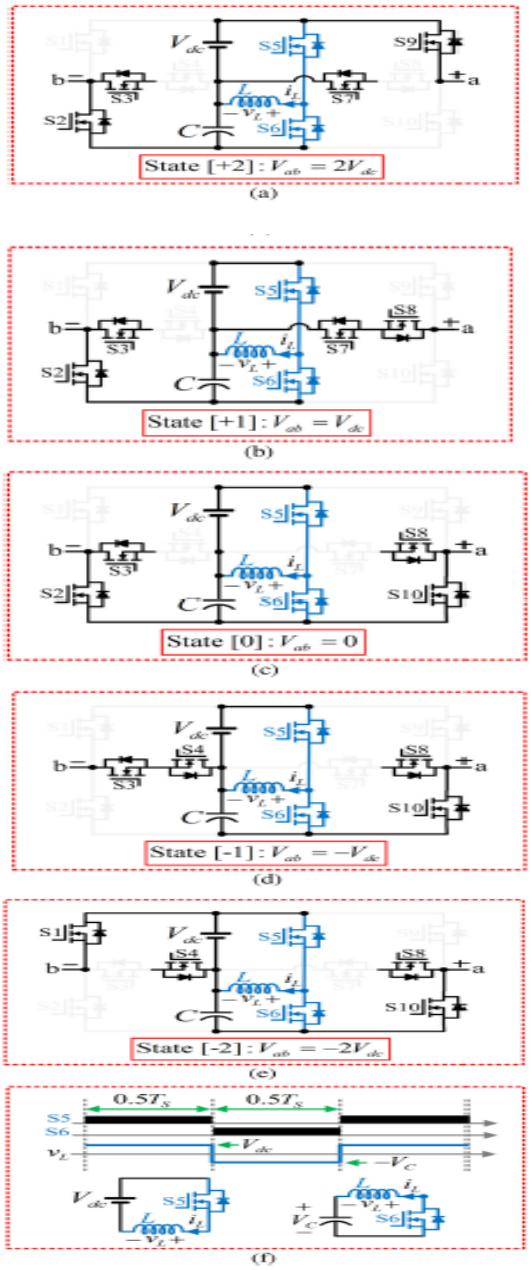

Fig. 2. Switching states of the proposed DTT-5L-CMI: (a) state [+2], (b) state [+1], (c) state [0], (d) state [−1], (e) state [−2], and (f) soft charging of C.

Taking state [0] for instance, S3 and S8 are non-conducting switches which can be grew to become ON to cater for the dead-time commutation. Considering the case while there's a voltage level transition from 0 V to Vdc, both S7 and S10 are OFF to save you short circuit across capacitor C. Assuming an inductive load with S8 is ON, the negative load current can freewheel through S8 in addition to the antiparallel diode of S7. The load voltage will ultimately clamped to Vdc for the duration of dead time, making sure smooth transition from 0 V to Vdc. On the opposite hand, if S8 is OFF, the negative load current is compelled to glide through the antiparallel diode of S9. A voltage spike of 2Vdc will be generated in the course of dead time, that's enormously unwanted. It is therefore essential for all the switching states to be layout with cautious attention to avoid voltage spike at some stage in transfer transitions.

For achieving tender charging of capacitor C, S5 and S6 are managed complementary with a consistent duty cycle of 0.5. Energy is stored temporarily into inductor L by using turning ON S5 earlier than it is discharged to capacitor C while S6 is switched ON. To reduce price, S6 can be replaced with a diode. However, active strength MOSFET is recommended in view of its bidirectional strength go with the flow functionality. The switching states in Fig.3 indicates that switches S1, S2, S5, S6, S9, and S10 each blocks a maximum voltage of 2Vdc, whilst voltage strain at the closing switches are constrained to Vdc. On the alternative hand, the current conduction path analyzed in Fig. 3 depicts that the current stress on S5 and S6 are decided by using the inductor current, while that at the ultimate switches are same to load current.

III. MATLAB/SIMULATION RESULTS

This paper applied level shifted PWM control to generate the switching pulses for the back to back T-type topology. Simulations were directed to concentrate on the practicality of the proposed method. Two back to back modules (n = 2) with dc sources voltage of 100 V each are thought of. The Simulations results are shown in Fig. 6. Every module is creating five even voltage levels somewhere in the range of −200 and 200 V. Their most extreme voltage level is twice of the dc source voltage, subsequently approving a voltage gain of two. A sum of nine various voltage levels are produced and the most extreme voltage level is reached out to 400 V. Individual module is additionally researched in this Simulation. Perceptions shows that the capacitor voltage, capacitor current, and inductor current caught for the two modules are comparable. This infers that the tasks for the two modules are uniform and the modularity feature of back to back inverter structure is held. It is also showed in Fig. 6 that the capacitor charging current is dictated by the inductor current. This is on the grounds

that the capacitor in every module is charged through its separate inductor. In such manner, soft switching is accomplished and no impulse current is seen in the plotted capacitor current waveforms.

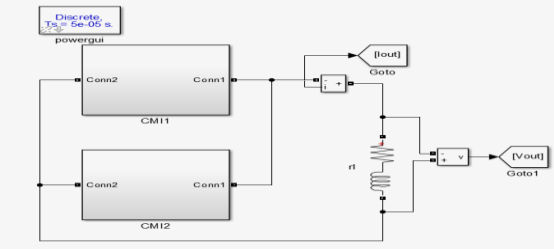

Fig3 Simulation block diagram for the proposed method.

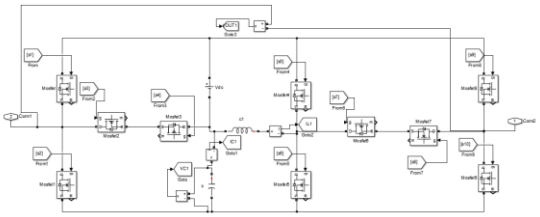

Fig 4 simulation diagram T-Type CMI

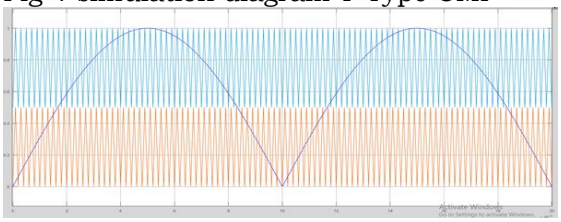

Fig 5. Modulation scheme for each module.

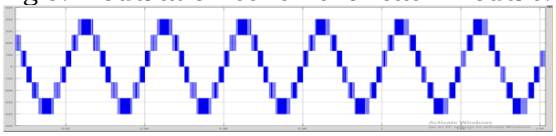

Fig 6a output voltage waveform for the proposed method

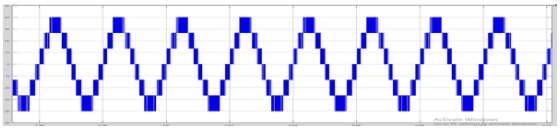

Fig 6b output current waveform for the proposed method

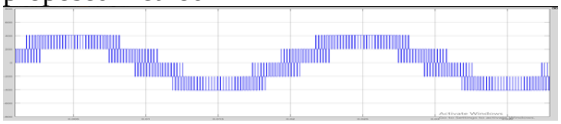

Fig 6c output voltage waveform for first module

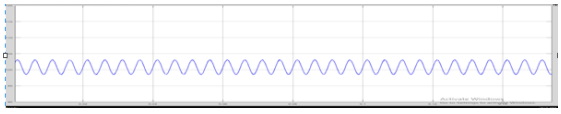

Fig 6d output capacitor voltage waveform for first module

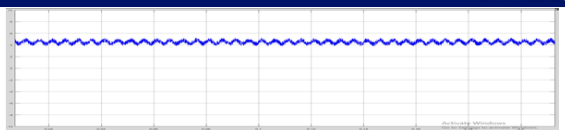

Fig 6e output capacitor current waveform for first module

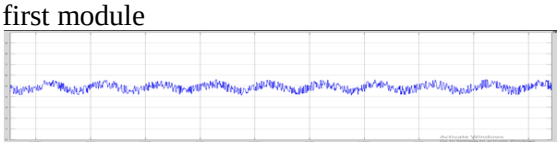

Fig 6f output inductor current waveform for first module

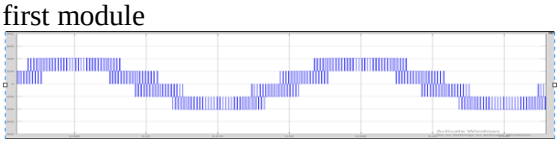

Fig 6g output voltage waveform for second module

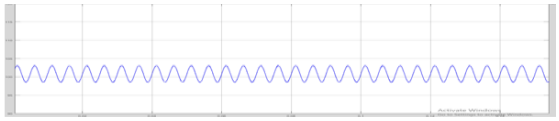

Fig 6h output capacitor voltage waveform for second module

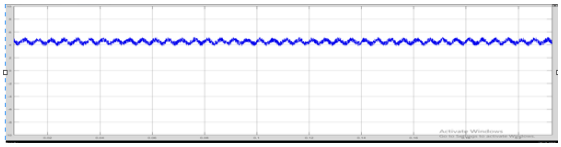

Fig 6i output capacitor current waveform for second module

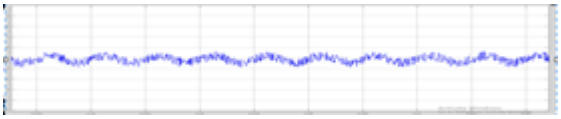

Fig 6j output inductor current waveform for second module

Fig. 6(a-j) Simulation results of the proposed DTT-5L-CMI with two cascaded modules (n = 2).

VI Future Work

Although the 5L drive systems have better performance compared to 3L and 2L drive systems, the fault diagnosis and fault tolerance of these topologies have not been studied yet. Therefore, the authors plan to study the fault diagnosis and tolerance of 5L T-type converters. In addition, the authors are going to test the performance of the 5L T-type converters using advanced semiconductor technologies and for three phase topologies in order to enhance their power circuit and reduce the EMI effects.

V CONCLUSION

In this article, an advanced CMI topology is presented. Theoretical analyses were performed and verified by using simulation in MATLAB/Simulink. The proposed DTT-5L-CMI is able to five levels technology with double voltage boosting advantage. Soft charging of capacitor and uniform operation for all cascaded modules are achieved that resolved the issues of new SC-CMI. Therefore, the proposed topology is an appealing opportunity for dc–ac energy conversion device.

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