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A THREE-PHASE SERIES-PARALLEL CONVERTED CASCADED SWITCHED CAPACITOR MULTILEVEL INVERTER FOR INDUCTION MOTOR DRIVE

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ABSTRACT: Multilevel Inverter widely used in high power industrial applications. This paper presents a three-phase series-parallel converted cascaded multilevel inverter with switched capacitor component for induction motor drive. In traditional switched capacitor inverters required more number of components, it seem to more complex control circuitry and bulky. All over world concentrating to improve the efficiency of Multilevel Inverter such as voltage balancing, reduction in components, switched capacitor multilevel inverter methods etc. The Proposed multilevel inverter output voltage level increasing by using less number of switches driven by the multicarrier series-parallel techniques. In this paper presents generalized structure, Operation, comparison with other traditional topology; the aim of this paper is to present a new structure for switched-capacitor multilevel inverters (SCMLIs) which can generate a great number of voltage levels with optimum number of components for both symmetric and asymmetric values of dc-voltage sources. In this paper, initially, a new switched-capacitor dc/dc converter (SCC) is presented which can switch as conventional series/parallel conversion and generate multiple dc-link voltages with optimum components. In this case, voltage of all capacitors is filled by binary asymmetrical pattern without using any auxiliary circuits. That has boost ability and can charge capacitors as self-balancing by using the proposed binary asymmetrical algorithm and series–parallel conversion of power supply.The single-phase multilevel inverter is extended for three-phase and applicable to induction motor drive.Induction motor stator current speed and torque responses are improved it can be shown by using MATLAB/SIMULINK platform.

KEY WORDS: Switched Capacitor Converter(SCC), Sub multilevel inverters (SMLI), D-STATCOM and Induction Motor.

I. INTRODUCTION

Nowadays, the multilevel inverters have received more attentions their considerable advantages such as high power quality, lower harmonic components, better electromagnetic consistence, lower switching losses. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources [1].Multilevel inverters are composed of a number of power electronic switches and DC voltage sources that produce a stepped voltage waveform in its output. Generally, multilevel inverters are divided into three categories as follows: neutral-

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point clamped inverter (NPC), flying capacitor inverter (FC), and cascaded H-bridge inverter (CHB) [2-4]. These inverters can surrender higher power with lower dv/dt and di/dt in output waveform which is to reduce EMI noise and Size of the output filter. Cascade inverters are made of series separate single phase inverters with separate dc voltage sources. On the other hand, this inverter consists of a number of basic blocks (sub multilevel inverter) that each of these blocks has similar control system. One of the major advantages of this type of inverters is the ability of its modulation [5]. So, if an error occurs in one of the blocks, it can replace or fix by using a control system, but there are some disadvantages such as high number of dc voltage sources and power electronic switches. Increasing the number of power electronic switches leads to increase the number of driver circuits too. Both of these issues caused to increase in complexity, size, and cost of the circuit. Thus, reducing the number of power electronic switches is very vital and should be considered [6].A switched-capacitor (SC) inverter outputs multilevel voltages with switched capacitors. The SC inverter outputs a larger voltage than the input voltage in similar way to the charge pump. Switched capacitor (SC) power converters are a subset of power converters with the help of only switches and capacitors this can efficiently convert one voltage to another voltage. SC comprises of different topologies, but topology employed here is series/parallel topology [6-9]. SCMLIs contain several capacitors and switches, which can connect dc power supply to ac output and are able to decrease the burden of power supply to achieve higher number of voltage levels.

A new series parallel switched MLI in order to synthesize a sinusoidal voltage from isolated dc sources through the passage of a minimum number of active switches in the path for the current to reach each level is presented [10]. New types of SCMLIs have emerged using the series–parallel switching strategy (SCISPC). The distinctive features of these types of inverters are that they can increase the flexibility of systems by switching between several capacitors in series or parallel modes and therefore can transfer more input power to the output [11].A new switched-capacitor dc/dc converter (SCC) is presented which can switch as conventional series/parallel conversion and generate multiple dc-link voltages with optimum components. In this case, voltage of all capacitors is filled by binary asymmetrical pattern without using any auxiliary circuits. At the next, a new submultilevel inverter (SMLI) topology presents, which is performed based on the proposed SCC unit and without using the full H-bridge cell. In addition, this structure is suitable for an inductive load with the capability to pass the reverse current. After that, the proposed submultilevel modules are cascaded with each other and create more output voltage levels [12][13]. Therefore, most of the parameters such as number of required switches, diodes, maximum current path components, and value of total blocked or standing voltage are improved. Induction motor is further implemented to proposed system the results are validated by using MATLAB/SIMULINK Software.

II. PROPOSED SCC

Fig.1(a) shows the basic circuit of the proposed SCC. This circuit is named as basic unit and contains one dc power supply, one capacitor,

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one passive power diode, and two active power switches. Photovoltaic (PV) cells, batteries, and fuel cells can be used as a power supply in this structure. Fig.1(b) and (c) shows that how to carry out the charging and discharging operations for capacitor C. Switches Sa and Sb are used in series and parallel conversions, respectively. As it can be inspected, when the switch Sb becomes ON, the capacitor C is charged to Vdc and when the switch Sa turns ON, the diode becomes reverse biased and capacitor is discharged. In this mode, the power supply's energy and stored energy of C are transferred to the output. It is obvious that, basic unit does not need any extra charge balancing control circuits and complicated commutation methods, which is counted as a great merit of this structure. Also, it is remarkable that, the internal resistance of power diode and capacitor can damp the unequal voltage between capacitor and dc-voltage source during the charging operation, which leads to introduce an effective and practical power circuit.

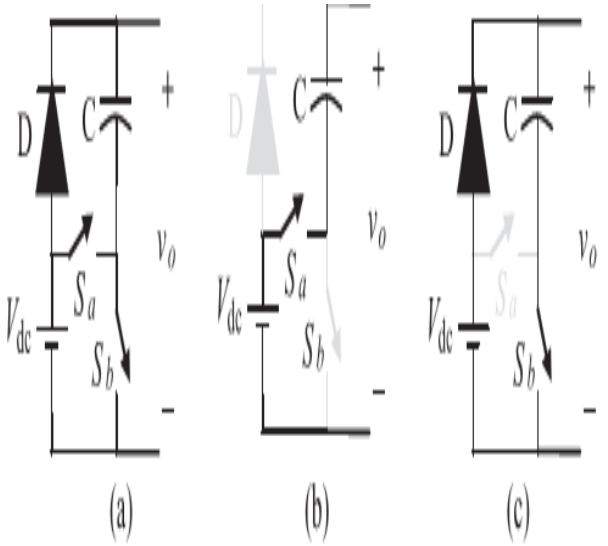

Fig.1(a) Basic series/parallel unit. (b) Capacitor discharging mode. (c) Capacitor charging mode.

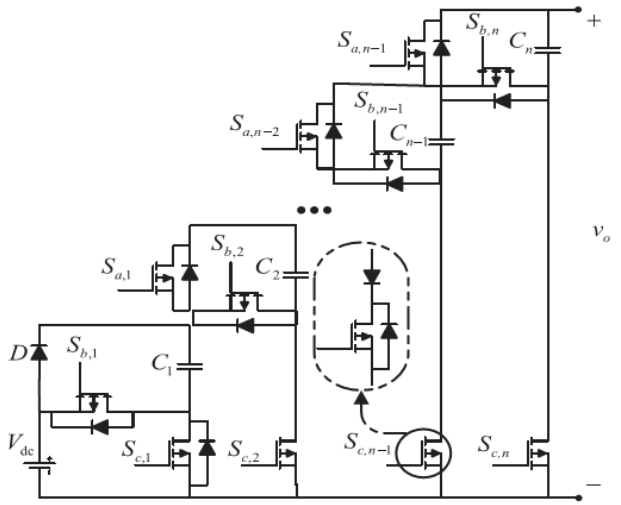

Fig.2. Proposed SCC

The proposed dc/dc converter is made by extended connection of this basic unit. Then, a staircase voltage waveform is generated at the output with the capability of passing the reverse current for inductive load and can be used as a part of inverters. Fig.2 shows the circuit configuration of the proposed converter. In order to charge all the capacitors and generate output voltage waveform, the switches Sai(i = 1,2, . . . , n − 1), Sbi, and Sci(i = 1,2, . . . , n) are driven by series/parallel conversion or combination of them.In this case, switches Sci are unidirectional power switches without antiparallel diode, which can pass the reverse inductive load current and other switches are also unidirectional with internal antiparallel diode. As figure shows, switches Sci(i = 2,3, . . . , n) can be substituted by ordinary power switches and a series diode to counteract the effect of internal antiparallel diode. Table I indicates the different switching and capacitors' states for the proposed SCC.In this table, 0 and 1 mean OFF and ON switching state and C and D refer to charging and discharging modes for capacitors, respectively. In order to generate more number of output voltage levels with

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optimum number of components, all the capacitors should be charged by binary asymmetrical algorithm, according to this table in such a way that, in state (1) when switch Sc,1 becomes ON, capacitor C1 is charged to Vdc and this voltage level is transferred to the output through Sa,i(i = 1,2, . . . , n − 1) simultaneously. Also in state (2), C2 is being charged to Vdc + Vc1 through switch Sc,2 and with discharging of C1, second voltage level generates at the output through Sa,i and Sb,1, simultaneously, which is equal to 2Vdc. After this moment, without entering other capacitors into the circuit, voltage level of 3Vdc can be transferred to the output by stored voltage of C2 and constant dc-voltage source. In this moment, C1 is again charged by dcvoltage source directly and for the next voltage level, this stored voltage besides the across voltage of C2 and constant dc-voltage source are transferred to the output, which is equalized to 4Vdc and this consecutive operation continues so on.

TABLE I
SWITCHING AND CAPACITORS STATES OF THE PROPOSED SCC

v_o		V_{dc}	$2V_{dc}$	$3V_{dc}$	$4V_{dc}$	⋯	$2^n V_{dc}$
Switching states	$S_{a,1}$	1	1	0	0	⋯	0
	$S_{a,2}$	1	1	1	1	⋯	0
	⋮	1	1	1	1	⋯	0
	$S_{a,n-1}$	1	1	1	1	⋯	0
	$S_{b,1}$	0	1	0	1	⋯	1
	$S_{b,2}$	0	0	1	1	⋯	1
	⋮	0	0	0	0	⋯	1
	$S_{b,n}$	0	0	0	0	⋯	1
	$S_{c,1}$	1	0	1	0	⋯	0
	$S_{c,2}$	0	1	0	0	⋯	0
	⋮	0	0	0	⋮	⋯	0
	$S_{c,n}$	0	0	0	0	⋯	0
Capacitors states	C_1	C	D	C	D	⋯	D
	C_2	–	C	D	D	⋯	D
	C_3	–	–	–	C	⋯	D
	⋮	⋮	⋮	⋮	⋯	⋯	D
	C_n	–	–	–	–	C	D

The prominent feature of the proposed circuit is that by entering the next capacitors into the circuit and also continuing the series–parallel switching strategy, the number of output voltage levels is enhanced as binary manner from Vdc to 2^nVdc.It is important to note that, always at each of voltage steps, the pertinent capacitor of previous steps must be connected as parallel to keep on the charging operation. Therefore, if we assume the number of capacitors equal to n, the stored voltage of each capacitor would be equalized to

$$V_{C,k} = 2^{k-1}V_{dc}, \text{ for } k = 1,2,\ldots,n \tag{3.1}$$

Also from this table, it is obvious that, the proposed SCC is able to generate different positive output voltage levels by self-balancing ability. Now, by considering the proposed overall structure (Fig.2), number of required switches (Nswitch,u) or gate drivers (NDriver,u), number of required isolated-gate bipolar transistors (IGBTs) (NIGBT,u), power diodes (Ndiode,u), and output voltage levels (Nlevel,u) are calculated by the following equations, respectively,

$$N_{\text{switch},u} = N_{\text{Driver},u} = N_{\text{IGBT},u} = 3n - 1 \tag{3.2}$$

$$N_{\text{diode},u} = n \tag{3.3}$$

$$N_{\text{level},u} = 2^n \tag{3.4}$$

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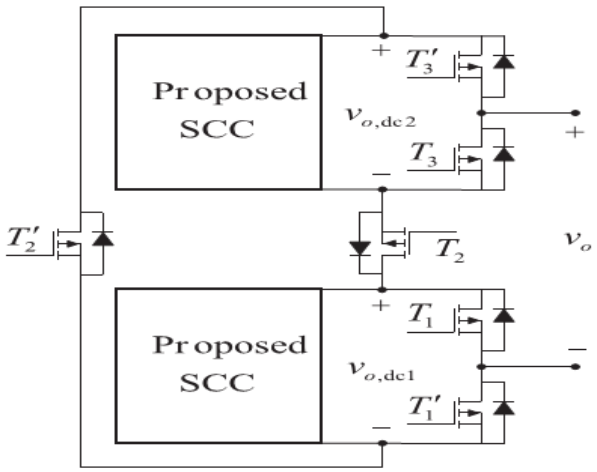

Fig.3. Proposed SMLI configuration.

According to (4), the proposed circuit possesses an appropriate performance as boost capability. This factor can be defined as

$$\beta = \frac{V_{o,\max,u}}{\sum V_{dc}} = 2^n \tag{3.5}$$

Moreover, this structure is able to mitigate the total blocked voltage. As it is clear, the value of blocked voltage should be tolerated by switches and means standing voltage across of switches, which effects on conduction losses, efficiency, and cost. In this case, the total blocked voltage is formulized by

$$V_{\text{block},u} = [3(2^n - 1) - 1]\, V_{dc} \tag{3.6}$$

III. PROPOSED SMLI

As it was analyzed before, the proposed SCC generates output voltage waveform with positive polarity. Therefore, it is not suitable for inverter applications. In order to change the polarity and create an ac waveform, an H-bridge cell can be connected to the output similar to the other existing structures. However, this cell may increase the number of required IGBTs and the number of involved components in the current path. This project has not focused on added H-bridge cell and presents a new scheme of SCISP shown in Fig.3.3, based on two utilized half-bridges.In order to convert the output polarity of SCC and create all the voltage levels (even and odd) at the output, this structure always requires a pair stage of SCC units. Therefore, the proposed SCISPC named as SMLI can produce positive, zero, and negative output voltage levels with six unidirectional power switches and two same units of SCC. As a result, 2n capacitors and two isolated dc power supplies are needed for this structure.

Now, the number of required IGBTs or gate drivers and the number of power diodes can be expressed as follows:

$$N_{\underset{\text{Sub}}{\text{IGBT}}} = N_{\underset{\text{Sub}}{\text{Driver}}} = 6n + 4 \tag{3.7}$$

$$N_{\underset{\text{Sub}}{\text{Diode}}} = 2n. \tag{3.8}$$

Table II indicates ON switching states of the proposed SMLI, which is summarized by seven different modes. According to this table, to refrain from short-circuit problems, switches of

TABLE II
SWITCHING PATTERN OF THE PROPOSED SMLI

		ON switches	v_o
Switching states	1	T_1', T_2, T_3'	$v_{o,dc1} + v_{o,dc2}$
	2	T_1, T_2, T_3'	$v_{o,dc2}$
	3	T_1', T_2, T_3	$v_{o,dc1}$
	4	T_1, T_2, T_3	0
		T_1', T_2', T_3'	
	5	T_1, T_2', T_3'	$-v_{o,dc1}$
	6	T_1', T_2', T_3	$-v_{o,dc2}$
	7	T_1, T_2', T_3	$-v_{o,dc1} - v_{o,dc2}$

(T1, T'1), (T2, T'2), and (T3, T'3), are triggered as complementary operation with each other's and should not to be ON simultaneously. Also, this structure can work on symmetric and asymmetric values of dc-voltage sources. In

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symmetric structure, all the dc sources are equal and that are different in asymmetric topology. Then, by considering (1), to obtain the maximum number of voltage levels from asymmetric condition, the value of other isolated dc power supply should conform the following expression:

$$V_{dc,2} = (1 + 2^n)V_{dc,1} \tag{3.9}$$

TABLE III
DIFFERENT RELATED EQUATIONS FOR THE PROPOSED SMLI TOPOLOGY

Parameters	Symmetric	Asymmetric
N_{level} Sub	$1+2^{n+2}$ (11)	$1+2^{n+2}+2^{2n+1}$ (14)
$v_{o,\max}$ Sub	$2^{n+1}V_{dc}$ (12)	$[2^{n+1}+2^{2n}]V_{dc}$ (15)
V_{block} Sub	$2\sum_{j=1}^{3}V_{\text{block},Tj}+\sum_{j=1}^{2}V_{\text{block},uj}$ (13) $=[(7\times 2^{n+1})-8]V_{dc}$	$2\sum_{j=1}^{3}V_{\text{block},Tj}+\sum_{j=1}^{2}V_{\text{block},uj}$ (16) $=[2^{2n+2}+2^{n+3}]V_{dc}$

Table III indicates the pertinent equations of N_{level} Sub, $v_{o,\max}$ Sub, and V_{Blocked} Sub for symmetric and asymmetric forms in the proposed SMLI. In this case, the asymmetric calculations in Table III are done by considering (9).To achieve the greater number of voltage levels, the proposed SMLI can be extended by increasing the number of output voltage levels for the proposed SCC. But, this way yields some identical restrictions due to increase in the voltage drop and existed spikes across each of capacitors especially in high power ratio. To avoid this constraint, the best solution to increase the number of voltage levels is considered by series connection of the proposed SMLIs with each other shown as proposed cascaded sub multilevel inverter (CSMLI) in Fig.4. In this figure, number of cascaded SMLI units is indexed by m. As a result, output voltage of the proposed CSMLI is obtained by

$$v_o(t) = v_{o,1}(t) + v_{o,2}(t) + \cdots + v_{o,m}(t) \tag{3.10}$$

It should be noted that, in this case, the number of capacitors that have been used in each of SCCs is assumed same. To reduce the cost, weight, total blocked voltage, and some other identical problems, the required capacitors for each of the proposed SCC units (n) is optimized.

IV. PROPOSED IMPROVED CSMLI

The number of required capacitors in each of the proposed SMLI units is optimized from the view point of maximum produced output voltage levels for the proposed CSMLI with minimum number of IGBTs. This optimization is done based on asymmetric value of dc sources according to (9).

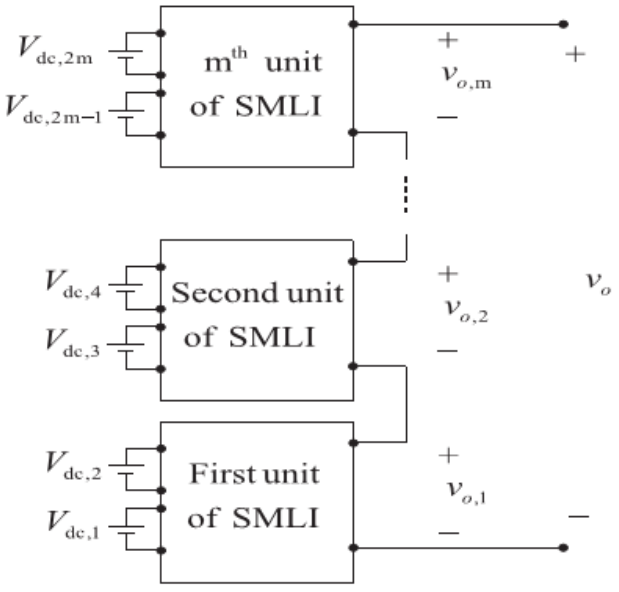

Fig.4. Proposed CSMLI

In general, the number of output voltage levels for the proposed CSMLI is obtained by

$$N_{\text{level}} = \left(N_{\text{level}}\right)^m \tag{3.17}$$

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where $N_{\text{Sub}}^{\text{level}}$ Sub is the number of output voltage levels for the proposed SMLI, which is calculated by (14). Then, (17) can be rewritten as

$$N_{\text{level}} = \left(2^{n+2} + 2^{2n+1} + 1\right)^{m} \tag{3.18}$$

On the other hand, the relation of m in terms of NIGBT (number of required IGBTs for the proposed CSMLI) and $N_{\text{Sub}}^{\text{IGBT}}$ is equalized to the following equation:

$$m = \frac{N_{\text{IGBT}}}{N_{\text{Sub}}^{\text{IGBT}}} \tag{3.19}$$

Also, by inserting (13) into (18) and (19),

$$N_{\text{level}} = \left(2^{n+2} + 2^{2n+1} + 1\right)^{\frac{N_{\text{IGBT}}}{6n+4}} \tag{3.20}$$

In order to obtain the optimal number of capacitor from each of SMLIs, the variation of Nlevel against NIGBT for specific number of n, is curved according to (20) and illustrated by Fig.5. As this figure shows, for a constant value of NIGBT, Nlevel has been maximized when one capacitor is being used. Therefore, with respect to n = 1, number of output voltage levels, required IGBTs, power diodes, and total value of blocked

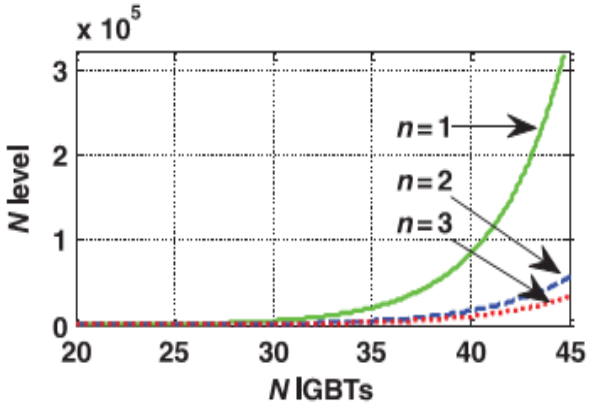

Fig.5. Variation of N_{level} against N_{IGBT} for different values of n.

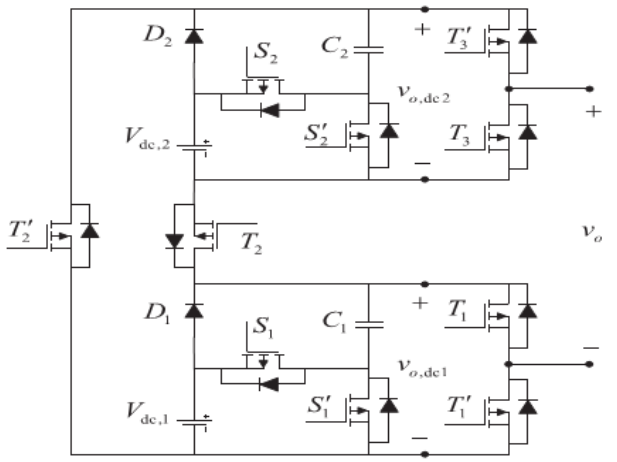

Fig.6. Proposed 17-level structure

voltage for the proposed improved CSMLI are obtained for both symmetric and asymmetric conditions and are summarized in Table IV. In addition, based on (9), the value of dc-voltage sources in ith unit of the proposed CSMLI should be adopted by

$$V_{\text{dc2},i} = 3V_{\text{dc1},i} = 3(17^{i-1})V_{\text{dc}}, \quad i = 1,2,\ldots,m \tag{3.21}$$

Fig.6 shows an improved CSMLI configuration by considering m = 1, which leads to generate 17-level output voltage based on the proposed asymmetric topology. In this circuit, the values of dc isolated power supplies are set on Vdc and 3Vdc according to (9). Table V shows the switching pattern of the proposed 17-level inverter.In this case, all the switches are driven by fundamental switching frequency, whereas the sinusoidal reference voltage is compared with some available dc-voltage levels and create the related gate switching pulses. The most advantage of this switching method is referred to low switching frequency that yields to the reduction of switching loss. Details of fundamental switching modulation strategy are not the objective of this paper. In addition from Table V, it is clear that, to generate each of the output voltage levels, only five switches are being involved in the current path.

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At this stage, to determine the capacitance of C1 and C2, two assumptions are considered in which one is related to the output sinusoidal load current with phase difference between output voltage and current (ϕ) and the other is contributed to the same duration in each step of staircase output voltage. Thus, the maximum discharging amount of each capacitor can be defined as (30) in one half-cycles

TABLE IV
DIFFERENT RELATED CALCULATIONS OF THE PROPOSED IMPROVED CSMLI

Parameters	Symmetric	Asymmetric
N_{level}	$8m+1$ (22)	17^m (25)
$V_{o,max}$	$4mV_{dc}$ (23)	$\frac{17^m-1}{2}$ (26)
V_{block}	$m\times[2\sum_{j=1}^{3}V_{block,Tj}+\sum_{j=1}^{2}V_{block,sj}]$ (24) $=20mV_{dc}$	$\sum_{k=1}^{m}(2\sum_{j=1}^{3}V_{block,Tj,k}+\sum_{j=1}^{2}V_{block,sj,k})$ (27) $=\frac{5(17^m-1)}{2}$
N_{IGBT}	$10m$ (28)	
N_{Diode}	$2m$ (29)	

TABLE V
DIFFERENT SWITCHING AND CAPACITORS STATES OF THE PROPOSED 17-LEVEL INVERTER

		ON switches	v_o	C_1	C_2
Switching states	1	T_1',T_2,T_3',S_1,S_2	$4V_{dc}+v_{c,1}+v_{c,2}$	D	D
	2	T_1',T_2,T_3',S_1',S_2	$4V_{dc}+v_{c,2}$	C	D
	3	T_1,T_2,T_3',S_1',S_2	$3V_{dc}+v_{c,2}$	C	D
	4	T_1',T_2,T_3',S_1,S_2'	$4V_{dc}+v_{c,1}$	D	C
	5	T_1',T_2,T_3',S_1',S_2'	$4V_{dc}$	C	C
	6	T_1,T_2,T_3',S_1',S_2'	$3V_{dc}$	C	C
	7	T_1',T_2,T_3,S_1,S_2'	$V_{dc}+v_{c,1}$	D	C
	8	T_1',T_2,T_3,S_1',S_2'	V_{dc}	C	C
	9	T_1,T_2,T_3,S_1',S_2' T_1',T_2',T_3,S_1',S_2'	0	C	C
	10	T_1,T_2',T_3',S_1',S_2'	$-V_{dc}$	C	C
	11	T_1,T_2',T_3',S_1,S_2'	$-V_{dc}-v_{c,1}$	D	C
	12	T_1',T_2',T_3,S_1',S_2'	$-3V_{dc}$	C	C
	13	T_1,T_2',T_3,S_1',S_2'	$-4V_{dc}$	C	C
	14	T_1,T_2',T_3,S_1,S_2'	$-4V_{dc}-v_{c,1}$	D	C
	15	T_1',T_2',T_3,S_1',S_2	$-3V_{dc}-v_{c,2}$	C	D
	16	T_1,T_2',T_3,S_1',S_2	$-4V_{dc}-v_{c,2}$	C	D
	17	T_1,T_2',T_3,S_1,S_2	$-4V_{dc}-v_{c,1}-v_{c,2}$	D	D

$$Q_{Ci}=\int_{t_j}^{\frac{T}{4}-t_j} I_{out}\sin(2\pi f_S t-\varphi)dt,\quad i=1,2 \tag{3.30}$$

where T, f_S, and Iout are the period of one cycle, frequency of output voltage, and amplitude of load current, respectively, and also $[t_j,\frac{T}{4}-t_j]$ is the time interval corresponded to the longestdischarging cycle (LDC) of each capacitor. On the other hand, in the proposed 17-level inverter, this time interval varies for $C1$ and $C2$. According to Table V, the LDC for $C1$ and $C2$ is illustrated by Fig.7. Thus, by considering the kVin as maximum allowable voltage ripple, the optimum value of capacitors can be taken by

$$C_{opt,i}\geq\frac{Q_{Ci}}{kV_{in}},\quad i=1,2 \tag{3.31}$$

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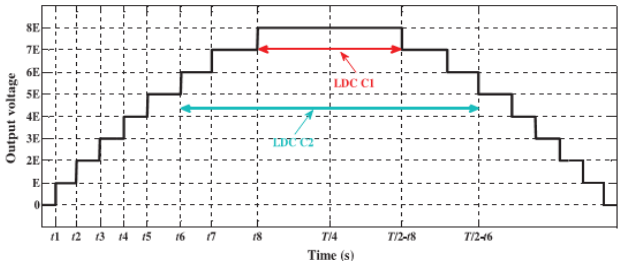

Fig.7. Typical output voltage waveform of 17-level inverter for positive half-cycle.

V. POWER LOSS ANALYSIS

Theoretical total power losses and overall efficiency of the proposed improved CSMLI based on (m = 1) are calculated. For this kind of converters, always three major types of associated losses should be considered, which include: switching losses (Psw), conduction losses of semiconductor devices (PCon), and ripple losses of two utilized capacitors (PRip). All calculations are done based on the fundamental switching frequency strategy.

A. Switching Losses

Switching loss occurs during the ON and OFF period of switching states. For simplicity, a linear approximation between voltage and current of switches in the switching period is considered. Based on thisassumption, the following equations can be expressed for ith involved power switch:

$$\begin{aligned} P_{\mathrm{sw,on},i} &= f_{\mathrm{sw}} \int_0^{t_{\mathrm{ON}}} v_{\mathrm{ON},i}(t) i(t) dt \\ &= f_{\mathrm{sw}} \int_0^{t_{\mathrm{ON}}} \left(\frac{V_{\mathrm{ON},i}}{t_{\mathrm{ON}}} t\right) \left(-\frac{I_i}{t_{\mathrm{ON}}}(t - t_{\mathrm{ON}})\right) dt \\ &= \frac{1}{6} f_{\mathrm{sw}} V_{\mathrm{ON},i} I_i t_{\mathrm{ON}} \end{aligned} \tag{3.32}$$

$$\begin{aligned} P_{\mathrm{sw,OFF},i} &= f_{\mathrm{sw}} \int_0^{t_{\mathrm{OFF}}} v_{\mathrm{block},i}(t) i(t) dt \\ &= f_{\mathrm{sw}} \int_0^{t_{\mathrm{OFF}}} \left(\frac{V_{\mathrm{block},i}}{t_{\mathrm{OFF}}} t\right) \left(-\frac{I'_i}{t_{\mathrm{OFF}}}(t - t_{\mathrm{OFF}})\right) dt \\ &= \frac{1}{6} f_{\mathrm{sw}} V_{\mathrm{block},i} I'_i t_{\mathrm{OFF}} \end{aligned} \tag{3.33}$$

where Ii and $I_i^{'}$ are the currents that pass through ith power switch after turning ON and before turning OFF, respectively, and fsw is the switching frequency equalized to the reference frequency. In order to calculate the total switching loss, the number of ON (Non) and the number of OFF (Noff) switching states per one cycle should be multiplied by (32) and (33) according to the following:

$$P_{\mathrm{sw}} = \sum_{i=1}^{10} \left(\sum_{k=1}^{N_{\mathrm{ON}}} P_{\mathrm{sw,ON},ik} + \sum_{k=1}^{N_{\mathrm{OFF}}} P_{\mathrm{sw,OFF},ik} \right) \tag{3.34}$$

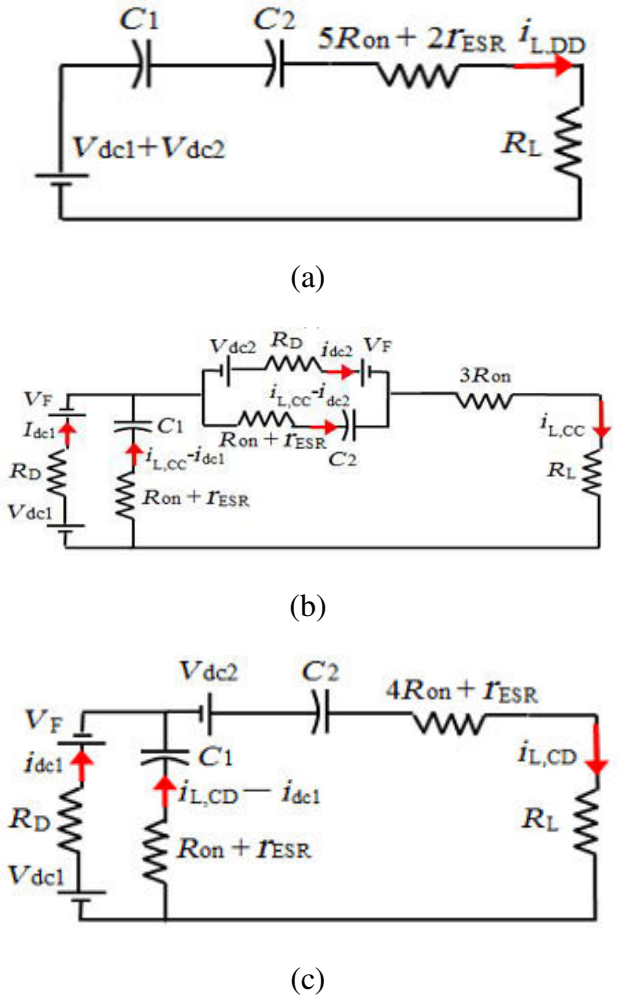

Fig.8. Equivalent circuit of the proposed 17-level structure with a resistive load in (a) discharging modes, (b) charging modes, and (c) combination of charging and discharging modes

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B. Conduction Losses

To calculate the total conduction losses of each component, a straightforward method based on pure-resistance load is presented. Regarding Table V, three possible operating modes can be investigated including discharging states for both capacitors (states number of 1 and 17), charging states for both capacitors (states number of 5, 6, 8, 10, 12, and 13), and discharging states for one capacitor and charging states for another one or vice versa (other remaining states).Fig.8(a)–(c) demonstrates the equivalent circuits of charging and discharging operating modes for capacitors. In these figures, Ron, RD, rESR, RL, and VF are the internal ON-state resistance of each switch, internal resistance of each diode, equivalent series resistance (ESR) of each capacitor, load resistance, and the forward voltage drop of each incurred diode, respectively.According to Fig.8(a) during the series connection of capacitors to the respective dc-voltage sources, the value of load current can be written as

$$i_{L,DD} = \frac{4V_{dc} + v_{c,1} + v_{c,2}}{5R_{ON} + 2r_{ESR} + R_L} \quad (3.35)$$

Therefore, the instantaneous conduction loss (pc,DD) and average conduction loss ($\overline{pc,DD}$) for one full cycle of discharging mode with respect to the time intervals of Fig.3.7 and Table V, can be calculated as follows:

$$p_{c,DD} = (5R_{ON} + 2r_{ESR}) i_{L,DD}^2 \quad (3.36)$$

$$\overline{p_{c,DD}} = \frac{2f_{sw}}{\pi}\left(\frac{\pi}{2} - t_8\right) p_{c,DD} \quad (3.37)$$

Also, with respect to Fig.8(b) and by considering the time intervals between states of 3 and 5 and also states of 1 and 2 in Fig.7, the instantaneous and average value of conduction losses for charging modes of both capacitors (pc,CC and pc,CC), are driven by the following equations, respectively,

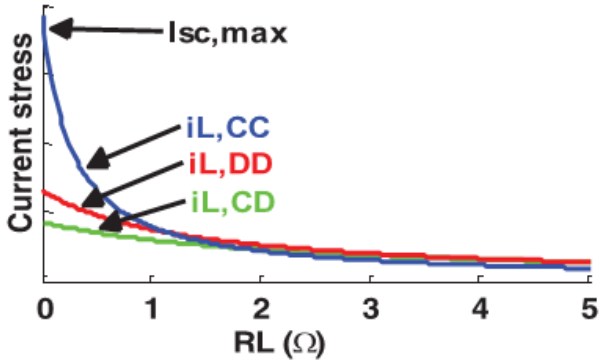

Fig.9. Variation of current stresses versus RL in three defined modes

$$p_{c,CC} = 3R_{ON} i_{L,CC}^2 + R_D(i_{dc,1}^2 + i_{dc,2}^2) + (R_{ON} + r_{ESR})\left[(i_{L,CC} - i_{dc,1})^2 + (i_{L,CC} - i_{dc,2})^2\right] \quad (3.38)$$

$$\overline{p_{c,CC}} = \frac{2f_{sw}}{\pi}\left[(t_5 - t_3) + (t_2 - t_1)\right] p_{c,CC} \quad (3.39)$$

where $i_{dc,1}$ and $i_{dc,2}$ can be calculated by using the Kirchhoff voltage law (KVL) according to following, respectively,

$$i_{dc,1} = \frac{(r_{ESR} + R_{ON}) i_{L,CC} + V_{dc} - v_{c,1} - V_F}{R_D + r_{ESR} + R_{ON}} \quad (3.40)$$

$$i_{dc,2} = \frac{(r_{ESR} + R_{ON}) i_{L,CC} + 3V_{dc} - v_{c,2} - V_F}{R_D + r_{ESR} + R_{ON}} \quad (3.41)$$

In addition, by taking Figs.8(c) and 7 into account, when the capacitor of C1(C2) is charged (discharged) and C2(C1) is discharged (charged), the instantaneous and average conduction losses can be expressed as follows, respectively,

$$P_{c,CD,i} = (4R_{ON} + r_{ESR}) i_{c,CD}^2 + R_D i_{dc,i}^2 + (R_{ON} + r_{ESR})(i_{c,CD} - i_{dc,i})^2 \quad \text{for } i = 1, 2 \quad (3.42)$$

$$\overline{p_{c,CD}} = \frac{2f_{sw}}{\pi}\left[[(t_8 - t_6)] p_{c,CD,2} + [(t_6 - t_5) + (t_3 - t_2)] p_{c,CD,1}\right]. \quad (3.43)$$

As a result, the total value of conduction losses (PCon) in one full cycle can be summarized by the following:

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$$P_{Con} = \overline{p_{c,DD}} + \overline{p_{c,CC}} + \overline{p_{c,CD}} \quad (3.44)$$

Fig.9 shows the variation of load current stresses versus load resistance. As it can be found, the maximum value of short circuit current ($i_{SC,max}$) occurs in the charging mode operation ($i_{L,CC}$) and therefore this value must be tolerated by incurred components among the three defined modes.

C. Ripple Losses

When the capacitors are connected in parallel for charging operation, the ripple losses occur by the difference between the respective input voltage and the across voltage of capacitors (vc,i(i = 1, 2)). Therefore, the ripple voltage of capacitors (ΔVCi) is taken from

$$\Delta V_{Ci} = \frac{1}{C_i} \int_{t'}^{t} i_{C_i}(t)dt \quad (3.45)$$

whereiCi(t) is the passing current of capacitor and $[T' - t]$ is that the time interval for charging modes, which can be attained by regarding Table V. Thus, the total value of ripple loss, for one full cycle of output waveform is equalized to the following equation:

$$P_{Rip} = \frac{f_{sw}}{2} \sum_{i=1}^{2} C_i \Delta V_{Ci}{}^2 \quad (3.46)$$

From (45) and (46), it is clear that, PRip is inversely proportional to the capacitance Ci, which means larger capacitance contributes to higher value of the overall efficiency.

Moreover, based on the above analysis, in order to design the proposed converter, two main identical restrictions must be considered, which are expressed as follows:

$$I_{out,max} \leq \frac{i_{sc,max}}{\lambda} \quad (3.47)$$

$$V_{out,max} \leq \frac{V_{Block}}{\lambda} \quad (4.48)$$

where λ, Vout,max, and Iout,max are a safety coefficient, maximum value of output voltage, and current, respectively. Therefore, with respect to (47) and (48), the maximum value of output power (Pout,max) can be expressed as

$$P_{out,max} \leq \frac{V_{Block} i_{sc,max}}{\lambda^2} \quad (3.49)$$

Finally, the overall efficiency of the proposed improved CSMLI can be defined by the following:

$$\eta = \frac{P_{out}}{P_{out} + P_{sw} + P_{Con} + P_{Rip}} \quad (3.50)$$

V. INDUCTION MOTOR

An asynchronous motor type of an induction motor is an AC electric motor in which the electric current in the rotor needed to produce torque is obtained by electromagnetic induction from the magnetic field of the stator winding. An induction motor can therefore be made without electrical connections to the rotor as are found in universal, DC and synchronous motors. An asynchronous motor's rotor can be either wound type or squirrel-cage type.Three-phase squirrel-cage asynchronous motors are widely used in industrial drives because they are rugged, reliable and economical. Single-phase induction motors are used extensively for smaller loads, such as household appliances like fans. Although traditionally used in fixed-speed service, induction motors are increasingly being used with variable-frequency drives (VFDs) in variable-speed service. VFDs offer especially important energy savings opportunities for existing and prospective induction motors in

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variable-torque centrifugal fan, pump and compressor load applications. Squirrel cage induction motors are very widely used in both fixed-speed and variable-frequency drive (VFD) applications. Variable voltage and variable frequency drives are also used in variable-speed service.In both induction and synchronous motors, the AC power supplied to the motor's stator creates a magnetic field that rotates in time with the AC oscillations. Whereas a synchronous motor's rotor turns at the same rate as the stator field, an induction motor's rotor rotates at a slower speed than the stator field. The induction motor stator's magnetic field is therefore changing or rotating relative to the rotor. This induces an opposing current in the induction motor's rotor, in effect the motor's secondary winding, when the latter is short-circuited or closed through external impedance. The rotating magnetic flux induces currents in the windings of the rotor; in a manner similar to currents induced in a transformer's secondary winding(s). The currents in the rotor windings in turn create magnetic fields in the rotor that react against the stator field. Due to Lenz's Law, the direction of the magnetic field created will be such as to oppose the change in current through the rotor windings. The cause of induced current in the rotor windings is the rotating stator magnetic field, so to oppose the change in rotor-winding currents the rotor will start to rotate in the direction of the rotating stator magnetic field. The rotor accelerates until the magnitude of induced rotor current and torque balances the applied load. Since rotation at synchronous speed would result in no induced rotor current, an induction motor always operates slower than synchronous speed. The difference, or "slip," between actual and synchronous speed varies from about 0.5 to 5.0% for standard Design B torque curve induction motors. The induction machine's essential character is that it is created solely by induction instead of being separately excited as in synchronous or DC machines or being self-magnetized as in permanent magnet motors.For rotor currents to be induced the speed of the physical rotor must be lower than that of the stator's rotating magnetic field (n_s); otherwise the magnetic field would not be moving relative to the rotor conductors and no currents would be induced. As the speed of the rotor drops below synchronous speed, the rotation rate of the magnetic field in the rotor increases, inducing more current in the windings and creating more torque. The ratio between the rotation rate of the magnetic field induced in the rotor and the rotation rate of the stator's rotating field is called slip. Under load, the speed drops and the slip increases enough to create sufficient torque to turn the load. For this reason, induction motors are sometimes referred to as asynchronous motors.[25] An induction motor can be used as an induction generator, or it can be unrolled to form a linear induction motor which can directly generate linear motion.

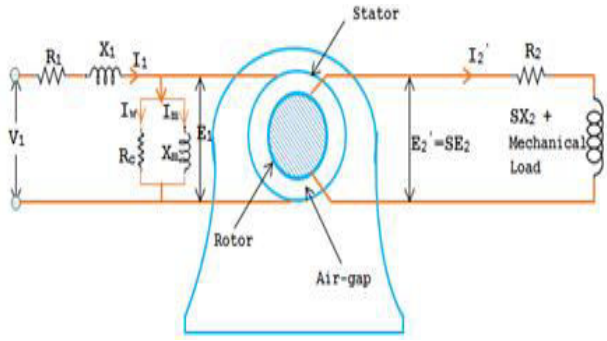

Fig.10. Equivalent circuit for Induction motor

Synchronous Speed:

The rotational speed of the rotating magnetic field is called as synchronous speed.

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$$Ns = \frac{120 \times f}{P} \quad (RPM) \qquad (51)$$

Where, f = frequency of the supply

P = number of poles

Slip:

Rotor tries to catch up the synchronous speed of the stator field, and hence it rotates. But in practice, rotor never succeeds in catching up. If rotor catches up the stator speed, there won't be any relative speed between the stator flux and the rotor, hence no induced rotor current and no torque production to maintain the rotation. However, this won't stop the motor, the rotor will slow down due to lost of torque, the torque will again be exerted due to relative speed. That is why the rotor rotates at speed which is always less the synchronous speed.The difference between the synchronous speed (Ns) and actual speed (N) of the rotor is called as slip.

$$\% \text{ slip } \quad s = \frac{Ns - N}{Ns} \times 100 \qquad (52)$$

VI. MATLAB/SIMULATION RESULTS

Case I : R Load Condition

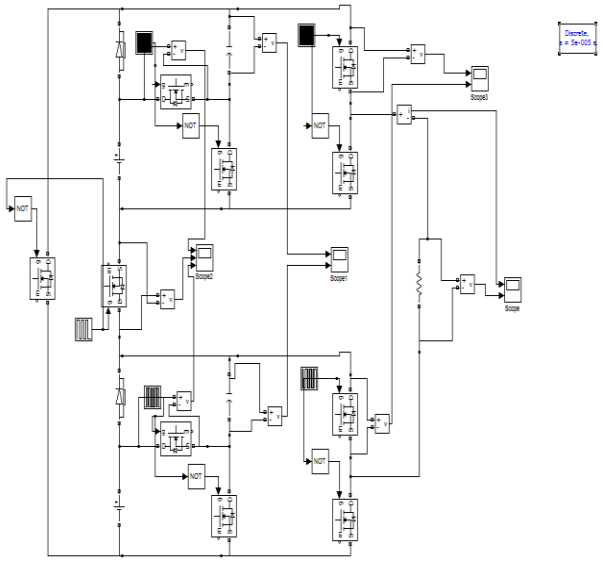

Fig.11.Matlab circuit for Proposed SMLI configuration with R Load

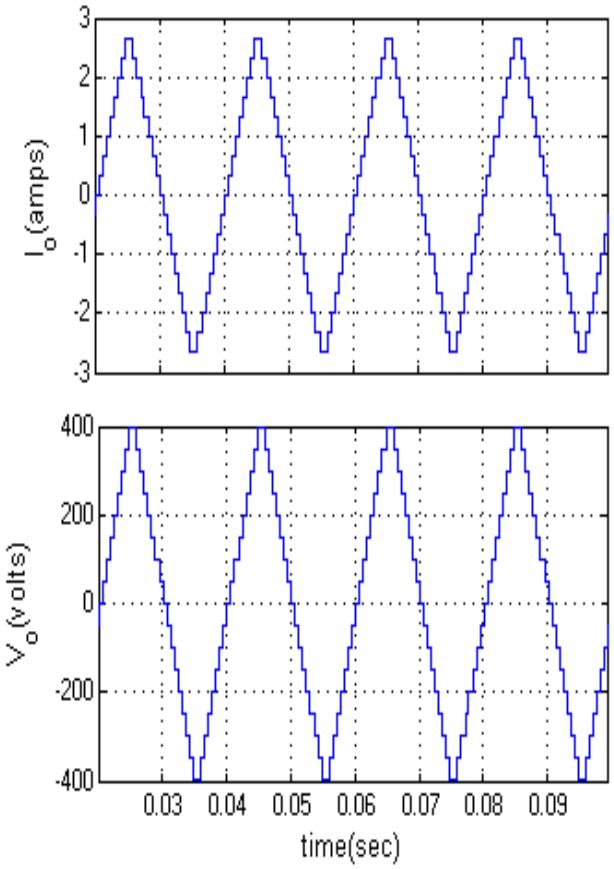

Fig.12. Simulation waveform for Rload current and voltage

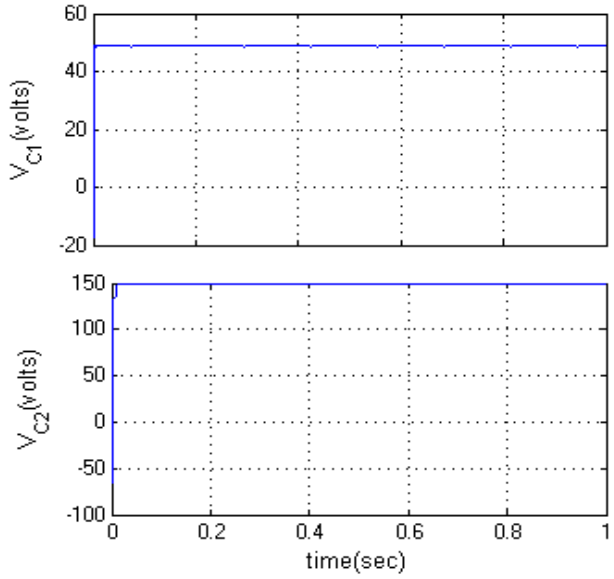

Fig.13. Simulation waveforms for Capacitors' voltage ripple waveforms R Load

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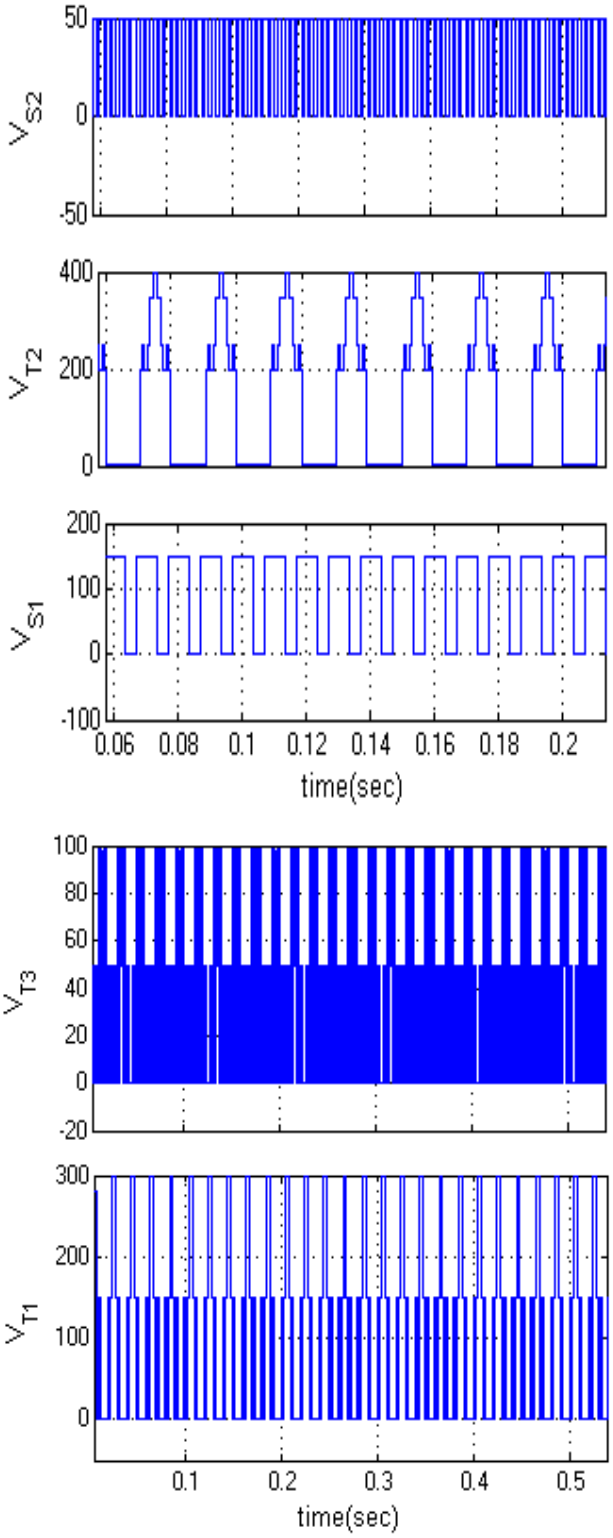

Fig.14. Simulation Voltage waveforms across switches at R Load

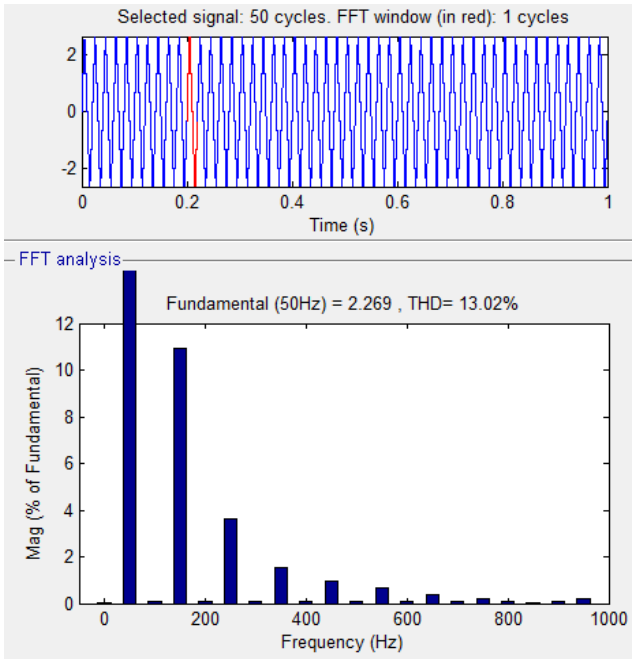

Fig.15. Simulation waveform of R Load THD

Case II : RL Load Condition

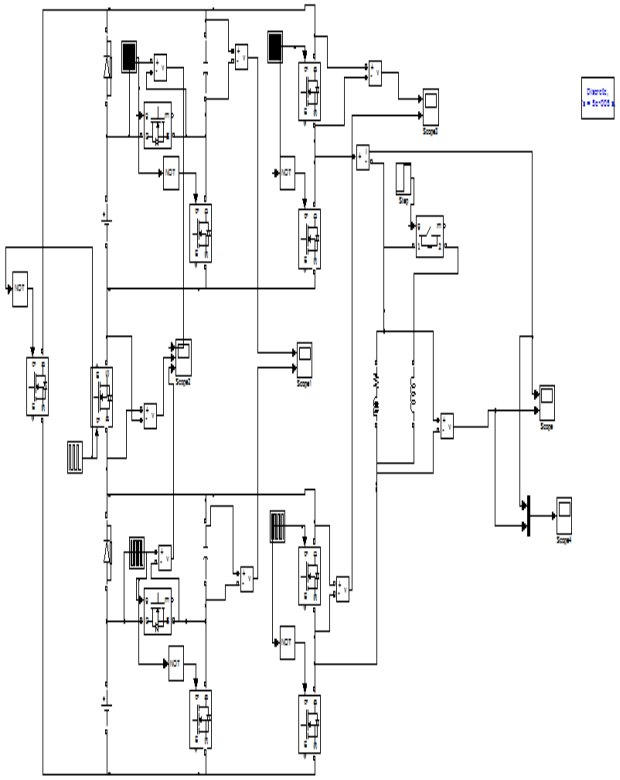

Fig.15.Matlab circuit for Proposed SMLI configuration with RL Load

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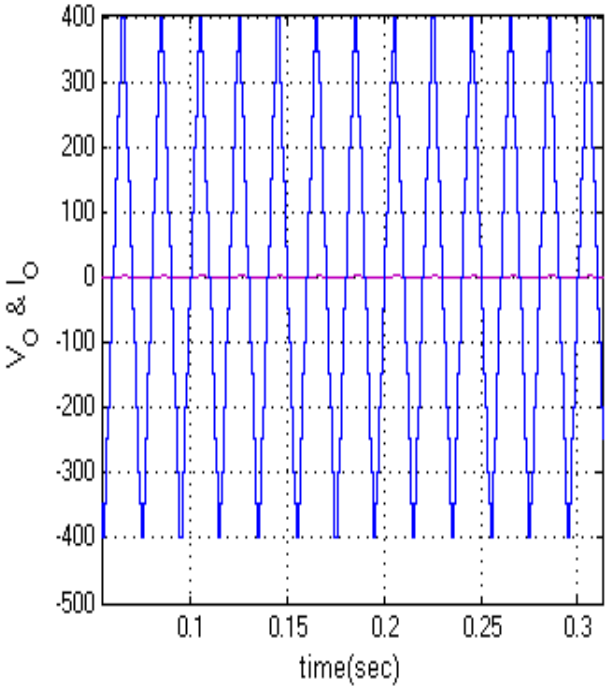


Fig.16. Current and voltage with RL Load

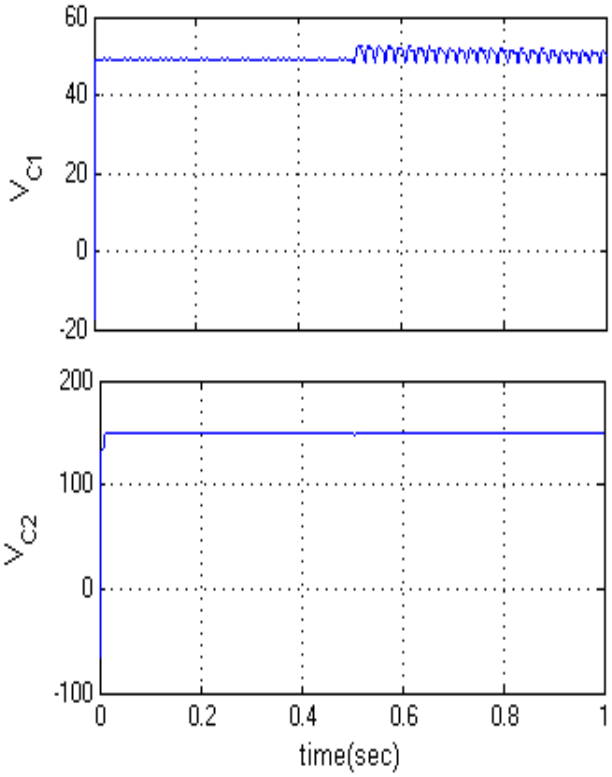
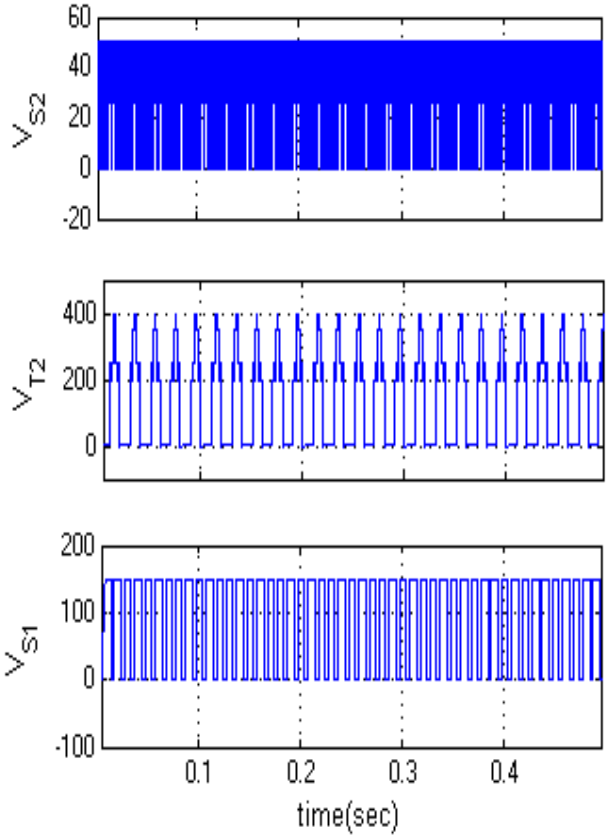


Fig.17. Simulation waveforms for Capacitors' voltage ripple waveforms RL Load



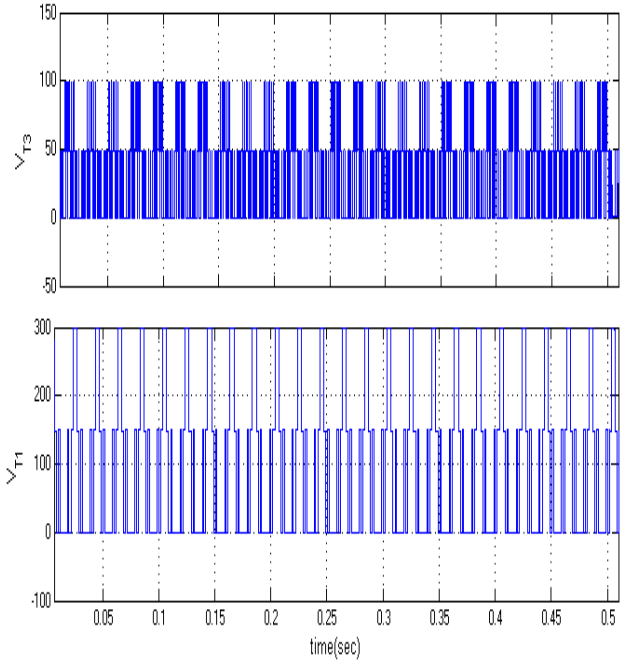


Fig.18.Simulation waveform of Switch voltages of RL Load

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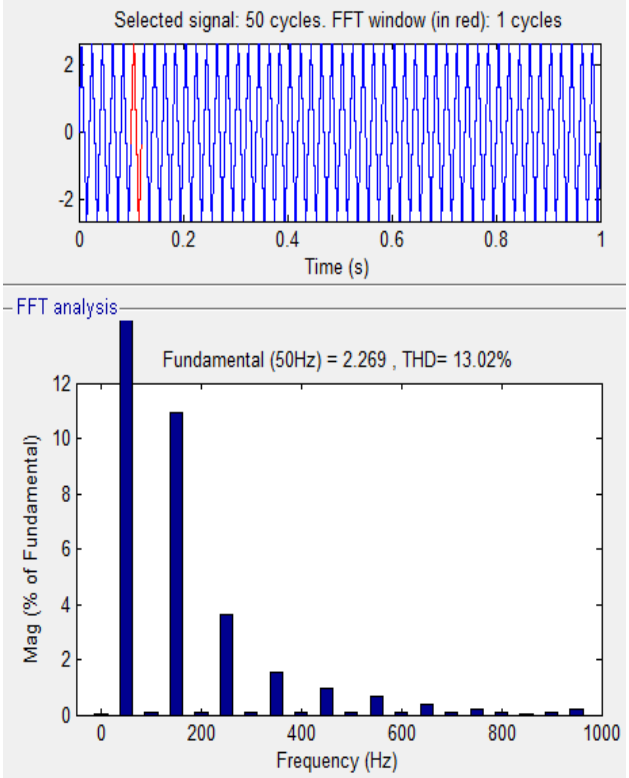

Fig.19.Simulation waveform of THD at RL LOAD

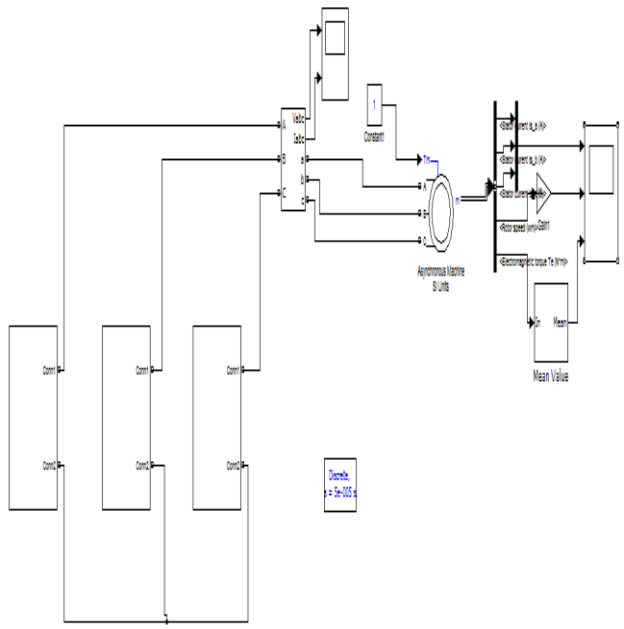

Fig.20.Matlab circuit for proposed SMLI configuration with R Load

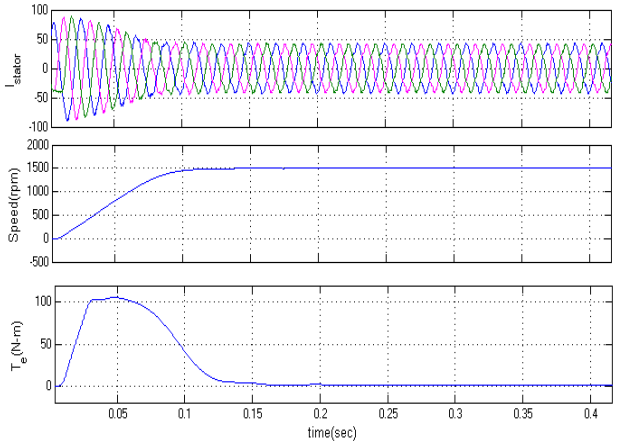

Fig.21.Simulation waveform of SMLI with R load stator current, Speed, Torque of Induction motor drive.

VII. CONCLUSION

In this Paper, a new reduced components' SCC topology was presented, which possesses boost capability remarkably and also can pass the reverse current for inductive loads through existing power switches. The voltage of all the capacitors in this structure is balanced by binary asymmetrical algorithm. And then new sub multilevel structure based on suggested SCC was proposed, which can generate all the voltage levels at the output (even and odd). In this case, the conventional output H-bridge cell used to convert the polarity of SCC units has been removed; therefore, number of required IGBTs and other involved components are decreased. After that, an optimizing operation was presented, which could obvious the number of required capacitors in each of SCC units that participate in the CSMLI to generate maximum number of output voltage levels with less number of elements. In this paper proposed topology is implemented with induction motor drive, the stator current, Speed and electromagnetic torque observed to be better on Matlab/Simulink software.

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