



COPY RIGHT

2017 IJIEMR. Personal use of this material is permitted. Permission from IJIEMR must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works. No Reprint should be done to this paper, all copy right is authenticated to Paper Authors

IJIEMR Transactions, online available on 9th November 2017. Link :

<http://www.ijiemr.org/downloads.php?vol=Volume-6&issue=ISSUE-10>

Title: A Three-Phase Series-Parallel Converted Cascaded Switched Capacitor Multilevel Inverter For Induction Motor Drive.

Volume 06, Issue 10, Page No: 161 – 174.

Paper Authors

***G.PRASHANTH, P.SRINIVAS RAJU.**

* Dept of EEE, Ellenki College of Engineering and Tenchnology.



USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per **UGC Guidelines** We Are Providing A Electronic Bar Code

A THREE-PHASE SERIES-PARALLEL CONVERTED CASCADED SWITCHED CAPACITOR MULTILEVEL INVERTER FOR INDUCTION MOTOR DRIVE

*G.PRASHANTH, ** P.SRINIVAS RAJU

*PG Scholar, Dept of EEE, Ellenki College of Engineering and Technology, Sangareddy (Dt); Telangana, India.

**Assistant Professor, Dept of EEE, Ellenki College of Engineering and Technology, Sangareddy (Dt); Telangana, India

prashanthg230@gmail.com

psr239@gmail.com

ABSTRACT-

Multilevel Inverter widely used in high power industrial applications. This paper presents a three-phase series-parallel converted cascaded multilevel inverter with switched capacitor component for induction motor drive. In traditional switched capacitor inverters required more number of components, it seem to more complex control circuitry and bulky. All over world concentrating to improve the efficiency of Multilevel Inverter such as voltage balancing, reduction in components, switched capacitor multilevel inverter methods etc. The Proposed multilevel inverter output voltage level increasing by using less number of switches driven by the multicarrier series-parallel techniques. In this paper presents generalized structure, Operation, comparison with other traditional topology; the aim of this paper is to present a new structure for switched-capacitor multilevel inverters (SCMLIs) which can generate a great number of voltage levels with optimum number of components for both symmetric and asymmetric values of dc-voltage sources. In this paper, initially, a new switched-capacitor dc/dc converter (SCC) is presented which can switch as conventional series/parallel conversion and generate multiple dc-link voltages with optimum components. In this case, voltage of all capacitors is filled by binary asymmetrical pattern without using any auxiliary circuits. That has boost ability and can charge capacitors as self-balancing by using the proposed binary asymmetrical algorithm and series-parallel conversion of power supply.

I INTRODUCTION

Multilevel inverters (MLIs) are known as one of the most popular solutions to improve the performance of renewable energy systems, electric vehicles (EVs), and other innovative power electronic utilities in medium and high power applications [1], [2]. These converters can generate a staircase voltage waveform at the output with high quality and desired spectrum. The desired output voltage is synthesized by appropriate switching of several dc-voltage links, which leads to decrease voltage stresses on switches and total harmonic distortion (THD) [3], [4].

In general, there are three conventional types of MLI configurations categorized into diode clamped (DCMLI) [5], flying capacitors (FCMLI) [6], [7], and cascade H-bridge (CHB)

topologies, which can be divided into two entire divisions based on symmetric and asymmetric values of dc power supplies [8]–[10].

Although these converters have a lot of advantages over the classic inverters, using aforementioned conventional topologies need more number of required power switches, power supplies, and large capacitor banks. Furthermore, voltage of the capacitors tends to be discharged theoretically and therefore charge balancing control processing is necessary. There have been several suggested charge balancing circuits to control the capacitors' voltage [11].

References [11]–[13] could regulate the duty cycle of dc bus capacitors for FCMLIs by

using the existing redundancy switching states (RSSs). In this case, the accuracy of the

+++

proposed approach depends on designing a closed-loop control system. Also, [14] presented a phase-shift modulation approach to obviate the discharging problem in a capacitor-based seven level CHB topology supplied by one dc-voltage source for main unit and one floating capacitor for auxiliary unit. Here, the main and auxiliary power switches have to drive by fundamental and high switching frequencies, respectively. Meanwhile, [15] presented a triplen harmonic compensatory method based on fundamental switching strategy to extend the range of modulation index for three-phase utility of seven-level CHB topology. Using the resonant switched-capacitor circuit (RSCC) as an external voltage balancing network can also prevent this problem for DCMLIs [16].

Nowadays, many researchers have presented numerous developed structures of MLIs with less number of key components, such as number of required switches, gate drivers, power supplies, and so on [18]–[20]. One of the most particular schemes of them is switched-capacitor multilevel inverters (SCMLIs). These converters can produce more output voltage levels with less number of required power supplies [21]–[24]. SCMLIs contain several capacitors and switches, which can connect dc power supply to ac output and are able to decrease the burden of power supply to achieve higher number of voltage levels.

Nevertheless, to attain the greater number of output voltage levels with less number of power semiconductors and simple commutation, a new type of SCMLIs have emerged using the series–parallel switching strategy (SCISPC) [25], [26]. The distinctive features of these types of inverters are that they can increase the flexibility of systems by switching between several capacitors in series or parallel modes and therefore can transfer more input power to the output. In this way, [27] and [28] presented a new family of cascade and hybrid SCISPC topologies that have a modular

structure and generate more output voltage levels with least of switches. But, such structures have used the full H-bridge units with

isolated dc-voltage sources to change the polarity of output voltage waveform, which makes more conducting loss through the current path components and increases the number of power switches.

In this project, initially, a new switched-capacitor dc/dc converter (SCC) is presented which can switch as conventional series/parallel conversion and generate multiple dc-link voltages with optimum components. In this case, voltage of all capacitors is filled by binary asymmetrical pattern without using any auxiliary circuits. At the next, a new sub multilevel inverter (SMLI) topology presents, which is performed based on the proposed SCC unit and without using the full H-bridge cell. In addition, this structure is suitable for an inductive load with the capability to pass the reverse current. After that, the proposed sub multilevel modules are cascaded with each other and create more output voltage levels. Therefore, most of the parameters such as number of required switches, diodes, maximum current path components, and value of total blocked or standing voltage are improved. In order to prove the performance of the proposed circuit, variety number of comparisons with other recently suggested topologies has been done in fair conditions and also analysis of theoretical power losses is given.

II. PROPOSED SCC

Fig.1 (a) shows the basic circuit of the proposed SCC. This circuit is named as basic unit and contains one dc power supply, one capacitor, one passive power diode, and two active power switches. Photovoltaic (PV) cells, batteries, and fuel cells can be used as a power supply in this structure. Fig.3.1(b) and (c) shows that how to carry out the charging and discharging operations for capacitor C. Switches Sa and Sb are used in series and parallel

conversions, respectively. As it can be inspected, when the switch S_b becomes ON, the capacitor C is charged to V_{dc} and when the switch S_a turns ON, the diode becomes reverse

output with the capability of passing the reverse current for inductive load and can be used as a part of inverters. Fig.3.2 shows the circuit configuration of the proposed converter. In

biased and capacitor is discharged. In this mode, the power supply's energy and stored energy of C are transferred to the output. It is obvious that, basic unit does not need any extra charge balancing control circuits and complicated commutation methods, which is counted as a great merit of this structure [28]. Also, it is remarkable that, the internal resistance of power diode and capacitor can damp the unequal voltage between capacitor and dc-voltage source during the charging operation, which leads to introduce an effective and practical power circuit.

order to charge all the capacitors and generate output voltage waveform, the switches S_{ai} ($i =$

$1, 2, \dots, n - 1$), S_{bi} , and S_{ci} ($i = 1, 2, \dots, n$) are driven by series/parallel conversion or combination of them.

In this case, switches S_{ci} are unidirectional power switches without antiparallel diode, which can pass the reverse inductive load current and other switches are also unidirectional with internal antiparallel diode. As figure shows, switches S_{ci} ($i = 2, 3, \dots, n$) can be substituted by ordinary power switches and a series diode to counteract the effect of internal antiparallel diode. Table I indicates the different switching and capacitors' states for the proposed SCC.

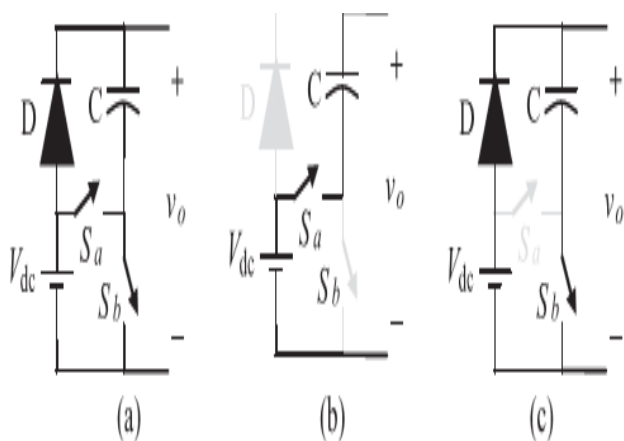


Fig.1 (a) Basic series/parallel unit. (b) Capacitor discharging mode. (c) Capacitor charging mode.

In this table, 0 and 1 mean OFF and ON switching state and C and D refer to charging and discharging modes for capacitors, respectively. In order to generate more number of output voltage levels with optimum number of components, all the capacitors should be charged by binary asymmetrical algorithm, according to this table in such a way that, in state (1) when switch $S_{c,1}$ becomes ON, capacitor C_1 is charged to V_{dc} and this voltage level is transferred to the output through $S_{a,i}$ ($i = 1, 2, \dots, n - 1$) simultaneously.

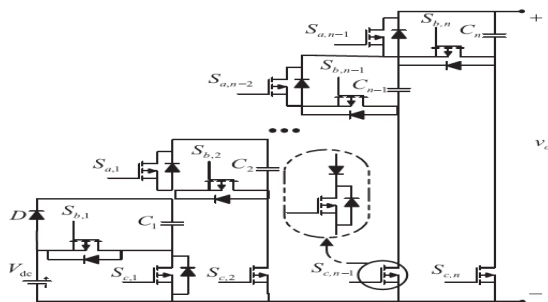


Fig.2. Proposed SCC

Also in state (2), C_2 is being charged to $V_{dc} + V_{c1}$ through switch $S_{c,2}$ and with discharging of C_1 , second voltage level generates at the output through $S_{a,i}$ and $S_{b,1}$, simultaneously, which is equal to $2V_{dc}$. After this moment, without entering other capacitors into the circuit, voltage level of $3V_{dc}$ can be transferred to the output by stored voltage of C_2 and constant dc-voltage source. In this moment, C_1 is again charged by dc-voltage source directly and for the next voltage level, this stored voltage besides the

The proposed dc/dc converter is made by extended connection of this basic unit. Then, a staircase voltage waveform is generated at the

across voltage of C2 and constant dc-voltage source are transferred to the output, which is equalized to 4Vdc and this consecutive operation continues so on.

TABLE 1

SWITCHING AND CAPACITORS STATES OF THE PROPOSED SCC

v_o	V_{dc}	$2V_{dc}$	$3V_{dc}$	$4V_{dc}$...	$2^n V_{dc}$	
Switching states	$S_{a,1}$	1	1	0	0	...	0
	$S_{a,2}$	1	1	1	1	...	0
	\vdots	1	1	1	1	...	0
	$S_{a,n-1}$	1	1	1	1	...	0
	$S_{h,1}$	0	1	0	1	...	1
	$S_{h,2}$	0	0	1	1	...	1
	\vdots	0	0	0	0	...	1
	$S_{h,n}$	0	0	0	0	...	1
	$S_{c,1}$	1	0	1	0	...	0
	$S_{c,2}$	0	1	0	0	...	0
	\vdots	0	0	0	0	...	0
	$S_{c,n}$	0	0	0	0	...	0
	Capacitors states	C_1	C	D	C	D	...
C_2		-	C	D	D	...	D
C_3		-	-	-	C	...	D
\vdots		\vdots	\vdots	\vdots	D
C_n		-	-	-	-	C	D

The prominent feature of the proposed circuit is that by entering the next capacitors into the circuit and also continuing the series-parallel switching strategy, the number of output voltage levels is enhanced as binary manner from Vdc to $2^n V_{dc}$.

It is important to note that, always at each of voltage steps, the pertinent capacitor of previous steps must be connected as parallel to keep on the charging operation. Therefore, if we assume the number of capacitors equal to n, the stored voltage of each capacitor would be equalized to

$$V_{C,k} = 2^{k-1} V_{dc}, \text{ for } k = 1, 2, \dots, n \quad (1)$$

Also from this table, it is obvious that, the proposed SCC is able to generate different

positive output voltage levels by self-balancing ability. Now, by considering the proposed overall structure (Fig.3.2), number of required switches ($N_{switch,u}$) or gate drivers ($N_{Driver,u}$), number of required isolated-gate bipolar transistors (IGBTs) ($N_{IGBT,u}$), power diodes ($N_{diode,u}$), and output voltage levels ($N_{level,u}$) are calculated by the following equations, respectively,

$$N_{switch,u} = N_{Driver,u} = N_{IGBT,u} = 3n - 1 \quad (2)$$

$$N_{diode,u} = n \quad (3)$$

$$N_{level,u} = 2^n \quad (4)$$

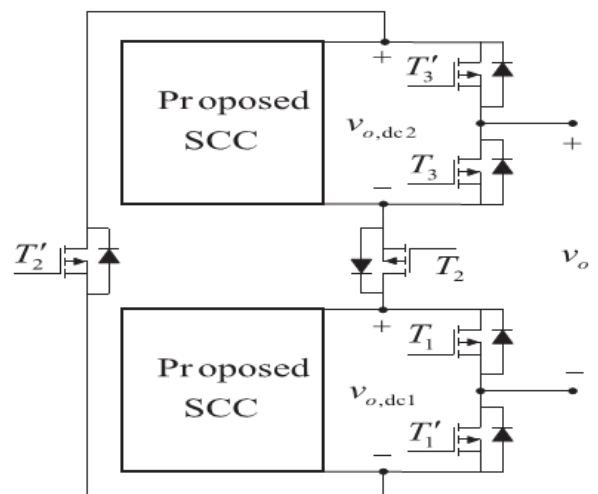


Fig. 3. Proposed SMLI configuration.

According to (4), the proposed circuit possesses an appropriate performance as boost capability. This factor can be defined as

$$\beta = \frac{V_{o,max,u}}{\sum V_{dc}} = 2^n \quad (5)$$

Moreover, this structure is able to mitigate the total blocked voltage. As it is clear, the value of blocked voltage should be tolerated by switches and means standing

voltage across of switches, which effects on conduction losses, efficiency, and cost [29]. In this case, the total blocked voltage is formulized by

$$V_{block,u} = [3(2^n - 1) - 1] V_{dc} \quad (6)$$

III. PROPOSED SMLI

As it was analyzed before, the proposed SCC generates output voltage waveform with positive polarity. Therefore, it is not suitable for inverter applications. In order to change the polarity and create an ac waveform, an H-bridge cell can be connected to the output similar to the other existing structures. However, this cell may increase the number of required IGBTs and the number of involved components in the current path. This project has not focused on added H-bridge cell and presents a new scheme of SCISP shown in Fig.3.3, based on two utilized half-bridges.

In order to convert the output polarity of SCC and create all the voltage levels (even and odd) at the output, this structure always requires a pair stage of SCC units. Therefore, the proposed SCISPC named as SMLI can produce positive, zero, and negative output voltage levels with six unidirectional power switches and two same units of SCC. As a result, 2n capacitors and two isolated dc power supplies are needed for this structure.

Now, the number of required IGBTs or gate drivers and the number of power diodes can be expressed as follows:

$$N_{IGBT,Sub} = N_{Driver,Sub} = 6n + 4 \quad (7)$$

$$N_{Diode,Sub} = 2n. \quad (8)$$

Table II indicates ON switching states of the proposed SMLI, which is summarized by seven different modes. According to this

table, to refrain from short-circuit problems, switches of

TABLE 2
SWITCHING PATTERN OF THE PROPOSED SMLI

		ON switches	v_o
Switching states	1	T'_1, T_2, T'_3	$v_{o,dc1} + v_{o,dc2}$
	2	T_1, T_2, T'_3	$v_{o,dc2}$
	3	T'_1, T_2, T_3	$v_{o,dc1}$
	4	T_1, T_2, T_3	0
		T'_1, T'_2, T'_3	
	5	T_1, T'_2, T'_3	$-v_{o,dc1}$
	6	T'_1, T'_2, T_3	$-v_{o,dc2}$
7	T_1, T_2, T'_3	$-v_{o,dc1} - v_{o,dc2}$	

(T1, T'1), (T2, T'2), and (T3, T'3), are triggered as complementary operation with each others and should not to be ON simultaneously. Also, this structure can work on symmetric and asymmetric values of dc-voltage sources. In symmetric structure, all

the dc sources are equal and that are different in asymmetric topology. Then, by considering (1), to obtain the maximum number of voltage levels from asymmetric condition, the value of other isolated dc power supply should conform the following expression:

$$V_{dc,2} = (1 + 2^n)V_{dc,1} \quad (9)$$

TABLE 3
DIFFERENT RELATED EQUATIONS FOR THE PROPOSED SMLI TOPOLOGY

Parameters	Symmetric	Asymmetric
N_{level_Sub}	$1 + 2^{n+2}$ (11)	$1 + 2^{n+2} + 2^{2n+1}$ (14)
V_{o,max_Sub}	$2^{n+1}V_{dc}$ (12)	$[2^{n+1} + 2^{2n}]V_{dc}$ (15)
V_{block_Sub}	$2\sum_{j=1}^3 V_{block,j} + \sum_{j=1}^2 V_{block,ij}$ (13) $= [(7 \times 2^{n+1}) - 8]V_{dc}$	$2\sum_{j=1}^3 V_{block,j} + \sum_{j=1}^2 V_{block,ij}$ (16) $= [2^{2n+2} + 2^{n+3}]V_{dc}$

Table 3 indicates the pertinent equations of N_{level_Sub} , $v_{o,maxSub}$, and $V_{Blocked_Sub}$ for symmetric and asymmetric forms in the proposed SMLI. In this case, the asymmetric calculations in Table 3 are done by considering (9).

To achieve the greater number of voltage levels, the proposed SMLI can be extended by increasing the number of output voltage levels for the proposed SCC. But, this way yields some identical restrictions due to increase in the voltage drop and existed spikes across each of capacitors especially in high power ratio. To avoid this constraint, the best solution to increase the number of voltage levels is considered by series connection of the proposed SMLIs with each other shown as proposed cascaded sub multilevel inverter (CSMLI) in Fig.3.4. In this figure, number of cascaded SMLI units is indexed by m. As a result, output voltage of the proposed CSMLI is obtained by

$$v_o(t) = v_{o,1}(t) + v_{o,2}(t) + \dots + v_{o,m}(t) \quad (10)$$

It should be noted that, in this case, the number of capacitors that have been used in each of SCCs is assumed same. To reduce the cost, weight, total blocked voltage, and some other identical problems, the required capacitors for each of the proposed SCC units (n) is optimized.

IV PROPOSED IMPROVED CSMLI

The number of required capacitors in each of the proposed SMLI units is optimized from the view point of maximum produced output voltage levels for the proposed CSMLI with minimum number of IGBTs. This optimization is done based on asymmetric value of dc sources according to (9).

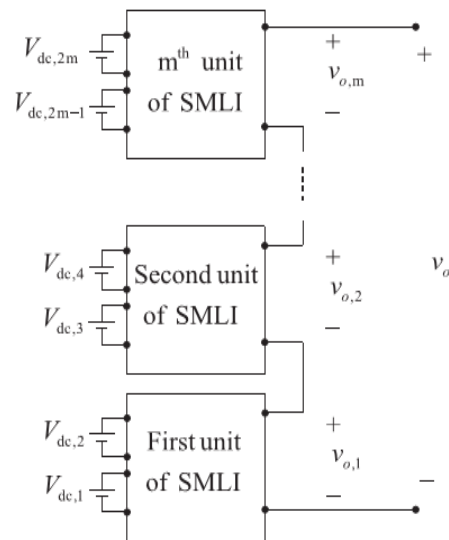


Fig.4. Proposed CSMLI

In general, the number of output voltage levels for the proposed CSMLI is obtained by

$$N_{level} = \left(N_{level_Sub} \right)^m \quad (17)$$

where N_{level_Sub} is the number of output voltage levels for the proposed SMLI, which

is calculated by (14). Then, (17) can be rewritten as

$$N_{\text{level}} = (2^{n+2} + 2^{2n+1} + 1)^m \quad (18)$$

On the other hand, the relation of m in terms of NIGBT (number of required IGBTs for the proposed CSMLI) and $N_{\text{Sub}}^{\text{NIGBT}}$ is equalized to the following equation:

$$m = \frac{N_{\text{IGBT}}}{N_{\text{Sub}}^{\text{NIGBT}}} \quad (19)$$

Also, by inserting (13) into (18) and (19),

$$N_{\text{level}} = (2^{n+2} + 2^{2n+1} + 1)^{\frac{N_{\text{IGBT}}}{6n+4}} \quad (20)$$

In order to obtain the optimal number of capacitor from each of SMLIs, the variation of Nlevel against NIGBT for specific number of n , is curved according to (20) and illustrated by Fig.3.5. As this figure shows, for a constant value of NIGBT, Nlevel has been maximized when one capacitor is being used. Therefore, with respect to $n = 1$, number of output voltage levels, required IGBTs, power diodes, and total value of blocked

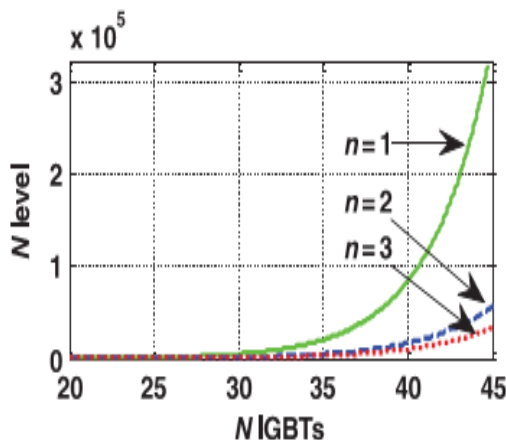


Fig. 5. Variation of N_{level} against N_{IGBT} for different values of n .

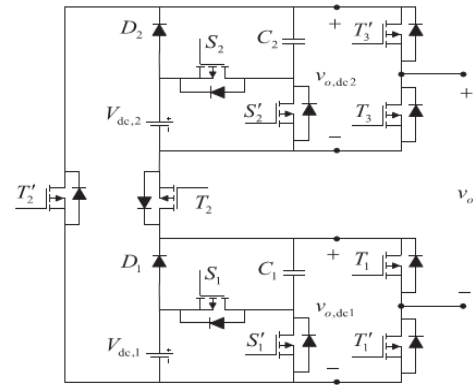


Fig 6. Proposed 17-level structure

Voltage for the proposed improved CSMLI are obtained for both symmetric and asymmetric conditions and are summarized in Table IV. In addition, based on (9), the value of dc-voltage sources in i th unit of the proposed CSMLI should be adopted by

$$V_{dc2,i} = 3V_{dc1,i} = 3(17^{i-1})V_{dc}, \quad i = 1, 2, \dots, m \quad (21)$$

Fig.3.6 shows an improved CSMLI configuration by considering $m = 1$, which leads to generate 17-level output voltage based on the proposed asymmetric topology. In this circuit, the values of dc isolated power supplies are set on V_{dc} and $3V_{dc}$ according to (9). Table V shows the switching pattern of the proposed 17-level inverter.

In this case, all the switches are driven by fundamental switching frequency, whereas the sinusoidal reference voltage is compared with some available dc-voltage levels and create the related gate switching pulses. The most advantage of this switching method is referred to low switching frequency that yields to the reduction of switching loss [29], [30].

Details of fundamental switching modulation strategy are not the objective of this paper. In addition from Table 3.5, it is clear that, to generate each of the output voltage levels, only five switches are being involved in the current path.

At this stage, to determine the capacitance of C1 and C2, two assumptions are considered in which one is related to the output sinusoidal load current with phase difference between output voltage and current (ϕ) and the other is contributed to the same duration in each step of staircase output voltage.

Thus, the maximum discharging amount of each capacitor can be defined as (30) in one half-cycles

TABLE.4
DIFFERENT RELATED CALCULATIONS OF THE PROPOSED IMPROVED CSMLI

Parameters	Symmetric	Asymmetric
N_{level}	$8m+1$ (22)	17^m (25)
$V_{o,max}$	$4mV_{dc}$ (23)	$\frac{17^m-1}{2}$ (26)
V_{block}	$m \times [2 \sum_{j=1}^3 V_{block,j} + \sum_{j=1}^2 V_{block,up}]$ $= 20mV_{dc}$ (24)	$\sum_{k=1}^m (2 \sum_{j=1}^3 V_{block,j,k} + \sum_{j=1}^2 V_{block,up,k})$ $= \frac{5(17^m-1)}{2}$ (27)
N_{IGBT}	$10m$ (28)	
N_{Diode}	$2m$ (29)	

TABLE 5
DIFFERENT SWITCHING AND CAPACITORS STATES OF THE PROPOSED 17-LEVEL INVERTER

	ON switches	v_o	C_1	C_2	
Switching states	1	$T'_1, T_2, T'_3, S'_1, S_2$	$4V_{dc} + v_{c,1} + v_{c,2}$	D	D
	2	$T'_1, T_2, T'_3, S'_1, S_2$	$4V_{dc} + v_{c,2}$	C	D
	3	$T_1, T_2, T'_3, S'_1, S_2$	$3V_{dc} + v_{c,2}$	C	D
	4	$T'_1, T_2, T'_3, S'_1, S_2$	$4V_{dc} + v_{c,1}$	D	C
	5	$T'_1, T_2, T'_3, S'_1, S_2$	$4V_{dc}$	C	C
	6	$T_1, T_2, T'_3, S'_1, S_2$	$3V_{dc}$	C	C
	7	$T'_1, T_2, T_3, S'_1, S_2$	$V_{dc} + v_{c,1}$	D	C
	8	$T'_1, T_2, T_3, S'_1, S_2$	V_{dc}	C	C
	9	T_1, T_2, T_3, S'_1, S_2	0	C	C
		$T'_1, T'_2, T'_3, S'_1, S'_2$			
	10	$T_1, T_2, T'_3, S'_1, S_2$	$-V_{dc}$	C	C
	11	$T_1, T_2, T'_3, S'_1, S_2$	$-V_{dc} - v_{c,1}$	D	C
	12	$T'_1, T_2, T_3, S'_1, S_2$	$-3V_{dc}$	C	C
	13	T_1, T_2, T_3, S'_1, S_2	$-4V_{dc}$	C	C
	14	T_1, T_2, T_3, S'_1, S_2	$-4V_{dc} - v_{c,1}$	D	C
	15	$T'_1, T_2, T_3, S'_1, S_2$	$-3V_{dc} - v_{c,2}$	C	D
	16	T_1, T_2, T_3, S'_1, S_2	$-4V_{dc} - v_{c,2}$	C	D
17	T_1, T_2, T_3, S'_1, S_2	$-4V_{dc} - v_{c,1} - v_{c,2}$	D	D	

$$Q_{Ci} = \int_{t_j}^{\frac{T}{4} - t_j} I_{out} \sin(2\pi f_s t - \varphi) dt, \quad i = 1, 2 \quad (30)$$

where T , f_s , and I_{out} are the period of one cycle, frequency of output voltage, and amplitude of load current, respectively, and

also $[t_j, \frac{T}{4} - t_j]_{is}$ is the time interval corresponded to the longest discharging cycle (LDC) of each capacitor. On the other hand, in the proposed 17-level inverter, this time interval varies for C1 and C2. According to Table 3.5, the LDC for C1 and C2 is illustrated by Fig.3.7. Thus, by considering the kV_{in} as maximum allowable voltage ripple, the optimum value of capacitors can be taken by

$$C_{opt,i} \geq \frac{Q_{Ci}}{kV_{in}}, \quad i = 1, 2. \quad (31)$$

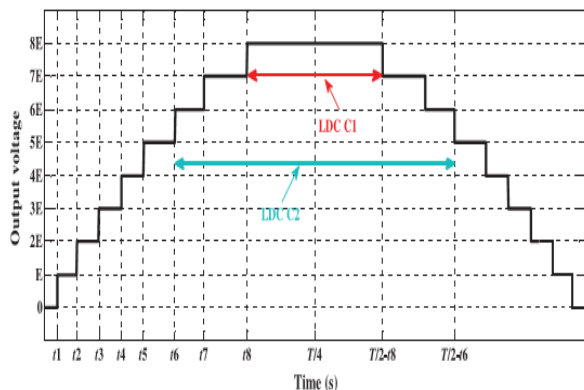


Fig.7. Typical output voltage waveform of 17-level inverter for positive half-cycle.

V POWER LOSS ANALYSIS

Theoretical total power losses and overall efficiency of the proposed improved CSMLI based on ($m = 1$) are calculated. For this kind of converters, always three major types of associated losses should be considered, which include: switching losses (P_{sw}), conduction losses of semiconductor devices (P_{Con}), and ripple losses of two utilized capacitors (P_{Rip}). All calculations are done based on the fundamental switching frequency strategy [29].

Switching Losses

Switching loss occurs during the ON and OFF period of switching states. For simplicity, a linear approximation between voltage and current of switches in the switching period is considered. Based on this

assumption, the following equations can be expressed for i th involved power switch:

$$\begin{aligned}
 P_{sw,on,i} &= f_{sw} \int_0^{t_{ON}} v_{ON,i}(t) i(t) dt \\
 &= f_{sw} \int_0^{t_{ON}} \left(\frac{V_{ON,i}}{t_{ON}} t \right) \left(-\frac{I_i}{t_{ON}} (t - t_{ON}) \right) dt \\
 &= \frac{1}{6} f_{sw} V_{ON,i} I_i t_{ON}
 \end{aligned}
 \tag{32}$$

$$\begin{aligned}
 P_{sw,off,i} &= f_{sw} \int_0^{t_{OFF}} v_{block,i}(t) i(t) dt \\
 &= f_{sw} \int_0^{t_{OFF}} \left(\frac{V_{block,i}}{t_{OFF}} t \right) \left(-\frac{I'_i}{t_{OFF}} (t - t_{OFF}) \right) dt \\
 &= \frac{1}{6} f_{sw} V_{block,i} I'_i t_{OFF}
 \end{aligned}
 \tag{33}$$

where I_i and I'_i are the currents that pass through i th power switch after turning ON and before turning OFF, respectively, and f_{sw} is the switching frequency equalized to the reference frequency. In order to calculate the total switching loss, the number of ON (N_{ON}) and the number of OFF (N_{OFF}) switching states per one cycle should be multiplied by (32) and (33) according to the following:

$$P_{sw} = \sum_{i=1}^{10} \left(\sum_{k=1}^{N_{ON}} P_{sw,ON,ik} + \sum_{k=1}^{N_{OFF}} P_{sw,OFF,ik} \right)
 \tag{34}$$

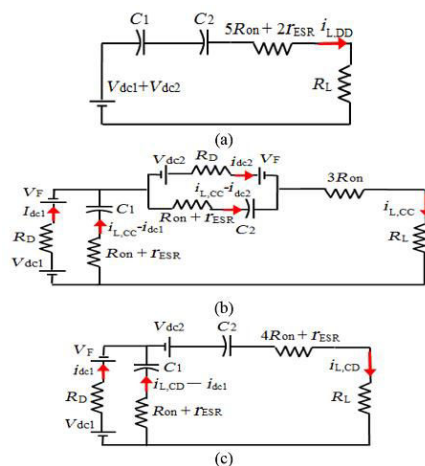


Fig. 8. Equivalent circuit of the proposed 17-level structure with a resistive load in (a) discharging modes, (b) charging modes, and (c) combination of charging and discharging modes.

Conduction Losses

To calculate the total conduction losses of each component, a straightforward method based on pure-resistance load is presented. Regarding Table V, three possible operating modes can be investigated including discharging states for both capacitors (states number of 1 and 17),

charging states for both capacitors (states number of 5, 6, 8, 10, 12, and 13), and discharging states for one capacitor and charging states for another one or vice versa (other remaining states).

Fig.3.8(a)–(c) demonstrates the equivalent circuits of charging and discharging operating modes for capacitors. In these figures, R_{on} , R_D , r_{ESR} , R_L , and V_F are the internal ON-state resistance of each switch, internal resistance of each diode, equivalent series resistance (ESR) of each capacitor, load resistance, and the forward voltage drop of each incurred diode, respectively.

According to Fig.3.8(a) during the series connection of capacitors to the respective dc-voltage sources, the value of load current can be written as

$$i_{L,DD} = \frac{4V_{dc} + v_{c,1} + v_{c,2}}{5R_{ON} + 2r_{ESR} + R_L} \quad (35)$$

Therefore, the instantaneous conduction loss ($p_{c,DD}$) and average conduction loss ($\overline{p_{c,DD}}$) for one full cycle of discharging mode with respect to the time intervals of Fig.3.7 and Table V, can be calculated as follows:

$$p_{c,DD} = (5R_{ON} + 2r_{ESR})i_{L,DD}^2 \quad (36)$$

$$\overline{p_{c,DD}} = \frac{2f_{sw}}{\pi} \left(\frac{\pi}{2} - t_8 \right) p_{c,DD} \quad (37)$$

Also, with respect to Fig.3.8(b) and by considering the time intervals between states of 3 and 5 and also states of 1 and 2 in Fig.3.7, the instantaneous and average value of conduction losses for charging modes of both capacitors ($p_{c,CC}$ and $p_{c,CD}$), are driven by the following equations, respectively,

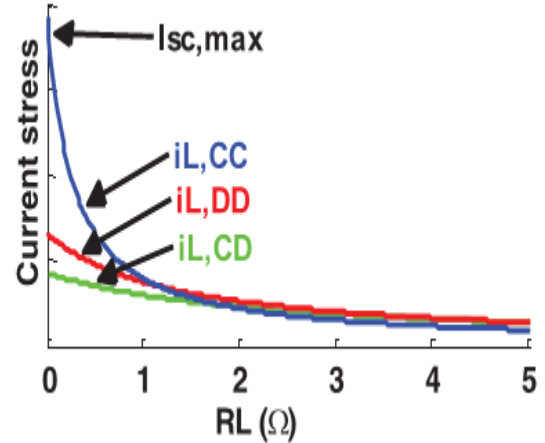


Fig.9. Variation of current stresses versus R_L in three defined modes

$$p_{c,CC} = 3R_{ON}i_{L,CC}^2 + R_D(i_{dc,1}^2 + i_{dc,2}^2) + (R_{ON} + r_{ESR}) \left[(i_{L,CC} - i_{dc,1})^2 + (i_{L,CC} - i_{dc,2})^2 \right] \quad (38)$$

$$\overline{p_{c,CC}} = \frac{2f_{sw}}{\pi} [(t_5 - t_3) + (t_2 - t_1)] p_{c,CC} \quad (39)$$

where $i_{dc,1}$ and $i_{dc,2}$ can be calculated by using the Kirchhoff voltage law (KVL) according to following, respectively,

$$i_{dc,1} = \frac{(r_{ESR} + R_{ON})i_{L,CC} + V_{dc} - v_{c,1} - V_F}{R_D + r_{ESR} + R_{ON}} \quad (40)$$

$$i_{dc,2} = \frac{(r_{ESR} + R_{ON})i_{L,CC} + 3V_{dc} - v_{c,2} - V_F}{R_D + r_{ESR} + R_{ON}} \quad (41)$$

In addition, by taking Figs.3.8(c) and 7 into account, when the capacitor of C1(C2) is

charged (discharged) and C2(C1) is discharged (charged), the instantaneous and average conduction losses can be expressed as follows, respectively,

$$P_{c,CD,i} = (4R_{ON} + r_{ESR})i_{c,CD}^2 + R_D i_{dc,i}^2 \quad \text{for } i = 1, 2 \\ + (R_{ON} + r_{ESR})(i_{c,CD} - i_{dc,i})^2 \quad (42)$$

$$\overline{P_{c,CD}} = \frac{2f_{sw}}{\pi} [[(t_8 - t_6)] p_{c,CD,2} + [(t_6 - t_5) \\ + (t_3 - t_2)] p_{c,CD,1}] \quad (43)$$

As a result, the total value of conduction losses (PCon) in one full cycle can be summarized by the following:

$$P_{Con} = \overline{P_{c,DD}} + \overline{P_{c,CC}} + \overline{P_{c,CD}} \quad (44)$$

Fig.3.9 shows the variation of load current stresses versus load resistance. As it can be found, the maximum value of short circuit current ($i_{sc,max}$) occurs in the charging mode operation ($i_{L,CC}$) and therefore this value must be tolerated by incurred components among the three defined modes.

Ripple Losses

When the capacitors are connected in parallel for charging operation, the ripple losses occur by the difference between the respective input voltage and the across voltage of capacitors ($v_{c,i}(i = 1, 2)$) [25]. Therefore, the ripple voltage of capacitors (ΔV_{Ci}) is taken from

$$\Delta V_{Ci} = \frac{1}{C_i} \int_{t^t} i_{c_i}(t) dt \quad (45)$$

where $i_{c_i}(t)$ is the passing current of capacitor and $[T' - t]$ is that the time interval for charging modes, which can be attained by regarding Table V. Thus, the total value of ripple loss, for one full cycle of output waveform is equalized to the following equation:

$$P_{Rip} = \frac{f_{sw}}{2} \sum_{i=1}^2 C_i \Delta V_{Ci}^2 \quad (46)$$

From (45) and (46), it is clear that, PRip is inversely proportional to the capacitance C_i , which means larger capacitance contributes to higher value of the overall efficiency.

Moreover, based on the above analysis, in order to design the proposed converter, two main identical restrictions must be considered, which are expressed as follows:

$$I_{out,max} \leq \frac{i_{sc,max}}{\lambda} \quad (47)$$

$$V_{out,max} \leq \frac{V_{Block}}{\lambda} \quad (48)$$

where λ , $V_{out,max}$, and $I_{out,max}$ are a safety coefficient, maximum value of output voltage, and current, respectively. Therefore, with respect to (47) and (48), the maximum value of output power ($P_{out,max}$) can be expressed as

$$P_{out,max} \leq \frac{V_{Block} i_{sc,max}}{\lambda^2} \quad (49)$$

Finally, the overall efficiency of the proposed improved CSMLI can be defined by the following:

$$\eta = \frac{P_{out}}{P_{out} + P_{sw} + P_{Con} + P_{Rip}} \quad (50)$$

VI. INDUCTION MOTOR (IM)

An induction motor is an example of asynchronous AC machine, which consists of a stator and a rotor. This motor is widely used because of its strong features and reasonable cost. A sinusoidal voltage is applied to the

stator, in the induction motor, which results in an induced electromagnetic field. A current in the rotor is induced due to this field, which creates another field that tries to align with

the stator field, causing the rotor to spin. A slip is created between these fields, when a load is applied to the motor. Compared to the synchronous speed, the rotor speed decreases, at higher slip values. The frequency of the stator voltage controls the synchronous speed. The frequency of the voltage is applied to the stator through power electronic devices, which allows the control of the speed of the motor. The research is using techniques, which implement a constant voltage to frequency ratio. Finally, the torque begins to fall when the motor reaches the synchronous speed. Thus, induction motor synchronous speed is defined by following equation,

$$n_s = \frac{120f}{P}$$

Where f is the frequency of AC supply, n, is the speed of rotor; p is the number of poles per phase of the motor. By varying the frequency of control circuit through AC supply, the rotor speed will change.

Control Strategy of Induction Motor

Power electronics interface such as three-phase SPWM inverter using constant closed loop Volts / Hertz control scheme is used to control the motor. According to the desired output speed, the amplitude and frequency of the reference (sinusoidal) signals will change. In order to maintain constant magnetic flux in the motor, the ratio of the voltage amplitude to voltage frequency will be kept constant. Hence a closed loop Proportional Integral (PI) controller is implemented to regulate the motor speed to the desired set point. The closed loop speed control is characterized by the measurement of the actual motor speed, which is compared to the reference speed while the error signal is generated. The magnitude and polarity of the error signal correspond to the difference between the actual and required speed. The PI controller

generates the corrected motor stator frequency to compensate for the error, based on the speed error.

VII MATLAB/SIMULINK RESULTS

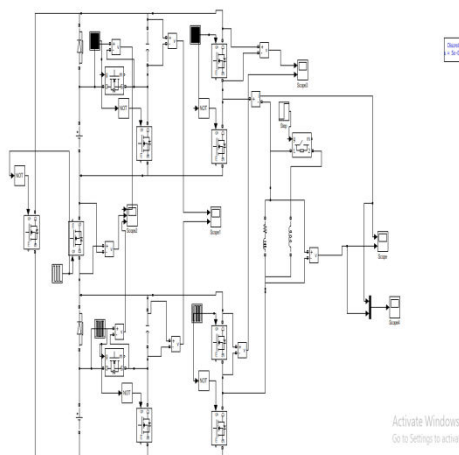


Fig 10 Simulation circuit of MLI 17-level

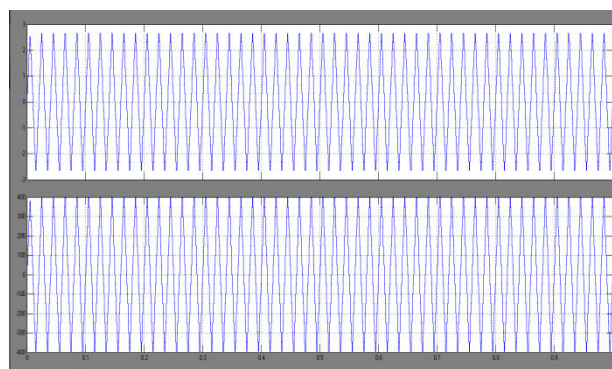


Fig 11 simulation wave form of 17-level output voltage and current

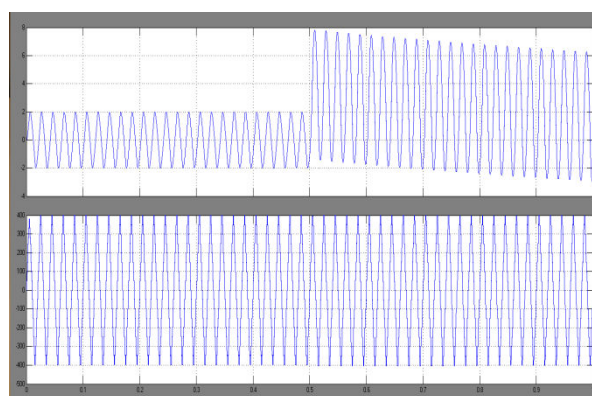


Fig 12 simulation wave form of 17-level output voltage and current with RL-load

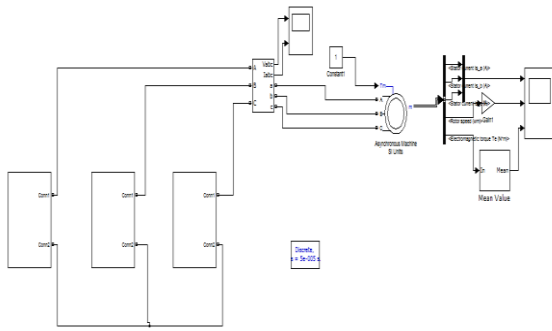


Fig 13 Simulation circuit of MLI 17-level three phase Inductions motor



Fig 14 Simulation wave form of output voltage and current

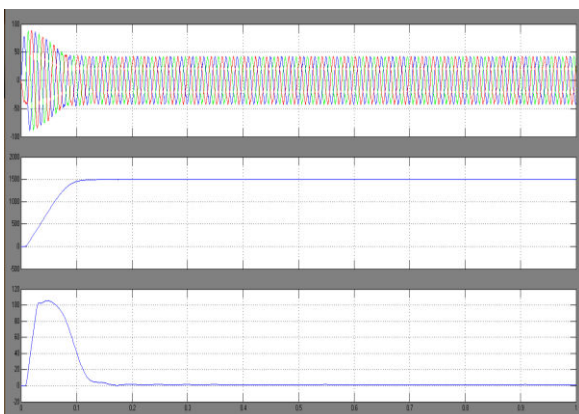


Fig 15 Simulation wave form of induction motor current, speed, torque

CONCLUSION

In this project, at the first, a new reduced components' SCC topology was presented, which possesses boost capability remarkably and also can pass the reverse current for inductive loads through existing power switches. The voltage of

all the capacitors in this structure is balanced by binary asymmetrical algorithm. Next, a new sub multilevel structure based on suggested SCC was proposed, which can generate all the voltage levels at the output (even and odd). In this case, the conventional output H-bridge cell used to convert the polarity of SCC units has been removed; therefore, number of required IGBTs and other involved components are decreased. After that, an optimizing operation was presented, which could obvious the number of required capacitors in each of SCC units that participate in the CSMLI to generate maximum number of output voltage levels with less number of elements. Moreover, comprehensive comparisons were given, which prove the differences between improved symmetric and asymmetric CSMLIs in contrast to some of the recently presented topologies in variety of aspects. The proposed system is three phase Induction Motor performance and characteristics we are studied

REFERENCES

- [1] J. Chavarria, D. Biel, F. Guinjoan, C. Meza, and J. J. Negroni, "Energy balance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMs," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 98–111, Jan. 2013.
- [2] G. Buticchi, E. Lorenzani, and G. Franceschini, "A five-level single-phase grid-connected converter for renewable distributed systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 906–918, Mar. 2013.
- [3] J. Rodriguez, L. J. Sheng, and P. Fang Zheng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [4] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.
- [5] M. M. Renge and H. M. Suryawanshi, "Five-level diode clamped inverter to

eliminate common mode voltage and reduce dv/dt in medium voltage rating induction

motor drives," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1598–1607, Jul. 2008.

[6] B. P. McGrath and D. G. Holmes, "Analytical modeling of voltage balance dynamics for a flying capacitor multilevel converter," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 543–550, Mar. 2008.

[7] J. Huang and K. A. Corzine, "Extended operation of flying capacitor multilevel inverters," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 140–147, Jan. 2006.

[8] K. K. Gupta and S. Jain, "Comprehensive review of a recently proposed multilevel inverter," *IET Power Electron.*, vol. 7, no. 3, pp. 467–479, 2014.

[9] A. Ajami, M. R. J. Oskuee, A. Mokhberdoran, and A. Van den Bossche, "Developed cascaded multilevel inverter topology to minimize the number of circuit devices and voltage stresses of switches," *IET Power Electron.*, vol. 7, no. 2, pp. 459–466, Feb. 2014.

[10] K. N. V. Prasad, G. R. Kumar, T. V. Kiran, and G. S. Narayana, "Comparison of different topologies of cascaded H-bridge multilevel inverter," in *Proc. Int. Comput. Commun. Informat. (ICCCI'13)*, Odisha, India, 2013, pp. 1–6.

[11] K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage balancing and fluctuation suppression methods of floating capacitors in a new modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1943–1954, May 2013.

[12] M. Khazraei, H. Sepahvand, K. A. Corzine, and M. Ferdowsi, "Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 769–778, Feb. 2012.

[13] M. Khazraei, H. Sepahvand, M. Ferdowsi, and K. A. Corzine, "Hysteresis based control of a single-phase multilevel flying capacitor active rectifier," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 154–164, Jan. 2013.

[14] H. Sepahvand, J. Liao, M. Ferdowsi, and K. Corzine, "Capacitor voltage regulation in single dc source cascade H-bridge multilevel converters using phase shift modulation," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3619–3626, Sep. 2013.

[15] Z. Du, L. M. Tolbert, B. Ozpineci, and J. N. Chiasson, "Fundamental frequency switching strategies of a seven-level hybrid cascaded H-bridge multilevel inverter," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 25–33, Jan. 2009