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INTELLIGENT SYSTEMS FOR ANALOG CIRCUIT DESIGN AUTOMATION

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ABSTRACT:

Analog circuits play an important role in modern electronic systems as they are irreplaceable to interact with the outside and analog world. More and more new products are based on analog circuits to improve speed and reduce energy consumption. Although the design of analog circuits has begun four decades ago, it is still in its infancy with the automation of digital design. Given the challenges of analog design problems and the low presence of analog design engineers, there are strong renewed economic pressures to develop new techniques to automate the analog design process. Many of these techniques have been based on intelligent systems such as simulation of annealing, fuzzy logic, neural networks and evolutionary calculus. This document provides an overview of intelligent system techniques for automating analog circuit design and analyzes possible future research work.

Keywords: analog design automation, optimization, fuzzy logic, neural networks, simulated annealing, evolutionary computation.

I INTRODUCTION

In recent trends the concept of system-on-chip(SoC) have become an important segment in the market of integrated circuits(IC). These developments have increased not only the number of devices and the functionality that can be put on a chip, but the chip now includes both digital and analog circuits. Generally, the digital parts account for about 90% of an integrated circuit while only 10% is analog. Trend is to move more functionality into the digital domain; analog circuits will continue to be an important part in electronics systems. Since, most of the signal processing today is performed in the digital domain, severe requirements are introduced on the analog circuitry in data converters and anti-aliasing filters. It is predicted that the number of systems-on-chip (SoC) containing analog circuitry will increase with time. In digital design, the levels of abstraction and automation in the design flow have managed to keep in phase with this development. However, this is not the case for analog circuits. The analog design flow suffers from a low-level of abstraction and automation, making it one of the major bottlenecks in mixed-signal design.

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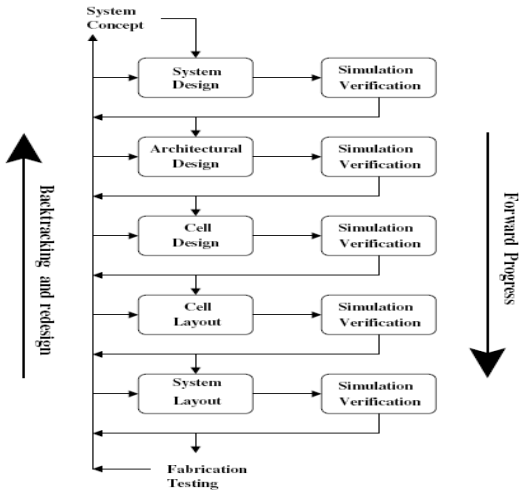

Fig1: Traditional Analog Design Flow

Most of the time and effort are spent on the analog parts. Analog design is particularly difficult: it deals with a huge number of specific circuit classes, it requires a customized design approach for each circuit class, and analog circuits are very susceptible to noise and variations. One of the most important problems with analog design is that many performance measures are used to characterize a circuit. Further, complicated relations exist between the performance measures and the design parameters. Hence, a traditional manual design methodology is a complicated trial-and-error procedure which is time consuming and requires much designer experience. By instead using an analog design automation tool all circuit performances can simultaneously be optimized to obtain better circuit performance in shorter time. Here the problem of automating the analog design flow is addressed. Specifically, the problem of determining the design parameters for an analog integrated circuit at the cell level is considered. An optimization method in conjunction with automatically derived equations for the circuit performance is used to solve this task.

II METHODLOGY

The schematic analog design problem discussed has high aims, and requires many features to be practical for industrial use. There have been no satisfactory solutions in the literature available to all the problems. Therefore, researchers have started to explore the potentials of combining different intelligent systems solutions.With the MAELSTROM system, Krasnicki *et. al.* applied "parallel recombinative simulated annealing (PRSA) to global parameter optimization. In PRSA, multiple simulated annealing algorithms are run concurrently, and share information via a genetic algorithm scheme. MAELSTROMoptimized circuits with up to 27 independent design variables (decent complexity) in a reasonable amount of time. A similar method by the same group called ANACONDA incorporated a genetic algorithm coupled with a local "pattern search" technique.ANACONDA had constraints on device operating regions as an effective heuristic to ensure a safety margin from manufacturing or environmental variations for MOSFETs. It was not clear how non-MOSFET devices could deal with variations. Doboli *et. al.* [9] proposed a two-layered synthesis methodology with a branch-and-bound algorithm for architecture generation and a genetic algorithm based heuristic method for component synthesis and constraint transformation, implemented in the VASE behavioral-synthesis tool [43].

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FASY : actually coupled fuzzy logic with simulated annealing and gradient search. It used fuzzy logic for topology selection, simulated annealing for the "rough" global parameter optimization, and gradient search to get a refined result via local parameter optimization. Is used a backpropagation algorithm borrowed from neural networks (essentially a local optimizer) to update the fuzzy rules based on data gathered in optimization runs.

III. EXISTING SYSTEM

Since analog circuit design presents well defined but difficult design problems, researchers in classical artificial intelligence, classical optimization, and intelligent systems have been using the analog design domain as a test-bed for their methods for quite some time.The biggest drawback to the classical AI approaches (tree search, expert systems, etc.) was the lack of flexibility: a lot of effort was needed in order to handle new processes, topologies, etc., and even once those were in place, the tools tended to break easily whenever slightly different problems were handled. The classical optimization approaches tended to be gradient-based approaches, which could only be applied to local parameter optimization when the objective functionswere differentiable and the design space was continuous. However, complex circuit problems tend to be non-differentiable and have continuous and discrete design spaces (or potentially even more unusual design spaces in the case of topology synthesis). Ochotta *et. al.* have gave a more detailed review of each these approaches.

Intelligent systems-based approaches, on the other hand, offer the potential to meet the aims and features of an "ideal" analog schematic cell design tool. Indeed, these approaches have come the farthest in achieving the "ideal tool" for automatic analog circuit design. Therefore, we will restrict the scope of our survey to intelligent systems approaches because these approaches offer the most promise for the future.

IV. PROPOSED SYSTEM

Broadly speaking, the goal of research in electronic design automation (EDA) is to develop tools and methodologies to aid digital/analog/mixed-signal circuit design engineers to design complex, high-performance circuits with greater functionalities, higher yield and lower cost in an effective and efficient way. EDA tools and methodologies have made possible the incredible levels of complexity present in today's circuits – some chips have on the order of tens of millions of transistors.A top-down methodology is one of the keys to handling such complex circuit designs [6]. In a top-down circuit design methodology, the preliminary system-level concept is refined in a series of steps. Initially, an architectural design phase is undertaken where the overall system concept is broken down to a set of high-level building blocks that, together, achieve system-level specifications. These blocks are further decomposed until they are small enough in size to treat as atomic circuit cells. Once all cells are designed, system layout is done. Then, bottom-up verification is performed, and changes are made as necessary. Some

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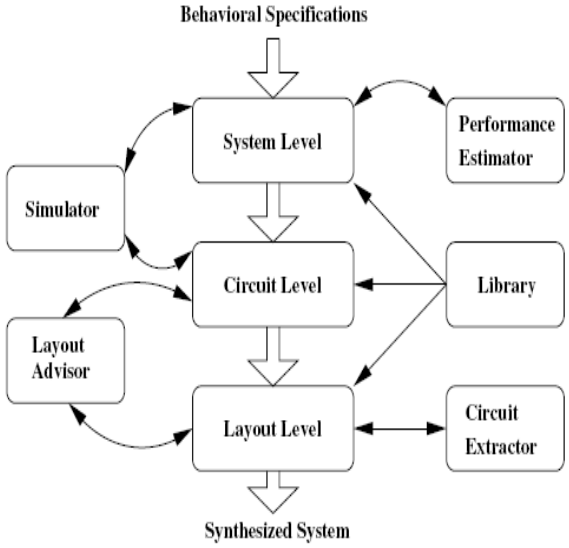
iterations among the levels in the design hierarchy are likely to occur.



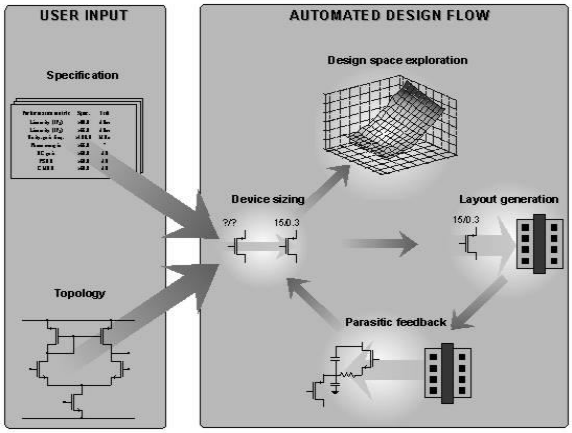


Fig 2: Proposed Analog Design Flow

Cell-level design deals with electrical components such as transistors, resistors, and capacitors (as opposed to higher-level blocks such as operational amplifiers or phase-locked loops). Generally, the design flow at the cell level proceeds as follows. Given the design specifications, the engineer first designs a sized schematic. A schematic is an arrangement of components joined by wires. Each component is further specified (sized) by a set of component values. A structural specification of an electrical circuit includes both its topology and the sizing of all of its components. Second, the engineer translates the sized schematic into a polygonal silicon-level description. This "physical" description specifies the geometrical placement and routing of components; it also describes how the silicon should be arranged on the chip in order to give the same behavior as the schematic. Finally, the engineer verifies the design at the layout level, and re-iterates if necessary.Considerable progress has been made in automating the design of certain categories of digital circuits. In contrast to digital design, most of the analog circuits are still hand-crafted by experts. In current mixed-signal (analog plus digital) integrated circuits, the analog circuits represent only a small part of the area (about 20%), but it takes 80% of the design efforts. This is largely because since SPICE in the 1970s, there have not been commercially-usable analog design tools to significantlyimprove analog designer productivity.There is a huge amount of research in electronic design automation tools, so we need to limit the scope of this paper to a very specific area of these tools. First, we focus on cell design, as we described above. Second, we focus only on the schematic-level aspect of design; we do not deal with the layout level. Third, we focus only on analog design tools; we do not specifically deal with digital, mixed-signal, or radiofrequency (RF) tools. Fourth, we address only the tools that deal directly with design; we do not deal with other topics such as visualization or prediction. Finally, we address only intelligent systems approaches to this problem.

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Design of analog schematics at the cell level includes specific tasks. The first task is to choose a topology – an appropriate interconnection of transistors, capacitors and other circuit devices. The second task, called *sizing and biasing*, is to choose circuit parameters such as device sizes and independent source biases to meet the nominal specifications. Manual execution of these tasks is a long, iterative process where an expert design engineer interacts with a circuit simulator to understand
how well a candidate design is performing. Consequently, cell design can take weeks to months. Therefore, it is desirable to have tools which can speed or automate this process. Such tools could have one of the following possible *aims*:

1. Local parameter optimization: to "tune" an almostdesigned circuit looking for slight increments in performance without drastically changing the design variables.

2. Global parameter optimization: to automatically find the optimal circuit parameters to the design specifications, independent of the initial circuit parameters.

3. Topology selection: given a set of pre-specified potential topologies, to automatically choose the optimal circuit topology along with the optimal circuit parameters.

4. Topology synthesis ("structural optimization"): to automatically
"invent" new circuits which are optimal in both topology and parameters.

V. CONCLUSION AND FUTURE SCOPE

The active research in analog design automation has resulted in a large volume of research. Since it is practically impossible to review the whole work in the field, we have restricted ourselves to intelligent system techniques applied to design of analog schematics at the cell level. The inter-disciplinary nature of the field requires close collaborations among electrical engineers, computer scientists and intelligent systems researchers in developing practical, usable tools and methodologies for analog design automation.It is our hope that most future research in intelligent systemsbased schematic analog cell design will have the aim of topology synthesis, and improve upon the state-of-the-art in features such as: complexity, efficiency, robust design, multi-objective design, interactive design, and flexibility. There is considerable work to be done in each of these areas, and in combinations of these areas. For example, very few papers in the literature have dealt with the issue of robust design, which is essential if the circuit is to be manufactured. Achieving these aims and features may involve more use of the intelligent systems techniques mentioned in this paper (many such as neural networks have barely been used), by use of newer techniques such as Particle Swarm Optimization, or by use of hybrid techniques combining more than one intelligent systems technique.

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