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DESIGN OF INDUCTOR-LESS LNA FOR WIDEBAND APPLICATIONS

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ABSTRACT—A design of inductor-less low-noise amplifier (LNA), which is an important block in the design of broadband receivers, is discussed in this paper. The LNA discussed in this paper uses a differential positive-negative feedback and Dual capacitive cross coupling (DCCC) techniques, which will enable us to choose the trans conductance of the LNA to increase the amplification and reduce the noise figure (NF). The LNA presented in this paper is implemented in 180nm technology. It consumes a power of 2.3mW from a 1.8v supply voltage. The results shows that the implemented LNA achieved a gain of 22.7dB with a 3-dB bandwidth of 1.7GHz, the circuit has achieved a noise figure of 2.1dB and the IIP_3 i.e third order input intercept point of the circuit is -2.2dBm with an input matching of 50Ω.

Index Terms—Differential positive-negative feedback, DCCC, inductor less, low-noise amplifier (LNA), low power, noise figure (NF) and gain.

(I) INTRODUCTION

The design of wide band amplifiers is became a major task in the transceiver design. The major challenges in the design of wideband receivers are design of Low Noise Amplifier (LNA).As the first block in the receiver chain, such an LNA should achieve good impedance matching, high and flat gain, and low noise figure (NF), Low power consumption and small size across a wide frequency band. Recently some LNA's used resistive feedbacks [1], some other are implemented using distributive amplifiers [2] and they achieved good bandwidth but they are power hungry. Other implementations used inductive source degeneration CS LNA's [3] with resistive feedback and achieved wideband matching but occupied more area because of inductors.One of the wideband LNA topologies that have been widely investigated is the common-gate low-noise amplifier (CGLNA). The CGLNA is attractive compared to other topologies as it features wideband input impedance matching. Also, it offers good linearity, stability, and low power consumption. However, its main drawback is the relatively high NF. This is due to the input matching condition, which restricts a certain value of trans conductance to be used that leads to low gain, and hence, high NF. Noise-reduction techniques are used to overcome the disadvantage of the CGLNA configuration [4]. The gain boosting scheme

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using negative feedback employing capacitive cross-coupling [5], dual negative feedback [6], and positive-negative feedback [7] are applied to break the tradeoff between the input matching condition and the NF, which lead to simultaneous reduction in noise and power dissipation. In this paper we are presenting a low noise amplifier which uses a differential positive-negative feedback.

(II) BACKGROUND

The capacitive cross-coupling (CCC) has been used for gain enhancement, matching and improving the NF of a common gate input stage [8]. The common gate capacitive cross coupling structure has a minimum NF as follow.

$$F = 1 + \gamma/2 \quad (1)$$

Where, γ is channel thermal noise coefficient.

To improve the Noise Factor (NF) and gain dual capacitive cross coupling has been used and is shown in fig 1.This DCCC structure [9] has attained a noise figure as shown below.

$$F = 1 + \gamma\left[\frac{(g_{m1}R_s - 1)}{g_{m1}R_s} + 2g_{m1}R_s - 1\right] \quad (2)$$

Differentiating the equation with respect to $g_{m1}R_s$ to get an optimized value of noise figure and is given as

$$(g_{m1}R_s)_{opt} = 1/1.732 \quad (3)$$

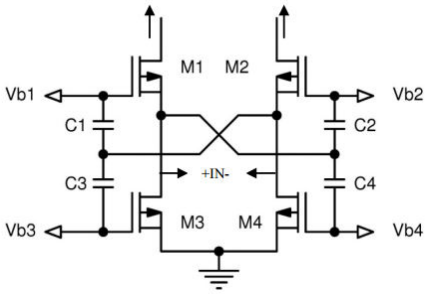

Fig 1: DCCC Structure

Substituting the $g_{m1}R_s$ value in equation 2 we will get the noise figure as below.

$$F = 1 + 0.464\,\gamma \quad (4)$$

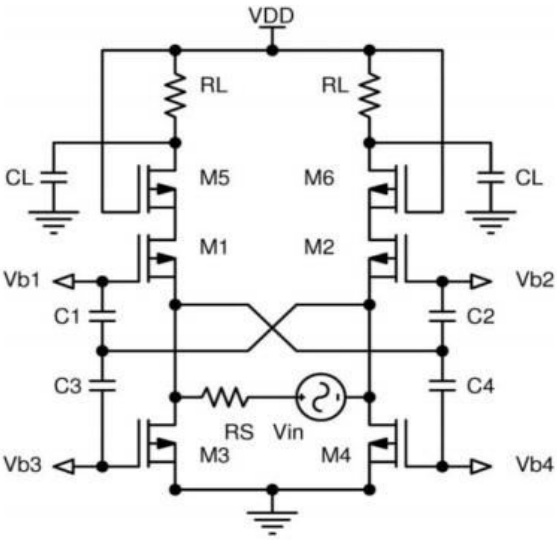

Fig 2: Circuit diagram of LNA core

The core LNA circuit schematic is shown in Fig. 2 without the biasing circuit required to supply and M5 and M6 are added for reverse isolation and are of small size to preserve the amplifier bandwidth. M3 and M4 can be coupled without the use of C3 and C4, but in this case, a large dc overhead on M3and M4 limits the linearity. M3 and M4 are biased from the same biasing circuit supplying M1 and M2 through high-resistivity polyresistors without much excess current consumption. The bias circuit implemented in this brief is similar to that in [10].

The voltage gain ratio is given by

$$\frac{V_o}{V_i} \cong \frac{2g_{m1}R_L}{1+SC_{d5}R_L} \quad (5)$$

(a) Negative Feedback CGLNA Employing Capacitive Cross-Coupling

The idea to improve the noise performance of the CGLNA is based on introducing a decoupling mechanism between the input

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power matching condition and the NF. This is achieved by improving the effective Trans conductance and enhancing the gain. The single-ended model of the trans conductance boosting structure [11]. The structure uses an inverting gain A_{NEG} that is inserted in the feedback between the gate and source terminals of M_1. The effective g_{m1} is boosted to $g_{m1}(1+A_{NEG})$ with input impedance matching of $1/g_{m1}(1+A_{NEG})$. . This means smaller bias current, less channel noise from M_1, and consequently smaller noise contribution and power consumption. The noise factor F is then given by

$$F = 1 + \frac{\gamma}{(1+A_{NEG})\alpha} + \frac{4R_S}{R_L}. \quad (6)$$

One possible way to implement the inverting gain is to use cross-coupling capacitors , as shown in the differential CGLNA topology's and is approximately given by the capacitors ratio$(C_1-C_{gs1})/(C_1+C_{gs1})$, where C_{gs1} is the gate–source capacitance of M1 .For C1>>Cgs1, A_{NEG} is almost unity, which reduces A_v, R_{in} and F to the following:

$$A_v = 2g_{m1}R_L$$
$$R_{in} = 2R_S = 1/g_{m1}$$
$$F = 1 + \frac{\gamma}{2\alpha} + \frac{4R_S}{R_L}.$$

Comparing to the conventional CGLNA, F is reduced and the effective Trans conductance is increased with reduction in power consumption.

(b) Positive–Negative Feedback CGLNA

The negative feedback CGLNA reduces the NF by the use of capacitive divider. Meanwhile, its Trans conductance is g_{m1} restricted to 10 mS to satisfy the input power matching condition. Thus, this solution suffers from low gain. To alleviate the restriction of low g_{m1}, a positive feedback along with the negative feedback is used in [12]. To increase the gain, the idea is to create a positive current feedback path through, as shown in this single-ended model. This feedback path increases the input impedance of the LNA to be equal to $1/[g_{m1}(1+A_{NEG})(1-A_{POS})]$, where $A_{POS}=g_{m2}R_L$ is the positive feedback gain, which varies from 0 to 1 for stability.

In this way g_{m1}, can be chosen arbitrarily to values higher than10 mS without restricting the input matching condition. For example, if $A_{POS}$is designed to be 0.5 and A_{NEG}=1, then g_{m1}=20mS for the 50- input matching to be satisfied. Thus, the gain increases. Since the positive feedback loop provides a degree of freedom in a way that the impedance matching does not fix the bias current, the current will be a design variable to improve the noise performance.

For A_{NEG}=1 and A_{POS}=0.5,A_v, R_{in} and F are reduced to the following:

$$A_v = 2g_{m1}R_L$$
$$R_{in} = 2R_S = 2/g_{m1}$$
$$F = 1 + \frac{\gamma}{4\alpha} + g_{m2}R_S\frac{\gamma}{\alpha} + \frac{9R_S}{4R_L}.$$

The given design is providing a reasonable noise factor still we can reduce the noise figure with the help of a Differential Positive negative feedback circuit [13].Since the positive feedback loop provides a degree of freedom in a way that the impedance matching does not fix the bias current, the current will be a design variable to improve the noise performance. The disadvantage of the circuit is it is more complex because the inductors occupy more area and the power consumption is also high. So we are going for a modified Differential positive negative feedback amplifier.

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III. IMPLEMENTATION OF DIFFERENTIAL POSITIVE-NEGATIVE FEEDBACK LNA WITH DCCC

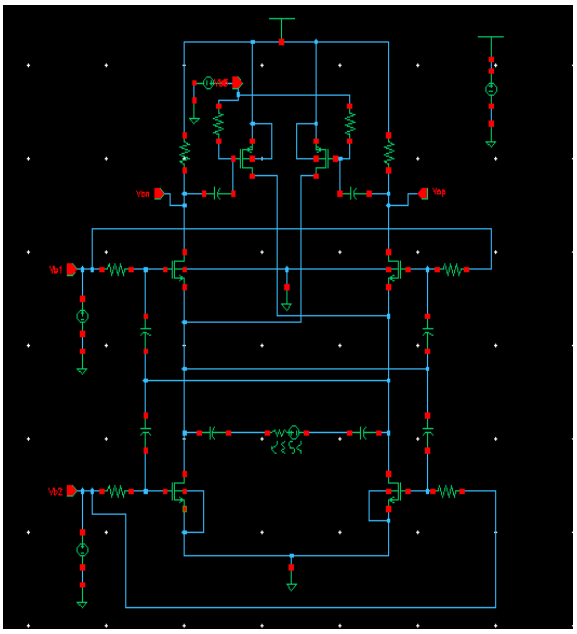

Fig3: Modified differential positive-negative Feedback.

The modified differential positive-negative feedback with DCCC is shown in the above figure. This LNA is implemented by combining the dual capacitive cross coupling structure which is implemented to reduce the noise figure and the differential positive-negative feedback network to choose the choice of LNA's Trans conductance, to increase the gain and noise figure. The implemented circuit results in increased g_m value nearly 20.11mS keeping the input matching condition constant. The input impedance matching is achieved by sizing and adjusting the bias current of the upper input transistors M1, M2 and lower input transistors M3 and M4. The differential positive-negative feedback is implemented with the help of PMOS transistors and is used to increase the value of g_m results in increasing the gain and reduction in noise figure. Proper biasing should be provided so that all the transistors are in saturation region to produce the output. The sizing of the transistors should be done precisely to get the accurate output. The capacitances at the input should be greater than the input capacitance's of M1, M2, M3 and M4 to keep the desired frequency band.

IV. RESULTS AND DISCUSSION

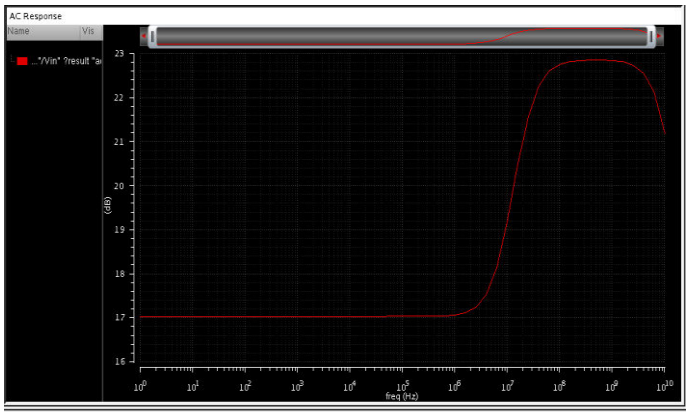

Fig4: Graph of Gain

(a) Gain

The above figure shows the gain of the differential positive negative feedback with DCCC. The circuit results a gain of 22.7dB for a 1.8v supply which is more as compared to the differential positive-negative feedback network with inductors and DCCC circuit. This is due to the feedback network which results a g_m of 20.11mS which increased the gain because the gain is dependent on g_m.

(b) Noise figure

The noise figure that is explained in positive-negative feedback was dependent on g_m and is implemented with DCCC structure will results in reduction of the noise figure. The noise figure obtained is 2.1dB which is less compared to the LNA's explained in this paper for a 1.8v supply.

(c) Input Impedance

The figure6 shows that the input impedance of the circuit is 50Ω at an input frequency of 1GHz even though the trans conductance of the circuit is increased. This will results in good impedance matching.

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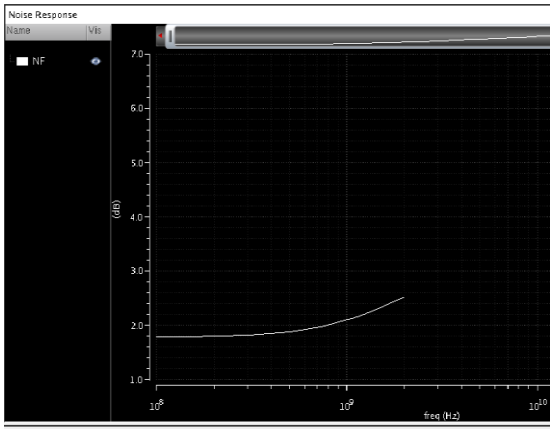

Fig5: Graph of noise figure

the output power versus the input power both on logarithmic scales. The typical value of IIP3 is -10dB, here we got -2.2dB which is better than the other topologies.

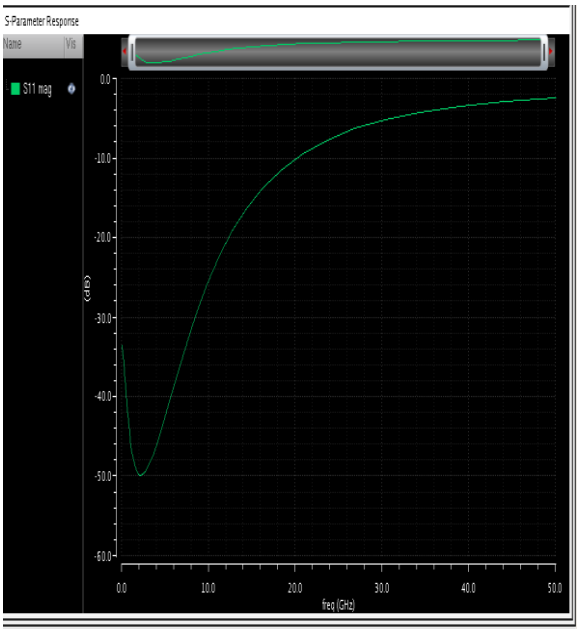

Fig6: Graph of S_{11}

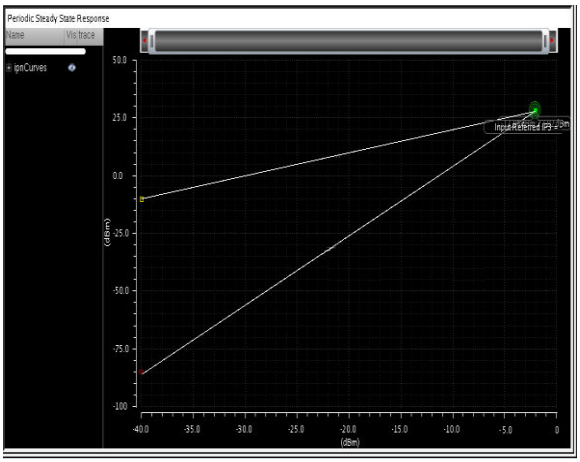

Fig7:Graph of IIP3

(d). IIP3

The corruption of the signal due to third-order intermediation of two nearby interferers is so common and so critical. So a performance metric has been defined that is called third-order intercept point. The third-order intercept point is defined to be at the intersection of two lines. The horizontal co-ordinate of this point is called the input IP3, and the vertical co-ordinate is called output IP3. The intercept point is obtained graphically by plotting.

(E). Stability Factor

While designing any amplifier, it is important to check the stability of the device chosen, or the amplifier may function as an oscillator. For determining stability, calculate Rollets stability factor (represented as variable K) using S-parameters at a given frequency. For a transistor to be stable, parameters must satisfy K>1 and $|\Delta|<1$. For our circuit we got stability factor is >1 so that our circuit works properly.

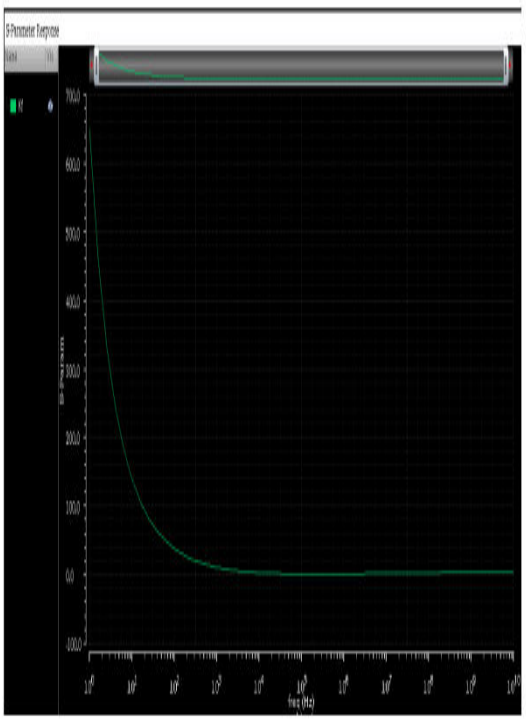

Fig 8: Graph of Stability Factor

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Table1: Performance summery of our LNA with the existing work

Topology	Gain(dB)	NF(dB)	IIP_3(dBm)	Power(mW)	Frequency range(GHz)	Technology
Single ended CG	16.9	2.57	-0.7	12.6	1.05-3.05	0.18um
Differential CG	21	2.3	-3.2	3.6	0.3-0.92	0.18um
DCCC Structure	18.94	3.15	-3	5.77	0.4-5.7	0.18um
Differential resistive feedback	21	1.4	-1.5	18	0.002-2.3	0.090um
This work	22.7	2.1	-2.2	2.3	0.1-1.77	0.18um

V. CONCLUSION

In this paper we presented an inductor-less LNA with differential positive-negative feedback and DCCC technique in 180nm technology. The implemented LNA achieved a gain of 22.7dB with a 3-dB bandwidth of 1.7GHz, the circuit has achieved a noise figure of 2.1dB and the IIP3 i.e. third order input intercept point of the circuit is -2.2dBm with an input matching of 50Ω. This results shows that the implemented LNA is better than the other LNA topologies.

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