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Volume 06, Issue 10, Pages: 114–127.
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AN ASYMMETRIC SINGLE PHASE REDUCED SWITCH COUNT MULTILEVEL INVERTER USING ADVANCED PULSE WIDTH MODULATION TECHNIQUE

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ABSTRACT- In this paper, a new topology for Multilevel Inverter (MLI) with reduced switch count is proposed with an asymmetric dc source configuration. This configuration is used to double the output voltage level in multilevel inverter based on switched dc sources by adding two switches with dc sources. The increased number of levels in the output voltage reduces the filtering requirements. The working principle of the proposed asymmetric inverter is presented through the single phase fifteen level inverter. The harmonic contents of different modulation indices are examined. The performance analysis of the inverter is compared with trapezoidal and Sinusoidal Pulse Width Modulation (SPWM) in terms of Total Harmonic Distortion (THD), fundamental rms voltage (Vrms) and Crest Factor (CF). The simulation results for the same are evaluated using MATLAB/SIMULINK.

KEYWORDS Asymmetric, crest factor, multilevel inverter, pulse width modulation, total harmonic distortion.

1. INTRODUCTION

The multilevel inverter is one of the most researched areas in recent years. The aim of multilevel inverter is established on the forming of high quality output voltage waveform with less harmonic distortion and hence it reduces the size of passive filter requirements. So it is more suitable for high voltage and high power industrial applications as compared to the conventional two level inverters [1]. When the number of levels increases, the usage of switches with gate drive circuits also increases, thereby, resulting in increased complexity and cost. Diode Clamped Multilevel Inverter (DCMLI), Flying Capacitor Multilevel Inverter (FCMLI) and Cascaded H Bridge Multilevel Inverter (CHBMLI) are the classical topologies of multilevel inverters. But the drawback of classical MLIs is that the number of switches increases and the cost also goes up when the topologies are expanded for a higher number of levels [1, 2]. Therefore the challenge is to reduce the switches in multilevel inverter topologies. Some of the possible methods are described here in to reduce the switches. Such methods are inverter structural modification, usage of asymmetric source instead of symmetric source and combination of structural modification with asymmetric source configuration. A new inverter topology

utilizing both bidirectional and unidirectional switches, capable of synthesizing all possible additive and subtractive combinations of the input dc levels are developed [2, 3]. The series connected switched sources structure [4, 5] and cross connected switched MLI [6, 7] utilizes only unidirectional switches and voltage levels may differ based on the input voltage source either symmetric or asymmetric. Symmetric multilevel inverter dc sources are equal in magnitude. Asymmetric multilevel inverter dc sources are not equal in magnitude. Gupta et al [4, 5, and 8] proposed a novel multilevel inverter based on switched dc sources. In this configuration alternate dc sources are linked in opposite polarities via power switches [4]. This configuration has 2 ' number of+' K ' number of input dc sources with ' 2K switches. Number of dc source and type of dc source (either symmetric or asymmetric) determines the maximum number of levels in the output voltage waveform. Symmetric dc 2 ' output voltage+sources were used to produce ' 2K levels [4,5,8]. The trinary dc source (1:3:9...) is not suitable for this configuration and also binary dc source (1:2:4...) cannot be employed when more than two dc sources are available. In this case when three dc sources are considered, there is no possible combination to give an output voltage of Vdc1+Vdc3,Vdc1-Vdc2, Vdc2-Vdc3 and Vdc1-Vdc3 [4-8]. In [9], binary configuration employed satisfactorily when the existing network is combined with the cascaded H bridge inverter. It produces 15 level output voltage waveform with 1:2:4 ratio dc sources. Originally the structure of inverter was proposed by Liao et al [10] for distributed energy resources. A level doubling network (LDN) is analyzed by adding an extra network with the rest of MLI configuration. The approach is valid for any MLI configuration [11, 12]. In [13], a LDN concept is utilized [4, 5, 6] with symmetric dc sources. This paper proposes a new configuration to almost double the output voltage level in an existing MLI [5] by adding only two switches with dc sources. The existing MLI operate at asymmetric condition in proposed configuration. Advance Pulse Width Modulation is used to improve the performance of the output voltage. Trapezoidal PWM is one of the types in it that gives better rms voltage compare to the SPWM. Sine and Trapezoidal PWM techniques are used to trigger the gate of the switches with Phase Disposition (PD), Alternative Phase Opposition Disposition (APOD), Phase Opposition Disposition (POD) and Variable Frequency (VF) carrier techniques. Sinusoidal pulse width modulation (SPWM) offers lower THD, whereas Trapezoidal PWM offers higher fundamental rms voltage. The proposed inverter configuration can generate 15 level output voltage and each level is equal to the smallest input voltage.

2. Arrangement of dc Sources

To increase the number of levels in the output voltage, different combinations of input dc sources are assumed in the following aspects. Unary arrangement consists of all dc sources are in equal magnitude or voltage which is called Symmetric source arrangement.

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$V_{dc,K} = V_{dc}$ ..... (1) where $(K = 1.,2,3.....n)$

1' combination of+By using this arrangement, ' 2K levels can be generated in the output voltage. Binary arrangement consists of all dc sources which are not in equal magnitude or voltage. They also have a geometric progression of '2' which is called Asymmetric Binary source arrangement.

$V_{dc,K} = 2^{K-1} V_{dc}$ ..... (2) where $(K = 1.,2,3.....n)$

The above formula can be utilized for $'2^{(K+1)} - 1$ combination of levels in the output voltage. Trinary arrangement consists of all dc sources which are not in equal magnitude or voltage. They also have a geometric progression of '3' which is called Asymmetric Trinary source arrangement

$V_{dc,K} = 3^{K-1} V_{dc}$ ..... (3) where $(K = 1.,2,3.....n)$

By using Trinary arrangement the number of level in the output voltage is ,, 3^K ". Quasi linear arrangement consists of all sources are not in equal magnitude or voltage and it can be expressed as

$V_{dc,K} = 3^{K-1} V_{dc}$ ..... (3) where $(K = 1.,2,3.....n)$

By using Trinary arrangement the number of level in the output voltage is ' 3^K '.

Quasi linear arrangement consists of all sources are not in equal magnitude or voltage and it can be expressed as

$$V_{dc,K} = \begin{cases} V_{dc} \ldots\ldots\ldots\ldots\ldots\ldots K = 1 \\ 2 \times 3^{K-2} V_{dc} \ldots\ldots\ldots\ldots K \geq 2 \end{cases} \quad \ldots\ldots\ldots (4)$$

By using quasi linear arrangement, the number of levels = $1 + \sum_{k=2}^{\infty} 2 \times 3^{K-1}$ .....(5)

Different dc source arrangements can generate different number of levels in the output voltage waveform. The results with three dc sources are summarized in Table 1. From the Table 1, it is concluded that if more than two dc sources used in the circuit, Trinary arrangement will give better number of levels compare to other arrangements.

3. Operation of Proposed Topology

The proposed configuration is realized by adding the extra network in the existing MLI which is shown in Fig.1 [5] and it can generate almost double the number of levels in the output. The general structure of single phase proposed configuration is shown in Fig 2 (a). The existing MLI (shown in Fig.1) cannot operate for binary configuration when more than two dc sources are used. Natural sequence of number (1, 2, 3….) dc sources is adapted for this configuration to generate the number of levels in the output voltage. The placement of dc sources is equally important to produce the maximum number of levels. The placement of dc sources in different position (up to five number of dc sources) are tabulated in Table 2 and also in literature [5].

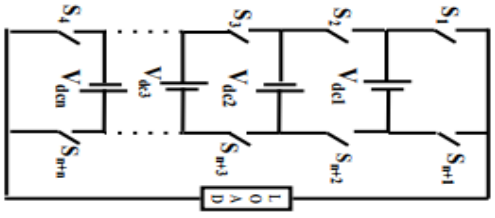

Fig.1. Generalized single phase structure of existing configuration

Table 1. Different dc source arrangements and their corresponding number of levels

S.No.	Type of dc source	Type of dc source arrangement	Ratio of dc sources	General output voltage formula	Number of level in the output voltage
1	Symmetric	Unary	1:1:1...	$2K+1$	7
2	Asymmetric	Natural number Sequence	1:2:3:...	K^2+K+1	13
3		Binary	1:2:4:...	$2^{(K+1)}-1$	15
4		Trinary	1:3:9:...	3^K	27
5		Quasi Linear	1:2:6...	$1+\sum_{i=2}^{\infty} 2 \times 3^{K-1}$	19

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To derive the general formula of the number of levels in the output voltage, let us consider the value of dc sources in the following condition

Even number of dc sources

$$V_{dc,i} = \begin{cases} (2i-1)V_{dc} \ldots\ldots for (1 \le i \le K/2) \\ 2(K+1-i)V_{dc} \ldots\ldots for \left(\frac{K+2}{2}\right) \le i \le K \ldots (6) \end{cases}$$

Odd number of dc sources

$$V_{dc,i} = \begin{cases} (2i-1)V_{dc} \ldots\ldots for (1 \le i \le (K+1)/2) \\ 2(K+1-i)V_{dc} \ldots\ldots for \left(\frac{K+3}{2}\right) \le i \le K \ldots (7) \end{cases}$$

The possible peak value of the output voltage of the inverter is

$$V_o = (1+2+3+\ldots\ldots+K)V_{dc}$$

$$V_o = V_{dc}\sum_{i=1}^{K} i$$

$$V_o = V_{dc}\left(\frac{K(K+1)}{2}\right)$$

From the above equation the possible peak value of the output voltage can be determined. The positive half cycle will have $\left(\sum_{i=1}^{K} i\right)$ number of levels excluding the zero level. So, the number of levels in the output voltage waveform is evaluated as Here 'P' represents the number of output voltage levels and 'Vo' represents the possible peak value output voltage. To increase the number of levels in output voltage, different asymmetric configurations are described in section 2. The disadvantage of these configurations is the requirement of high voltage dc sources. In the proposed configuration, addition of extra network in the existing MLI leads to almost double the output voltage level. The value of dc sources are required only at Vdcx=Vdcx′ = 0.5Vdc1. So, the output voltage level of the proposed inverter configuration is

$$P = [2\times(K^2+K+1)+1] \ldots\ldots\ldots\ldots (9) \quad \text{Where } (K = 2,3\ldots\ldots)$$

The above equation can be derived from the equation 8 because the proposed inverter can generate to almost double the output voltage level.

Table 2. Placement of dc source in proposed configuration

Number of dc sources	V_{dc1}	V_{dc2}	V_{dc3}	V_{dc4}	V_{dc5}
1	V_{dc}	-	-	-	-
2	V_{dc}	$2V_{dc}$	-	-	-
3	V_{dc}	$3V_{dc}$	$2V_{dc}$	-	-
4	V_{dc}	$3V_{dc}$	$4V_{dc}$	$2V_{dc}$	-
5	V_{dc}	$3V_{dc}$	$5V_{dc}$	$4V_{dc}$	$2V_{dc}$

The proposed configuration which is shown in Fig. 2(b) can generate fifteen level output voltage whereas the existing configuration (Fig. 1) without the extra network (i.e. Vdcx and Vdcx‟) can give only seven level output voltage. The modes of operation for 15-level output voltage of the proposed configuration are summarized in table 3. For the positive voltage level the voltage source Vdcx and the switch S7 conducts electricity. For the negative voltage level, the voltage source Vdcx′ and the switch S8 conducts electricity.

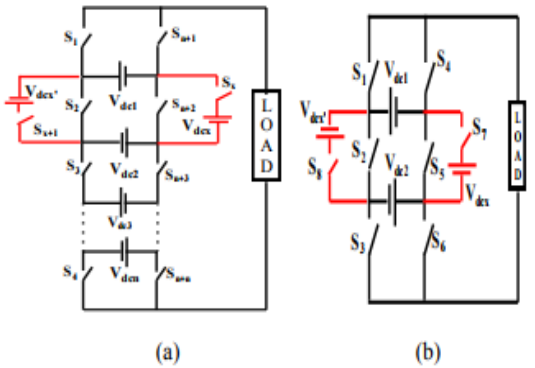

Fig.2(a) Generalized structure for single phase proposed configuration. **(b)** Proposed configuration for the fifteen level output voltage

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The value of dc sources in extra network is equal to the voltage of 0.5Vdc1. Mode 1 and 9 become a redundant state for zero level output voltage. Mode 1 to Mode 8 used for synthesis of positive levels and mode 9 to mode 16 used for synthesis of negative levels including zero level. When Mode 1, Mode 3, Mode 5 and Mode 7 alone operate (without extra network) the proposed inverter generates 7 level output voltage (Vdc1, Vdc2, Vdc1+Vdc2). When the extra network comes into operation, we get 15 level output voltage in the positive half cycle. In this case Mode 2, Mode 4 Mode 6 and Mode 8 operations are added with the previous operating modes (Vdcx, Vdc1+Vdcx, Vdc2+Vdcx, Vdc1+Vdc2+Vdcx). Similarly, in the negative half cycle, the output voltage levels (-Vdcx to – (Vdc1+Vdc2+Vdcx)) can be synthesized using the modes 9 to 16. It is observed that the proposed inverter generates an odd output voltage levels in both positive and negative half cycle with the extra network whereas the extra network is bypassed when an even output voltage level is produced in both positive and negative polarity. The proposed inverter is well suited for renewable energy application such as solar panel or fuel cell. Because the structure contains individual dc sources, it can be easily replaced by the solar panel or fuel cell depends on the rating.

Table 3. Operating modes with switches and corresponding output voltage for the proposed 15 level inverter

Mode	On state switches	Output Voltage
1	S_4, S_5, S_6	0
2	S_4, S_6, S_7	V_{dcx}
3	S_1, S_5, S_6	V_{dc1}
4	S_1, S_6, S_7	$V_{dc1}+V_{dcx}$
5	S_3, S_4, S_5	V_{dc2}
6	S_3, S_4, S_7	$V_{dc2}+V_{dcx}$
7	S_1, S_3, S_5	$V_{dc1}+V_{dc2}$
8	S_1, S_3, S_7	$V_{dc1}+V_{dc2}+V_{dcx}$
9	S_1, S_2, S_3	0
10	S_1, S_3, S_8	$-V_{dcx'}$
11	S_2, S_3, S_4	$-V_{dc1}$
12	S_3, S_4, S_8	$-V_{dc1}-V_{dcx'}$
13	S_1, S_2, S_6	$-V_{dc2}$
14	S_1, S_6, S_8	$-V_{dc2}-V_{dcx'}$
15	S_2, S_4, S_6	$-V_{dc1}-V_{dc2}$
16	S_4, S_6, S_8	$-V_{dc1}-V_{dc2}-V_{dcx'}$

4. Switching Scheme

Both high and low switching frequency modulation techniques have been employed for multilevel level control scheme. Carrier based pulse width modulation and space vector modulation techniques are the high switching frequency modulation techniques. Active harmonic elimination, selective harmonic elimination and fundamental frequency techniques are considered as low switching frequency techniques [4]. With suitable compliance, any one of these techniques can be used for the control of switches in the proposed configuration. In

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this paper, the switching scheme is exhibited through the Multi carrier Pulse Width Modulation (PWM). Advance PWM includes Trapezoidal modulation, Staircase Modulation, Stepped Modulation, Harmonic injection modulation, and Delta modulation to improve the performance parameters of the output. Compared to the SPWM, Trapezoidal PWM offers several advantages like production a higher fundamental output voltage, simplicity and ease of implemention. Trapezoidal signal itself constitutes of two linear segments, especially the horizontal line and slope line. The shape of the trapezoidal is completely depends on the location of its slope and angle (Fig. 3(b)). The harmonic contents will vary with respect to the shape of trapezoidal reference wave [14]. In bipolar switching, the multilevel inverter requires 'p-1' carriers for 'p' level inverter. The comparison of both SPWM and trapezoidal PWM techniques for different level shifting PWM is described. Triangular wave is considered as the carrier signal for both PWM techniques. Level shifting PWM is divided into two groups, namely constant switching frequency and variable switching frequency. Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternative Phase Opposition Disposition (APOD) are the subdivisions of the constant switching frequency. The frequency of the reference signal determines the output voltage frequency, and the peak amplitude of the reference signal controls the modulation index and output voltage level. Sine reference for SPWM and trapezoidal reference for trapezoidal PWM with multi carrier triangular carrier waveforms are used to generate the PWM pulse pattern of the proposed MLI.

4.1. Level shifting Pulse Width Modulation The level shifting pulse width modulation is most popular and very simple to implement. Constant switching frequency and Variable switching frequency are the subdivisions of level shifting PWM. Sinusoidal and trapezoidal pulse width modulations are used for both switching frequency. Here, „p-1" carriers with amplitude 'Ac' and frequency 'fc' are disposed such that the bands they occupy are contiguous for p-level inverter [15]. The peak to peak amplitude of reference is 'Am' and the frequency is 'fm'. The reference signal (Sine and Trapezoidal) is continuously compared with the each of the „p-1' carrier signals. Whenever the reference signal is greater than carrier signals the gating signal (high) is produced. The amplitude modulation index 'Ma' and frequency ratio 'Mf' is given as

$$M_a = \left(\frac{A_m}{(p-1)A_c}\right) \quad \text{.....(10)}$$

$$M_f = \left(\frac{f_c}{f_m}\right) \quad \text{.....(11)}$$

Fig. 3 (a) and (b) show PD technique for sinusoidal and trapezoidal PWM respectively. In this all „p-1' carriers are in phase. Fig. 4 (a) and (b) shows APOD technique for sinusoidal and trapezoidal PWM respectively. In this adjacent carrier are 180 degree out of phase with each other. Fig. 5(a) and (b) shows POD technique for sinusoidal and trapezoidal PWM respectively, where the positive carriers (above zero reference) are in phase, but negative carriers are shifted by 180 degree.

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In Variable Frequency PWM technique also 'p-1' carriers are used for p-level inverter. Such carriers are in phase, but the alternating carriers have different frequency. Fig. 6 (a) and (b) show VF technique for sinusoidal and trapezoidal PWM respectively.

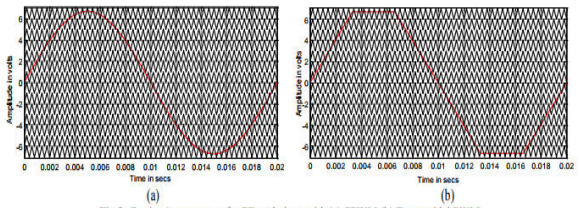

Fig.3. Carrier Arrangement for PD technique with (a) SPWM (b) Trapezoidal PWM

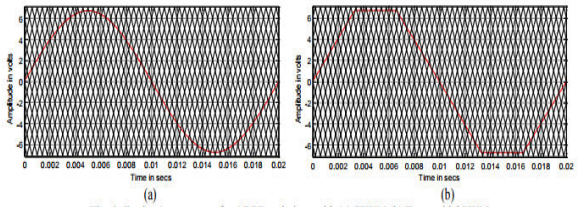

Fig.4. Carrier Arrangement for APOD technique with (a) SPWM (b) Trapezoidal PWM

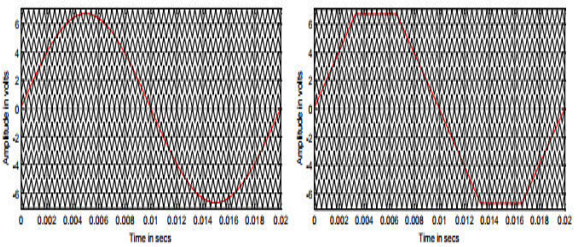

Fig.5. Carrier Arrangement for POD technique with (a) SPWM (b) Trapezoidal PWM

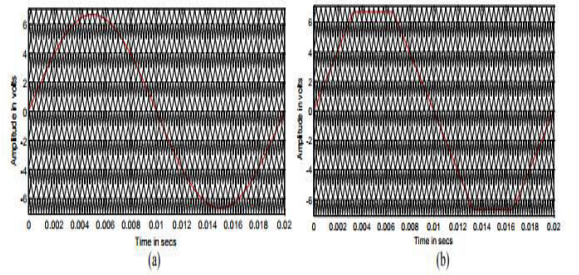

Fig.6. Carrier Arrangement for VF technique with (a) SPWM (b) Trapezoidal PWM

5. Comparison of Other Configuration with Proposed Configuration

The main aim of the proposed configuration is to double the output voltage levels compared to the existing MLI [5], by using minimum number of switches. This configuration is compared with the existing multilevel inverters in terms of number of switches, number of driver circuits, dc sources and output voltage levels. Table 4 shows the comparison of this configuration with existing MLI inverter in terms of general formula for output voltage level. Fig. 7 (a) shows the number of dc sources against the number of output voltage levels for existing asymmetric and proposed asymmetric configuration. From the Fig.7(a) and Table 4, it is clear that the output voltage level of this configuration is double the existing MLI configuration output voltage level according to the dc sources. Fig. 7 (b) shows the number of dc source against the number of output voltage levels for proposed symmetric and proposed asymmetric configuration. In this comparison, the same number of switches and same number of dc sources are used to obtain the output voltage levels. From the Fig.8(b), it is clear that the proposed asymmetric configuration produces better output voltage waveform when compared to the proposed symmetric configuration. Here, K indicates the dc sources of the proposed configuration without extra network. This configuration without extra network operates with either symmetric or asymmetric condition. The extra network dc source values already explained in section 2. If 'K' is 2 and number of switches are 6, the existing symmetric configuration delivers 5 level output voltage and 7 level output voltage delivers in case of asymmetric configuration. But the proposed symmetric

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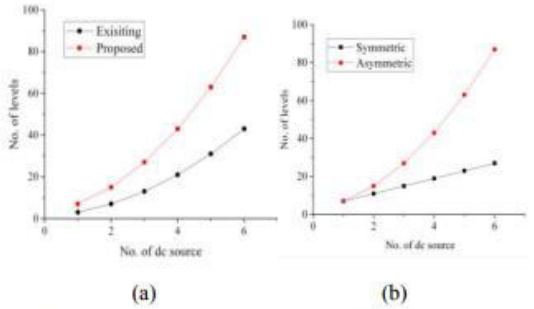
configuration with an extra 2 (8 switches) switches can deliver 11 level output voltage and 15 level output voltage produce in case of asymmetric configuration. In addition, the value of dc sources is 0.5Vdc1 for the extra network of proposed configurations. The comparison is very attractive when 'K' is high. The number of components in proposed inverter is a crucial factor, which is often argued when compared to the other multilevel inverters. In DCMLI, p-level inverter requires 'p-1' dc bus capacitors, '2(p-1)' switches and '2(p-3)' clamping diodes. The number of driver circuit is equal to the number of switches. In FCMLI, '2(p-1)' switches, 'p-1' dc bus capacitor and '(2p-6)/2' clamping capacitor needs for p-level inverter. For p-level inverter in CHBMLI, '2(p-1)' switches and '(p-1)/2' dc sources are required. The main advantage of CHBMLI does not require clamping diodes and clamping capacitor to extract the output voltage. So, the Table 5 compares the number of components required for 15-level inverter of classical configurations like Diode clamped MLI, Flying Capacitor MLI, Cascaded H-Bridge MLI with proposed. From table 5 it is clear that the number of switches is reduced significantly. While all the classical configurations requires twenty eight switches to give a single phase fifteen level and the proposed configuration does with only eight switches. In addition to that, it does not require clamping diodes and clamping capacitors.

Table 4. Comparison of proposed and existing configurations

Components	Existing Configuration		Proposed Configuration	
	Symmetric	Asymmetric	Symmetric	Asymmetric
No. of switches	$(2K+2)$	$(2K+2)$	$[(2K+2)+2]$	$[(2K+2)+2]$
No. of dc source	K	K	$(K+2)$	$(K+2)$
Output voltage	$(2K+1)$	(K^2+K+1)	$[2(2K+1)+1]$	$[2(K^2+K+1)+1]$
No. of driver circuits	$(2K+2)$	$(2K+2)$	$[(2K+2)+2]$	$[(2K+2)+2]$



(a) (b)

Fig.7. Comparison of number of level with against dc source (a) Existing asymmetric versus proposed asymmetric (b) Proposed symmetric versus proposed asymmetric

Table 5. Comparison of classical configurations and the proposed configuration for 15 level output

Components	DCMLI	FCMLI	CHBMLI	Proposed MLI
No. of switches	28	28	28	8
No. of dc source	1	1	7	2+2
Output voltage	15	15	15	15
No.of driver circuits	28	28	28	8
Clamping diodes	182	-	-	-
Clamping capacitors	-	91	-	-
DC bus capacitor	14	14	-	-

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In this comparison, the proposed configuration is represented by P1 which is shown in Fig 2 (b). Babaei et al [16] proposed a series connection of submultilevel inverter to generate maximum number of levels for a given dc source which is represented by R1. A symmetric cascaded multilevel H-Bridge configuration has been presented [17] and it is represented by R2 in this comparison. The same configuration with asymmetric source is presented in [18]. The new symmetric dc source MLI by Babaei et al [19] is represented by R3. The reduced switch MLI in [20] is represented by R4 and the configuration is similar to the switched dc source MLI [4] and it is represented by R5. The new MLI topology developed in [21] is represented by R6. The hybrid structure for symmetric MLI with reduced switch in [22] is represented by R7 in this comparison.

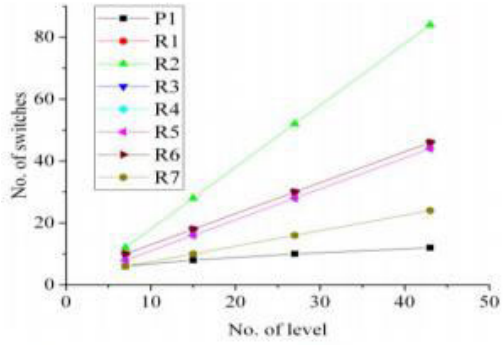

Fig.8. Comparison of switches with number of voltage levels of different topology

Fig. 8 compares the number of switches of the proposed configuration with other aforementioned configurations against the number of output voltage levels. From the Fig. 8 it is clear that the proposed configuration utilizes lower number of switches to generate a specific output voltage level. In addition, the number of switches is equal to the number of power diodes. As each switch needs a separate driver circuit, so the number of driver circuits is equal to the number of switches.

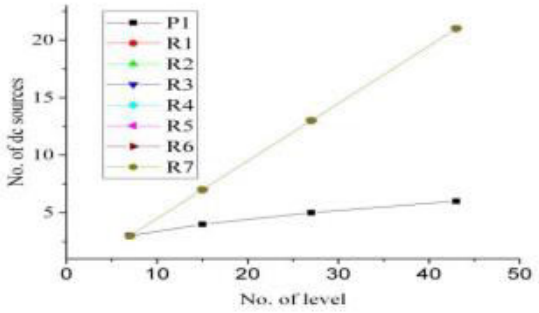

Fig.9. Comparison of dc sources against with number of levels

Fig. 9 compares the number of dc sources of the proposed configuration with the other aforementioned configurations. As it is clear thatown from the Fig. 9, the number of required dc voltage sources in the proposed configuration is less that that in the other configuration. In addition, the dc source value of the proposed configuration is less compared to the other asymmetric source configuration.

6. Simulation Result

To examine the proposed configuration, a simulation model of single phase fifteen level inverter is implemented in MATLAB/SIMULINK. The performance parameters of the proposed multilevel inverter are evaluated for SPWM and Trapezoidal PWM at different modulation indices and their comparative results are shown in Table 6, 7 and 8. The inverter is operated in open loop mode. In the previous section, switching schemes of the proposed inverter are presented. The simulation

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parameters for constant switching frequency is Vdc1=60V, Vdc2=120V, Vdcx=Vdcx′=30V. The switching frequency is 2.5 kHz. The load (R) is 100 Ω. Depending on the modulation index the proposed inverter output voltage levels will vary. The amplitude modulation index changes from 0.5 to 1. Table 6 shows the comparison table of %THD in different techniques for both sinusoidal and trapezoidal PWM respectively. From the table 6, it is obvious that the sinusoidal PWM with POD technique have low %THD when compared to the other techniques in sinusoidal and trapezoidal PWM. In addition, when the amplitude modulation index decreases the %THD of the output voltage waveform increases. Table 7 represents the comparison of fundamental rms voltage in different techniques for both sinusoidal and trapezoidal PWM. From the table 7, it can be understood that the trapezoidal PWM with APOD techniques offers high Vrms when compared to the other techniques in sinusoidal and trapezoidal PWM. As the amplitude modulation index decreases, the output voltage and as well as rms voltage (Vrms) decrease significantly. Table 8 represents the comparison of crest factor in different techniques for both sinusoidal and trapezoidal PWM. It is evident that the value of crest factor is the same for all modulation indices with different techniques for both sinusoidal and trapezoidal PWM

Table 6. %THD for Sinusoidal and Trapezoidal PWM of different modulation index and its corresponding output voltage levels

M_a	Output Voltage Levels	% THD - Sinusoidal PWM				% THD - Trapezoidal PWM			
		PD	POD	APOD	VF	PD	POD	APOD	VF
1	15	8.01	7.6	7.63	7.82	7.94	7.6	7.87	7.91
0.95		8.96	8.81	8.76	8.93	9.70	9.55	9.74	9.78
0.9		8.98	8.74	9.28	9.21	10.12	9.89	10	10.05
0.85	13	9.64	9.57	9.47	9.54	9.27	9.04	9.19	9.28
0.8		10.59	10.42	10.41	10.36	11.34	11.28	10.46	11
0.75		10.64	10.56	10.18	10.49	11.64	11.46	11.63	11.63
0.7	11	11.82	11.66	11.77	11.83	11.38	11.19	11.36	11.36
0.65		13.18	13.22	13.29	13.21	13.74	13.67	13.7	13.79
0.6		13.23	13.09	12.95	13.1	13.51	13.46	13.43	13.56
0.55	9	15.29	15.06	15.53	15.45	14.43	14.17	14.37	14.52
0.5		17.09	16.89	16.81	16.89	17.43	17.31	17.22	17.35

Table 7. V_{rms} for Sinusoidal and Trapezoidal PWM of different modulation index and its corresponding output voltage levels

M_a	Output Voltage Levels	V_{rms} - Sinusoidal PWM				V_{rms} - Trapezoidal PWM			
		PD	POD	APOD	VF	PD	POD	APOD	VF
1	15	148.4	148.6	148.4	148.4	156.1	156	156.1	156.1
0.95		141.1	138.9	141.1	139	148.2	146.2	148.2	146.1
0.9		133.6	133.7	133.5	133.5	140.4	140.3	140.4	140.3
0.85	13	126.2	126	126.2	126.2	132.6	132.6	132.6	132.7
0.8		118.8	119	118.8	118.7	124.9	125.1	124.9	124.8
0.75		111.3	111.2	111.3	111.3	117.3	117.2	117.3	117.2
0.7	11	103.9	104.1	103.9	103.9	109.2	109.1	109.2	109.2
0.65		96.48	96.59	96.53	96.49	101.4	101.6	101.5	101.4
0.6		89.03	88.86	88.97	89.02	93.66	93.29	93.62	93.68
0.55	9	81.59	81.54	81.55	81.64	85.86	86.02	85.83	85.86
0.5		74.26	74.3	74.34	74.22	78.35	78.26	78.35	78.43

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Table 8. Crest Factor for Sinusoidal and Trapezoidal PWM of different modulation index and its corresponding output voltage levels

M_a	Output Voltage Levels	Crest Factor - Sinusoidal PWM				Crest Factor - Trapezoidal PWM			
		PD	POD	APOD	VF	PD	POD	APOD	VF
1	15	1.4144	1.4145	1.4144	1.4144	1.4138	1.4147	1.4145	1.4138
0.95		1.4139	1.414	1.4139	1.4144	1.4143	1.4138	1.4143	1.4134
0.9		1.4139	1.4144	1.4142	1.4142	1.4145	1.4148	1.4138	1.4148
0.85	13	1.4144	1.4143	1.4144	1.4144	1.4148	1.4148	1.4148	1.4145
0.8		1.4141	1.4134	1.4133	1.4145	1.4147	1.4141	1.4147	1.4151
0.75		1.4142	1.4137	1.4142	1.4142	1.4143	1.4138	1.4143	1.4147
0.7	11	1.4139	1.4140	1.4139	1.4139	1.4139	1.4143	1.4139	1.4139
0.65		1.4138	1.4142	1.4141	1.4147	1.4142	1.4144	1.4138	1.4142
0.6		1.4144	1.4146	1.414	1.4143	1.4136	1.4139	1.4142	1.4144
0.55	9	1.4144	1.414	1.4139	1.4147	1.4139	1.4136	1.4144	1.4139
0.5		1.414	1.4145	1.4138	1.4147	1.4142	1.4145	1.4142	1.414

In this paper, all the output voltage waveform and their corresponding FFT graph are shown in 0.95 amplitude modulation index for simplicity and similarity. The inverter output voltage waveform and their corresponding FFT plot for PD technique are shown in Fig. 10 (a) and (b) respectively, with Sinusoidal PWM. Trapezoidal pulse width modulation for PD technique, the output voltage and their corresponding FFT graph are shown in Fig. 11 (a) and (b). The fifteen level output voltage has equal steps of 30V each and a total harmonic distortion (THD) of 8.98% and 9.88% for sine and Trapezoidal PWM respectively. The output voltage waveform and its corresponding FFT graph For POD technique are shown in Fig. 12 (a) and (b) subsequently with sinusoidal PWM. Trapezoidal pulse width modulation for POD technique, the output voltage and their corresponding FFT graph are shown in Fig. 13 (a) and (b). The total harmonic distortion (THD) for POD technique with sine and trapezoidal PWM are 8.80% and 9.74% respectively. The output voltage waveform and its corresponding FFT graph for APOD technique are depicted in Fig. 14 (a) and (b) subsequently with sinusoidal PWM. Trapezoidal PWM for APOD technique, the output voltage and their corresponding FFT graph are shown in Fig. 15 (a) and (b). The fifteen level output voltage have 8.95% and 9.89% total harmonic distortion for sine and trapezoidal PWM respectively. The simulation parameters for variable switching frequency is Vdc1=60V, Vdc2=120V, Vdcx= Vdcx′ = 30V. The Switching frequencies are 2.5 kHz and 5 kHz alternatively used in carriers. The single phase load (R) is 100 Ω. For VF technique the output voltage waveform and its corresponding FFT graph are shown in Fig. 16 (a) and (b) with sinusoidal PWM. Trapezoidal PWM for VF technique, the output voltage and their corresponding FFT graph are shown in Fig. 17 (a) and (b). The total harmonic distortion (THD) of sine and trapezoidal PWM is 9.04% and 9.98% respectively for VF technique.

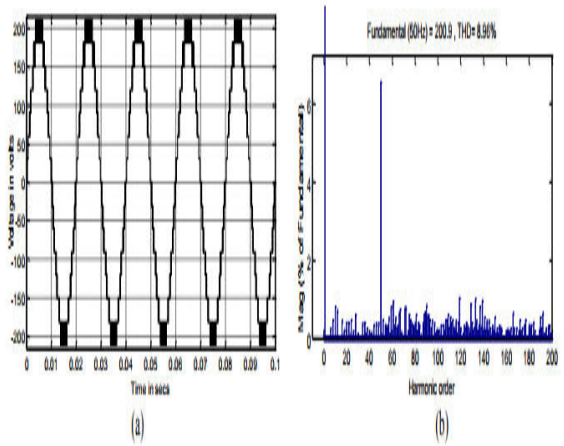

Fig.10 (a) Output voltage waveform and (b) FFT plot for PD technique with SPWM

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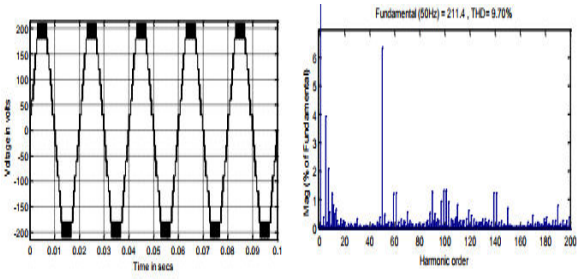
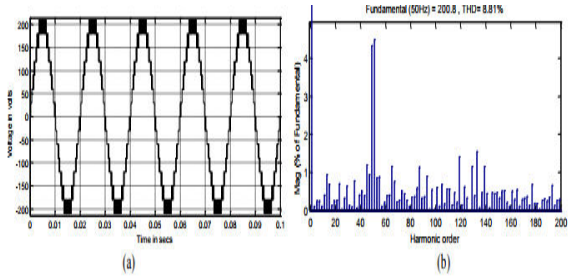


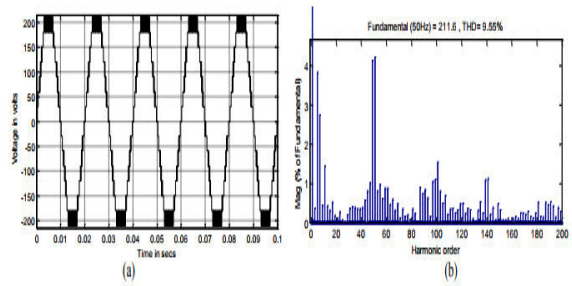
(a) (b)

Fig.11 (a) Output voltage waveform and (b) FFT plot for PD technique with Trapezoidal PWM



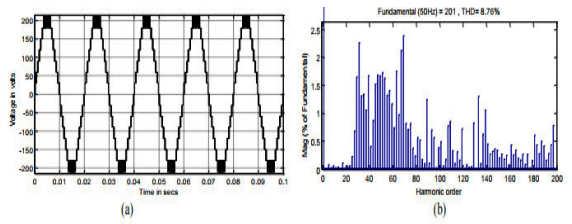
(a) (b)

Fig.12 (a) Output voltage waveform and (b) FFT Plot for POD technique with SPWM



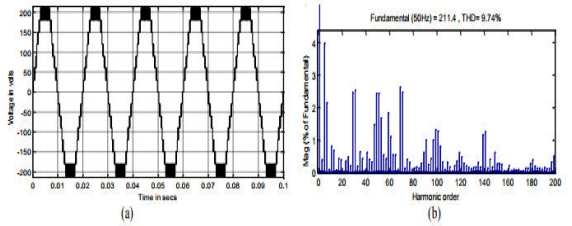
(a) (b)

Fig.13 (a) Output voltage waveform and (b) FFT Plot for POD technique with Trapezoidal PWM



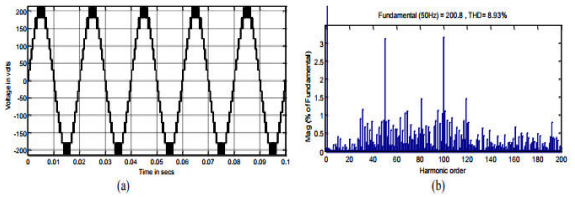
(a) (b)

Fig.14 (a) Output voltage waveform and (b) FFT plot for APOD technique with SPWM



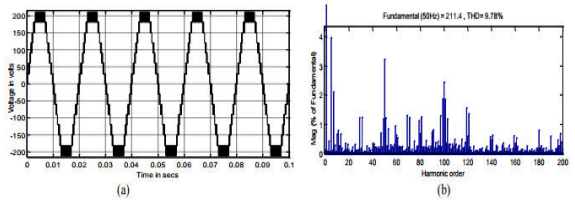
(a) (b)

Fig.15 (a) Output voltage waveform and (b) FFT Plot for APOD technique with Trapezoidal PWM



(a) (b)

Fig.16 (a) Output voltage waveform and (b) FFT Plot for VF technique with SPWM



(a) (b)

Fig.17 (a) Output voltage waveform and (b) FFT Plot for VF technique with Trapezoidal PWM

7. Conclusion

This paper proposes a new configuration to increase the number of levels in an existing MLI. The existing MLI may be either symmetric or asymmetric condition. By adding two switches per phase the output voltage level becomes double when compared to the existing MLI output voltage. The modes of operation of the proposed configuration are explained. Multi carrier pulse width modulation is adapted for the proposed configuration. Sine and Trapezoidal (Advance PWM) pulse width modulation techniques are used and their results (in terms of THD, Vrms and crest factor) are compared with different modulation indices. Sinusoidal Pulse Width Modulation (SPWM) with POD technique offers low THD when compared to the other techniques in both modulation. Trapezoidal pulse width modulation with APOD technique offers higher fundamental Vrms in output voltage compared to the other techniques. When compared to the existing MLI and other configuration, the number of switches is significantly reduced for a given number of levels in the output voltage in proposed configuration. The proposed

configuration is investigated through simulation on a single phase 15 level inverter with asymmetric source configuration. The techniques are properly adapted and their results validated for the proposed configuration. The implementation of integrating solar panel with proposed inverter can be executed along with the results in the future.

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