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# DESIGN OF FIR FILTER BASE ON IMPROVED DA ALGORITHM WITH ASIC FILTER

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**ABSTRACT**: The sigma-delta modulator based closed loop systems create high resolution, high SNR, low frequency systems. The sigma-delta analog to digital converter consists of the modulator followed by the decimation filter. In this project the planning and FPGA implementation of decimation filter, which performs the action of filtering the shaped quantization noise and changing one-bit data stream into 20 bit high-resolution output is reported. The multi-stage decimation methodology is customized, with the Cascaded Integrator Comb (CIC) filter followed by a FIR filters. The specifications of decimation filter are derived from the specifications of a 3rd-order single bit sigma-delta modulator. Distributed arithmetic algorithm is employed to design FIR filters. The hardware model for the filter is developed using verilog HDL.

## I.INTRODUCTION

The Finite Impulse Response (FIR) Filter is the important component for designing an efficient digital signal processing system. So, in this project, a FIR filter is constructed, which is efficient not only in terms of power and area but also in terms of delay. When considered the elementary structure of an FIR filter, it is found that it is a combination of multipliers and delays, which in turn are the combination of adders. Thus, adders serve as the basic components in the implementation of an FIR filter. Moreover, addition is one of the fundamental arithmetic operations, used extensively in many VLSI systems such as microprocessors and application specific DSP architectures.FIR Stands for Finite Impulse Response filter and it is also known as non-recursive filter and convolution filters. These are digital filters that have a finite impulse response. FIR filter operates only on current and past input values. FIR filters perform a convolution of the filter coefficients with a sequence of input values and produce an equally numbered sequence of output values.

## II. LITERATURE SURVEY

FIR filters are having finite impulse so we can eliminate more noise compared to IIR filters. Where IIR operates at infinite impulse which is practically impossible. The block diagram of the FIR filter consists of an amplifier to increase the strength of given input singal,followed by the A/D's and D/A's,Address Generator,SRL,LUT's and shift summation tables.Since FIR is a Digital filter its capable of receiving digital input

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instead of analog input.This FIR is implemented by using DA algorithm ( Distributed Arithmatic algorithm).The complicated multiplication operation is converted to the shifting and adding operation when the DA algoithm is directly applied to realize linear time-invariant since linear time-variant systems are practically not exist. However the scale of the LUT will increase exponentially with the coefficient. If the coefficient is small, it is very convenient to realize through the rich structure of LUT while the coefficient is large, it will take up to a lot of storage resources of LUT and reduce the calculation speed adopted to improve the speed of calculation.

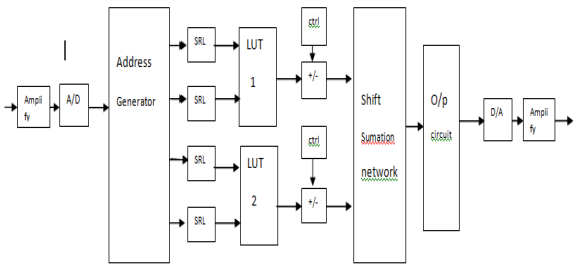


FIG.1 EXISTED SYSTEM

The Look-up Table is used to reduce processing time for applications that uses complex calculations. Generally The LUT contains data or results from the complex calculations needed by the application, which was already done beforehand once. By keeping the results in the LUT, when the application needs the values, instead of having to do the calculations, it can refer to the LUT retrieve the Values from it, bypassing the calculations. The LUT used in complex applications such as signal processing, image processing, device modeling, etc., rather than in digital filters. FIR only used when the filter coefficients are constant. The well-known multiple-constant multiplication based technique is widely used to implement FIR filters. A based structure requires a large chip area and consequently enforces a limitation on the maiximum possible order of the filter that can be realized for high throughput applications. In Conventional DA implementation whatever may be implemented it was permanently stored in the memory and it is only because of the impulse response coefficients are fixed, this behavior makes it possible to use ROM-based LUTs. For a Reconfigurable DA-based FIR filter whose filter coefficients dynamically change, we need to use rewritable RAM based LUT instead of ROM - based LUT. Efficient schemes for the optimized shared-LUT implementation of Reconfigurable FIR filters using DA technique, where LUTs are shared by the DA units for bit slices of different weitage. The FIR filter coefficients can be dynamically change in runtime with a very small reconfiguration latency.

## III. PROPOSED SYSTEM

ASIC stands for Application Specific Integrated Circuit. It is used for particular Application. When we are using ASIC we can reduce the area as well as power consumption.The block diagram consists of N number of sections to get efficient output. The basic blocks are serial-in parallel out shift registers, partial product generators,pipeline adder trees and shift –

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accumulator. In this the input samples x(n) arriving at every sampling instant are fed to a serial-in-parallel out shift register (SIPOSR) of size N. The SIPOSR decomposes the N recent most samples to P and feeds them to reconfigurable partial products.For high through put implementation, the RPPG generates L partial products corresponding to L bit slices in parallel using the LUT composed of single register bank. If the size of LUT becomes too large, and the LUT access time also becomes large. So we are using single LUT of small size instead of using two different LUT's and the entire size of LUT is based on order of the filter. The straight forward DA-based implementation is, therefore, not suitable for large filter order so we are using improved DA algorithm. A shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters [1], communication receivers [2], and image processing ICs. Recently, as the size of the data continues to increase due to the high demand for high quality data, the word length of the shifter register increases to process large data in image processing ICs. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches. Serial-in/parallel-out (SIPO) shift register is used to convert data from serial format on a single wire to parallel format on multiple wires.The input of an SIPO register is x(n) and generates different partial products in R time slots of same duration as the operating clock period so that we have one filter output at every R cycles. The output of the shift register (SIPO) will be giving to DRPPG i.e. DRAM- based partial product generator, and each section consists of P DRAM-based RPPGs. The PAT to calculate the right most summation, followed by shift-accumulator that performs over R cycles according to the second summation.

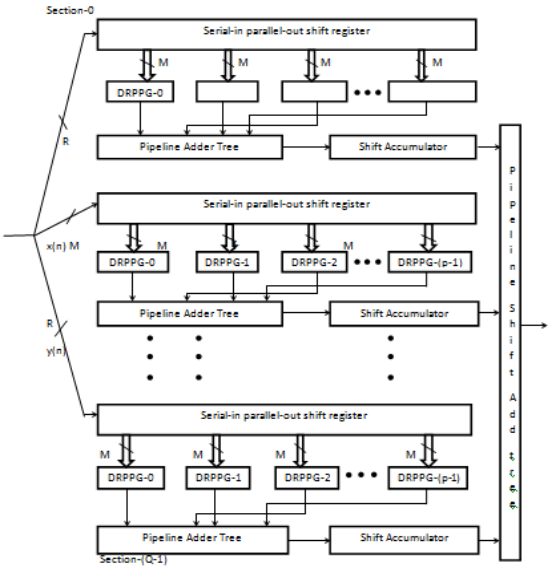


FIG.2 PROPOSED SYSTEM

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An Application-Specific Integrated Circuit (ASIC) is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use. Intermediate between ASICs and industry standard integrated circuits, like the 7400 or the 4000 series, are application specific standard products (ASSPs).Modern ASICs often include entire 32-bit processors, memory blocks including ROM, RAM, EEPROM, Flash and other large building blocks. Such an ASIC is often termed as SoCs (system-on-a-chip). We can describe the functionality of the ASICs by using either Verilog or VHDL.

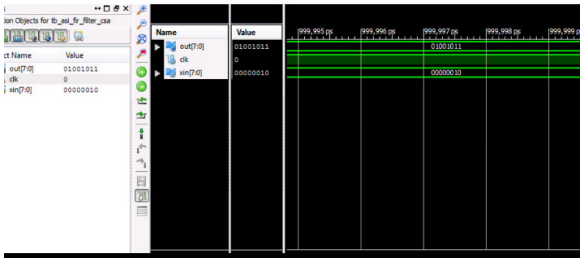

FIG.3 OUTPUT

## IV.CONCLUSION

If the DA algorithm is directly applied in FPGA to understand FIR filter, it is difficult to attain because of constant coefficients. The memory utilized and lookup table speed are very less due to concrete hardware realization of the FPGA circuit. So we are using improved DA algorithm and ASIC filter to reduce the complexity in the circuit and improves memory utilization and lookup table speed using RAM based LUT's where the coefficients varies dynamically. Since this improved system produces efficient output rather than existing output.

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