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PERFORMANCE EVALUATION OF MULTI LEVEL CASCADED TYPE FAULT CURRENT LIMITING DYNAMIC VOLTAGE RESTORER

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ABSTRACT: This paper proposes a new fault current limiting dynamic voltage restorer (FCL-DVR) concept. The new topology uses a bidirectional thyristor switch across the output terminals of a conventional back-to-back DVR. In the event of a load short, the DVR controller will deactivate the faulty phase of the DVR and activate its thyristor to insert the DVR filter reactor into the grid to limit the fault current. A fault condition is detected by sensing the load current and its rate of change. The FCL-DVR will operate with different protection strategies under different fault conditions. Design of the FCL-DVR involves selecting important parameters, such as DVR power rating, dc link voltage of the DVR, output filter reactors and capacitors, and grid-tied transformers is proposed. The model of a three phase grid system with different fault conditions described. A new multilevel cascaded-type dynamic voltage restorer (MCDVR) is introduced to reduce the ratio of the transformer. The MCDVR provides similar cascade inverter performance benefits, such as the lower power rating and cost of the power devices used. The FCL and DVR comparative analysis is simulated by using MATLAB / SIMULINK software.

Key Words: Dynamic voltage restorer (DVR), multilevel inverters, fault current limiter, voltage restoration.

I. INTRODUCTION

The advanced power network must manage the two noteworthy difficulties that they are: voltage changes and short out shortcomings. With wide utilization of variable and nonlinear burdens, the framework experiences power quality issues like voltage vacillation, voltage irregularity, symphonious twists and other. In the meantime, numerous power loads turn out to be more delicate to these unsettling influences [1] [2]. The fast multiplication of renewable power era sources in the network has exasperated these power quality issues [3]–[6].

Besides, cut off stay a standout amongst the most well-known blames in the network and cause incredible attentiveness toward matrix security and steadiness. A strong state blame current limiter (FCL) can be utilized to utmost blame currents in the matrix [7]–[10]. At the point when a short out blame happens, the strong state FCL embeds high arrangement impedance in the power circle and in this manner adequately constrains the blame current [11]. Notwithstanding, amid ordinary operation of the network the FCL work in a no heap mode, bringing about traded off energy transformation effectiveness and gear use proficiency. Then again, a dynamic voltage restorer (DVR) can be utilized to adjust for the vacillations of the framework voltage [12]. For some power systems, it would be enormously profitable to give both voltage remuneration and blame current restricting capacities by a solitary power electronic contraption. In the control methodology of a routine DVR is extended to offer extra blame current intrusion highlights. Be that as it may, this approach requires a three-crease increment in power rating of the DVR, prompting a sharp increment in framework cost [13-15]. In this paper, a new concept of fault current limiting dynamic voltage restorer (FCL-DVR) is proposed. The new topology can operate in two operational modes: 1) compensation mode for voltage fluctuation and unbalance; and 2) fault current limiting mode. It should be noted that only one additional crowbar bidirectional thyristor switch is added across the output terminals of each phase of the conventional DVR, greatly simplifying its implementation. Furthermore, the new FCL-DVR can maintain the same power rating as the conventional DVR without FCL function.

II. MCDVR TOPOLOGY

The MCDVR system based on multilevel inverters is shown in Fig.1. It consists of a series-connected transformer T_1, an energy-storage capacitor C_{dc}, a seven-level cascade inverter, and a filter. The transformer T_1 not only reduces the voltage requirement of the inverters, but also provides isolation between the inverter and the utility grid. There are also anti-parallel thyristors *K*, which are the main difference between the MCDVR and traditional DVRs [19]. In most practical inverters, there is also a bypass switch connected in parallel with the injection transformer [18]. Importantly, the energy-storage capacitor (C_{DC}) provides the required power to compensate for any voltage sag or fluctuation in the utility grid. Although low-order harmonics are eliminated by the cascaded H-bridge, a large number of high-order harmonics are still presently close to the equivalent switching frequency [18], [20]. As a result, an *LC* filter comprised of L_f and C_f is used as the filter for the cascaded multilevel DVR, as well as an impedance to limit the fault current. Thus, the *LC* filter can achieve two different functions, and this will help promote the full utilization of the equipment.

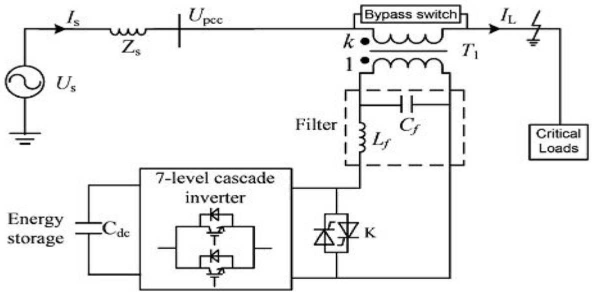

Fig.1. Schematic diagram of the proposed MCDVR.

A. Function of the MCDVR

Under normal operating conditions, the anti-parallel thyristors are not fired. Thus, the proposed MCDVR is effectively seen as only being comprised of the H-bridge cascade DVR. This multilevel converter not only realizes the higher power and voltage ratings using smaller rating switches, but also reduces the overall harmonic content. In addition, it contributes to a smaller in the output and, thus, reduces unwanted electromagnetic interference (EMI) [21].On the other hand, when a short-circuit fault occurs along the distribution line, the load current increases sharply. The thyristors are then activated to insert the filter into the main current path through the series transformer. The filter, the series transformer, and the anti-parallel thyristors together form variable impedance that operates as the current-limiting module. The fault current is limited to the desired value, and the components of the VSI and other equipment in the system can be protected. Since the voltage across the series transformer is not the same in different modes, the mathematical model of the MCDVR is

$$U_{\text{DF-DVR}} = k\alpha U_{\text{dc}} \operatorname{sgn}(x) + Z_{\text{lim}} I_{\text{fault}} \left(1 - \operatorname{sgn}(x)\right) \tag{1}$$

Where U_{dc} is the dc-link voltage, k is the turns-ratio of the series transformer, and α is the modulation depth. Importantly, *sgn (x)* is the return function, and x is any valid value. For example, if the system is in the voltage regulation mode, $x = 1$ and $\operatorname{sgn}(x) = 1$. Thus, (1) can be rewritten as

$$U_{\text{DF-DVR}} = k\alpha U_{\text{dc}}. \tag{2}$$

Instead, if the system is in the current-limiting mode, $x = 0$ and $\operatorname{sgn}(x) = 0$. Then, (1) can be rewritten as

$$U_{\text{DF-DVR}} = Z_{\text{lim}} I_{\text{fault}} \tag{3}$$

B. Current Limiting by the MCDVR

The single-phase equivalent circuit of the MCDVR in current-limiting mode is shown in Fig.2. When a short-circuit fault occurs, the insulated-gate biploar transistors (IGBTs) of the faulted phase in the voltage-source inverter (VSI) are turned off, and the cascade inverter is shut down. Then, the thyristors are activated. Thus, the filter is inserted into the main current path through the series transformer T_1, as shown in Fig.2 (a).

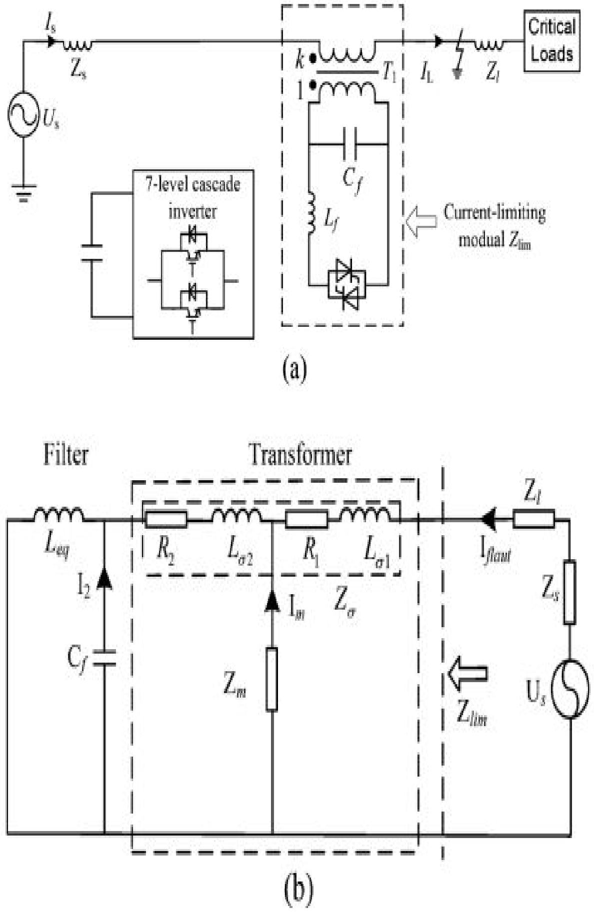

Fig.2. MCDVR in the current-limiting condition: (a) Schematic diagram. (b) Single-phase equivalent circuit.

The short-circuit current during the fault is then

$$I_{\text{fault}}(t) = \frac{U_s(t)}{Z_s + Z_l + Z_{\text{lim}}} \approx \frac{U_s(t)}{Z_{\text{lim}}} \tag{4}$$

Where Z_{lim} is the limiting impedance. As $Z_{lim} \gg Z_s + Z_{li}$, the I_{fault} is mainly determined by the magnitude of Z_{lim}. Consequently, it can be limited to the desired value to protect the equipment in the system. Z_{lim} is determined by $L\sigma_1$, $L\sigma_2$, R_1, R_2, L_m, C_f, and $L\sigma_1$and R_1 are the leakage reactance and resistance of the primary side, respectively. $L\sigma_2$and R_2 are the leakage reactance and resistance of the secondary side, respectively. Z_m is the excitation impedance of the transformer.Referring to Fig.2 (b), C_f is usually a small value and, $\left|\frac{1}{j_\omega C_f}\right|$ hence, is typically a large value. Furthermore, the influences of $L\sigma_1$, $L\sigma_2$, R_1, R_2can be ignored. It can then be concluded that the limiting impedance is

$$|Z_{\text{lim}}| \approx k^2(|j\omega L_{\text{eq}}|//|(1/j\omega C_f)|//|Z_m|) \tag{5}$$

Where L_{eq} is the equivalent impedance and therefore

$$L_{\text{eq}} = L_f \cdot \frac{\pi}{2\pi - 2\delta + \sin 2\delta} \tag{6}$$

Where $\delta$is the trigger delay angle of the thyristors. In reality, $|Z_m| \gg k^2|j_\omega L_{eq}| and \left|\frac{1}{j_\omega C_f}\right| \gg |j_\omega L_{eq}|$. Thus, I_{fault} is mainly determined by$|j_\omega L_{eq}|$. Hence, the short-circuit current can be limited to the desired value by a suitable selection of α, L_f and k.

III. CONTROL SCHEME DESIGN AND OPTIMAL PARAMETER SELECTION

The MCDVR can operate in one of the two operation modes according to the state of the grid. In this section, the control scheme design and optimal parameter selection are explained.

A. Control Scheme

The primary drawback of the H-bridge inverter is the possibility of accidentally short-circuiting the input dc-link voltage by simultaneously switching on both transistors in a leg of the inverter. This is why, in such converters, a dead time is typically introduced to avoid this shoot through and large over currents. New cascade inverters have also been proposed to solve this shoot-through problem, and they can greatly improve the overall system reliability [22], [23]. In this paper, the cascaded H-bridge inverter is adopted as it is widely used [16], [24].When the MCDVR is in the voltage compensation mode, it consists of a multilevel inverter with three H-bridge cells in each phase (synthesizing a 7-level output voltage), a small filter at the ac side, and three dc-link capacitors. One of the main advantages of this topology, compared to other multilevel topologies, is that the maximum number of levels is only limited by isolation constraints. Moreover, the modular structure of the converter leads to advantages in terms of manufacturing and overall system flexibility [24].Much research has been conducted on the control methods of cascade inverter-based DVRs [5], [12]–[16]. The phase-shifted PWM is a widely used modulation strategy for cascaded multilevel inverters as it offers an even power distribution among the cells and is very easy to implement independent of the number of inverters. This modulation shifts the phase of each carrier by a suitable angle to reduce the overall harmonic content of the output voltage [25]. Since it offers numerous benefits, the outlined inverter design and modulation strategy are used in this paper. Moreover, the voltage compensation control strategy for an MCDVR system, as described in [4], is used.When the MCDVR is in fault current-limiting mode, it operates as discussed previously. This paper mainly focuses on the fault current detection method and the transient state of the fault current limiting operation mode. A fault current detection method is developed to sense the load current and its rate of change. The fault current is consequently limited to an acceptable level rapidly, even before reaching its first peak [26], [27]. The schemes of the unbalanced disturbance are adopted [15], and are not discussed in this paper for brevity. The details of the transient state of the MCDVR are described.

B. Optimal Parameter Selection

1) Cascaded Inverter Design: Using a PWM control strategy, the switches in the multilevel inverters should satisfy the following conditions:

$$N_S \geq (U_{dvr}/n)/kU_r \tag{7}$$

$$N_P \geq (kI_L)/I_r \tag{8}$$

Where N_S and N_P are the number of series switches in each inverter level and parallel branches in each leg of the inverter, respectively. U_{dvr} is the rated peak value of the series injected voltage of the MCDVR. I_L is the rated value of the load current. U_r and I_r are the rated blocking voltage and the rated current of each switching component, respectively. n is the total number of inverter levels in each phase. Then, the rated dc-link voltage of each inverter level U_{dch} should meet

$$U_{dvr}/n \leq U_{dch} \leq N_S U_r. \tag{9}$$

From (7) – (9), the overall minimum capacity of the switching devices can be obtained

$$S_{min\_total} = nN_{S\_min}N_{P\_min}U_r I_r \geq U_{dvr}I_L \tag{10}$$

Where N_{Smin} and N_{Pmin} are the minimum values of N_S and N_P, respectively. $S_{mintotal}$ is the total minimum capacity of the multilevel inverters. It can be concluded that the capacity of the switching device, which is dependent on U_r and I_r, can be altered by setting the values of the turns ratio k, N_{S_min} and N_{Pmin}.

When a short-circuit fault occurs (e.g., a three-phase to ground fault), the fault current will be 6–10 times that of the normal load current. Let us assume that the fault current is λ times greater than the load current in steady state. When a short-circuit fault occurs, the secondary current is $k\lambda$ times greater than that of the load current. The ratio of the series transformer is 8:1 in [15], while the ratio is reduced to 3.5:1 in this paper. The change in the fault current at different transformer ratios is shown in Fig.3.3. The fault occurs at t_{fault} and MCDVR enters into the current-liming mode at t_{limit}. Δt is the fault detection period. The secondary current $I_{fault\_Pre} = 8I_l$ during Δt in [19], while $I_{fault\_Pre} = 3.5I_l$ in this paper. Thus, by decreasing the turn's ratio, the secondary-side current during the preliminary period of the fault (where the limit module is not in series with the line) can be reduced. Overall, this will help to reduce the impact on the IGBTs and dc bus capacitor. After t_{limit}, the MCDVR enters the limiting mode and the fault current is limited to the desired value.

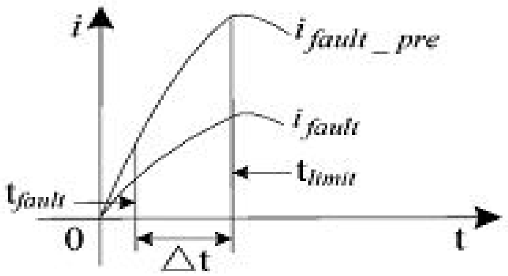

Fig.3. Change in the fault current at different ratios of the series transformer.

2) Fault Current-Limiting Module Design: When the MCDVR operates in the fault current–limiting mode, the fault current will flow through the series transformer T_1, LC output filter, and the bidirectional thyristors. The series transformer withstands the supply voltage during the faults and, hence, the capacity of the series transformer is

$$S_T \geq U_S I_{\text{fault}}. \tag{11}$$

In addition, the thermal stability of L_f and the maximal withstand voltage of C_f should be considered during the faults. This relation is expressed as

$$Q_{L_f} \geq \int_{t_{\text{fault}}}^{t_{\text{return}}} (k i_{\text{fault}})^2 dt \tag{12}$$

Where Q_{Lf} is the thermal stability of L_f during the fault. t_{fault} and t_{return} are the time of the fault occurring and disappearing, respectively. Since the filter capacitor can be easily damaged by the over voltage

$$U_{C_f} \geq \max(u_{S_{\max}}/k, u_{\text{dc}}) \tag{13}$$

Where $U_{Cf}$is the maximal withstand voltage of the filter capacitor. $u_{dc}$and $u_{Smax}$are the dc voltage and the maximum voltage across the series transformer, respectively.When the thyristors are deactivated, the voltages between the thyristors are the same as the output voltage of the cascade converter. The maximum value of the output voltages is approximately equal to the dc-side voltage, while the current flowing through the thyristors is zero. When the thyristors are activated during the fault, the current flowing through the thyristor is k times of the fault current at the primary side. Thus, the thyristors can be given by

$$Q_{\text{thy}} \geq \int_{t_{\text{fault}}}^{t_{\text{return}}} (k i_{\text{fault}})^2 dt \tag{14}$$

$$U_{\text{thy}} \geq \max(u_{cf}, u_{\text{dc}}) \tag{15}$$

Where Q_{thy} is the thermal stability of the thyristors, and U_{thy} is the maximal withstand voltage of the thyristors. Also, u_{cf} is the voltage of the filtering capacitors and $u_{cf}= u_s/k$

3) Ride-Through Capability: Assuming that the magnitude of the voltage sag (with no phase-angle jump) is U_{sag} in per unit, the MCDVR should inject an active power given by to restore the presag-rated voltage U_L at the load terminals [14]

$$P_{\text{DVR}} = -C_{\text{dc}} u_{\text{dc}} du_{\text{dc}}/dt = \sqrt{3} U_L I_L \cos\varphi_L (1 - U_{\text{sag}}) \tag{16}$$

Here, the load current I_L and the power factor $\varphi_L$are assumed to be constant. Furthermore, $P_L = \sqrt{3} U_L I_L cos\varphi_L$ is the rated load power. If t_{sag} is the voltage sag duration, the energy to be supplied by the MCDVR is

$$\begin{aligned} W_{\text{DVR}} &= \int_{t_0}^{t_0+t_{\text{sag}}} \left(-C_{\text{dc}} u_{\text{dc}} \frac{du_{\text{dc}}}{dt}\right) dt \\ &= \int_{t_0}^{t_0+t_{\text{sag}}} P_{\text{L}}(1 - U_{\text{sag}}) dt. \end{aligned} \tag{17}$$

Then

$$-C_{\text{dc}} \left[u_{\text{dc}}^2(t_0 + t_{\text{sag}}) - u_{\text{dc}}^2(t_0)\right]/2 = P_L t_{\text{sag}} (1 - U_{\text{sag}}) \tag{18}$$

If the initial dc-link voltage is assumed to be its rated value, then $u_{dc}(t_0) = U_{dc0}$. Also, $u_{dc}(t_0 + t_{sag}) = k_d U_{dc0}$, where $k_d U_{dc0}$is the minimum-allowable dc-link voltage at the end of the voltage sag ($0 < k_d < 1$). Thus, in order to compensate the maximum voltage sag magnitude for a maximum expected sag duration $U_{sag,max}$, the capacitance should be

$$C_{\text{dc}} \geq 2 P_L t_{\text{sag,max}} (1 - U_{\text{sag,max}}) / U_{\text{dc0}}^2 \left(1 - k_{\text{d}}^2\right) \tag{19}$$

Increasing U_{dc0} allows the reduction of the size of the dc capacitor, but the choice of that voltage also depends on the maximum voltage rating of the H-bridge power-electronic devices. Furthermore, the capacitor voltage rating also limits the maximum injection voltage. Two balancing schemes are adopted [28], and are not discussed in this paper for brevity.

4) LC Design: Although the equivalent switching frequency of the cascade multilevel inverter is very high (e.g., 15 kHz), there are several higher harmonic components near the equivalent switching frequency. To attenuate these components and effectively lower the ripple voltages and currents, an LC-based filter is proposed. Setting the resonance frequency of the filter as f_c, then $2\pi f_c L_f = 1/2\pi f_c L_f$. The equivalent resistance of the inverter on the dc link can be calculated as follows [29]:

$$R_L = 3U_{\mathrm{dc}}^2/P_{\mathrm{DVR}}. \tag{20}$$

Hence, the resonance frequency is

$$f_c = 1/2\pi\sqrt{L_f C_f} = \sqrt{L_f/C_f}/2\pi L_f. \tag{21}$$

In most engineering applications, a damping factor of $\rho = (0.5 \sim 0.8)R_L$ is present [15]. Assuming that the damping factor $\rho = \sqrt{L_f/C_f}$, then according to (3.20) and (3.21), L_f and C_f can be calculated as

$$\begin{cases} L_f = \rho/2\pi f_c \\ C_f = L/\rho^2 = 1/2\pi f_c \rho \end{cases} \tag{22}$$

The rated current in L_f is mainly determined by the fault current, which is described.

5) DC-Link Capacitor Protection: Varistors are well-known components often used to clamp overvoltage transients [8], [9], [30], [31]. In this paper, varistors are designed to protect the dc-link capacitor. Moreover, the overvoltage protection and under voltage protection of the dc-link capacitor are also applied in the software.

IV. TRANSIENT STATE ANALYSIS

A. From Compensation Mode to Current-Limiting Mode

The forward switching scheme (from the compensation mode to the current-limiting mode) is to isolate the VSI from large currents during faults. The scheme achieves this by rapidly adding a limiting impedance in series with the transmission line to limit the short-circuit current to the desired value. Since the scheme involves the state changes of the multilevel inverters and thyristors, the forward switching sequence is given in Fig.4.When a short-circuit fault occurs at t_1, the line current increases rapidly. Once the current magnitude exceeds a preset threshold i_t (which depends on the relay protection) at t_2, the IGBTs are turned off to completely deactivate the inverter. Considering the sensing time of the fault detector, the dead time and non ideal characteristics of the switches, the IGBTs are actually turned off at t_3. Then, the control system gives a trigger signal to the thyristors at t_4. Considering the non ideal characteristics of the thyristors, the path K through the thyristors is in conduction at t_5. Then, forward switching is finally completed.

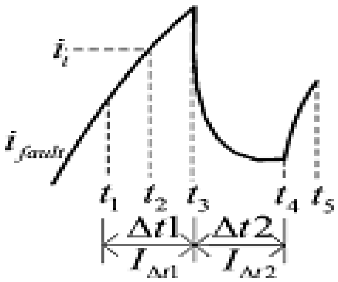

Fig.4. Trend of the fault current during the forward switching scheme.

1) During Δt_1, the fault current mainly depends on the system impedance Z_s, and the leakage impedance $Z\sigma$ of the series transformer [30]. Thus,

$$I_{\Delta t1}(t) = U_s(t)/(|Z_s + Z_\sigma|). \tag{23}$$

From Fig.4, it is evident that the fault current $I_{\Delta t1}$ increases sharply. The duration time Δt_1 is very important to other devices and hence a fast fault current detection method is necessary.

2) During Δt_2, the MCDVR includes the supply power U_s, the series transformer, and the filter capacitor C_f. The equivalent circuit is shown in Fig.5. Thus,

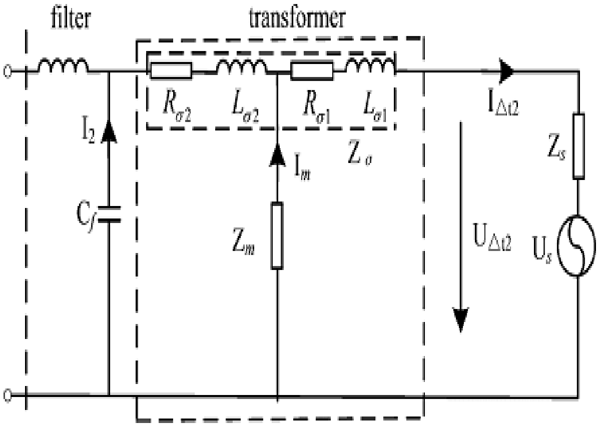

Fig.5. Equivalent circuit of the MCDVR during Δt_2.

$$I_{\Delta t2}(t) = U_{\Delta t2}(t)/|Z_m| + U_{\Delta t2}(t)/|1/j\omega C_f| \tag{24}$$

Where$Z_m \gg Z_\sigma$, and $Z_\sigma$is ignored. For the series transformer, the values of the excitation impedance $Z_m$and $|1/j_\omega C_f|$ are large, and hence $I_{\Delta t2}$ is much smaller than $I_{\Delta t1}$

3) During the switching process of the thyristors, the fault current will increase. After the thyristors are activated, the fault current I_{fault} is determined mainly by the limiting impedanceZ_{lim}, as given in (5). From (4) and (25), as $Z_{lim}$is much smaller than $Z_m$and $|1/j_\omega C_f|$, I_{fault} is larger than $I_{\Delta t2.}$

B. From Current-Limiting Mode to Compensation Mode

The backward switching scheme (from the current-limiting mode to the compensation mode) is to turn off the thyristors after the fault. This scheme involves the state changes of the multilevel inverters and the thyristors, and the backward switching sequence is given in Fig.6.

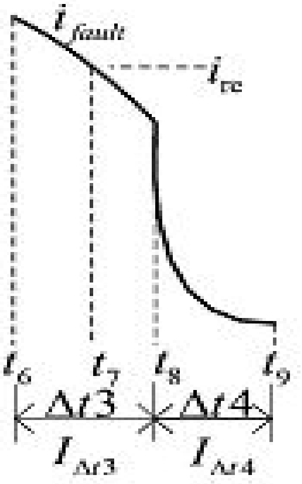

Fig.6. Fault current during the backward switching scheme.

The short-circuit fault disappears at t_6. If the magnitude of the load current is less than the return current i_{re} at t_7, the control system removes the trigger signal to the thyristors. i_{re} is the reference value of the fault detection, and is larger than the peak value of the load current. When the voltage across the thyristors is negative in polarity and the current is under the maintaining current, the thyristors are turned off at t_8. Then, all of the IGBTs in the inverter are turned on at t_9. Thus, the thyristors are still activated for the period Δt_3 (from t_6 to t_8) and are turned off during Δt_4 (from t_8 to t_9).

1) During Δt_3, the fault disappears. The equivalent circuit is shown in Fig.3.7. It

includes the power supply U_s, the limiting modules, and the load Z_{Load}. Ignoring Z_s and Z_l, the voltage across the current-limiting module is

$$U_{\Delta t3}(t) = U_s(t) - U_{\text{Load}}(t) \tag{25}$$

Since the leakage impedance Z_σ is ignored

$$I_{\Delta t3}(t) = U_{\Delta t3}(t)/(|Z_m//(1/j\omega C_f)//j\omega L_f|). \tag{26}$$

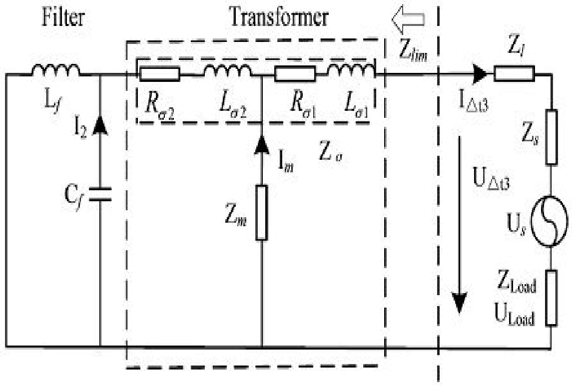

Fig.7. Equivalent circuit of the MCDVR during Δt_3.

2) During Δt_4, the thyristors and the IGBTs are also turned off. The equivalent circuit of the system is shown in Fig.8. It includes the supply power U_s, the series transformer, and the load Z_{Load}. Thus, the load current is

$$I_{\Delta t4}(t) = U_{\Delta t4}(t)/(|Z_m//(1/j\omega C_f)|). \tag{27}$$

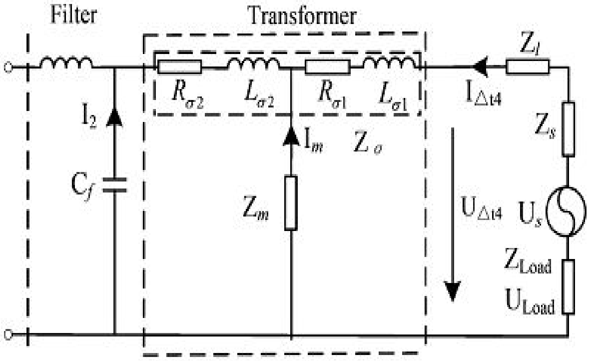

Fig.8. Equivalent circuit of the forward switching sequence during Δt_4.

From (26) and (27), because $|1/j_\omega C_f|$ is much smaller than $|Z_m|$ and $|1/j_\omega C_f|$, $I\Delta t_3$ is larger than $I\Delta t_4$. After the backward switching sequence, the line current will recover to the normal value.

V. FAULT CURRENT LIMITER

Many factors can cause a fault in a power system. The fault current level can be relatively large, which may damage equipment in the power system and even cause permanent failure. Power systems have to be designed to withstand mechanical and thermal stresses during a fault. Power system protection devices detect fault conditions and operate circuit breakers and other devices to limit the damage side in order to limit the fault current. Today, fault current levels in land-based distribution systems are of increasing concern because they are generally rising due to the increasing capacity of connected distributed generation. Increasing fault current levels will require expensive network investment in upgrading equipment such as circuit breakers and transformers. There is a growing need therefore for fault current limiting devices embedded into electrical networks to avoid a large scale and expensive upgrade of existing switchgear. FCLs are expected to reduce fault current levels without adding additional impedance during normal operation. The capital cost of purchasing and installing FCLs must be less than the cost of upgrading the existing equipment before they can be attractive for commercial applications.

VI. MATLAB/SIMULATION RESULTS

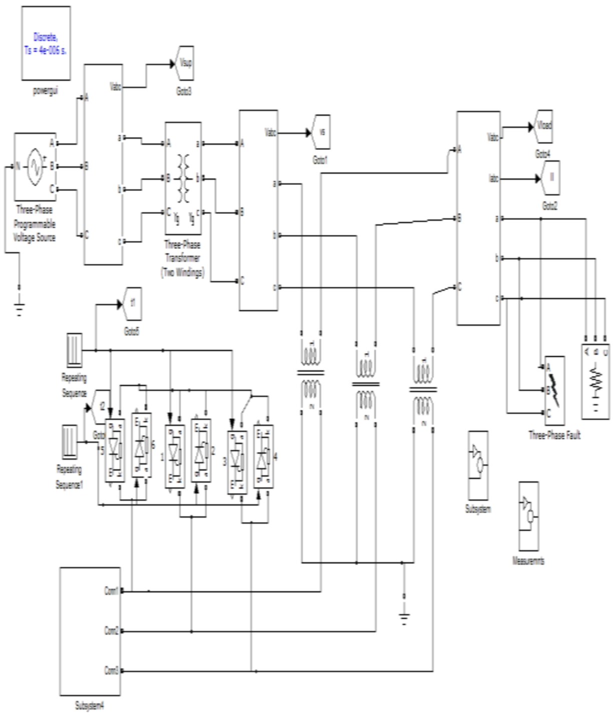

Fig.9 Simulink model of MCDVR

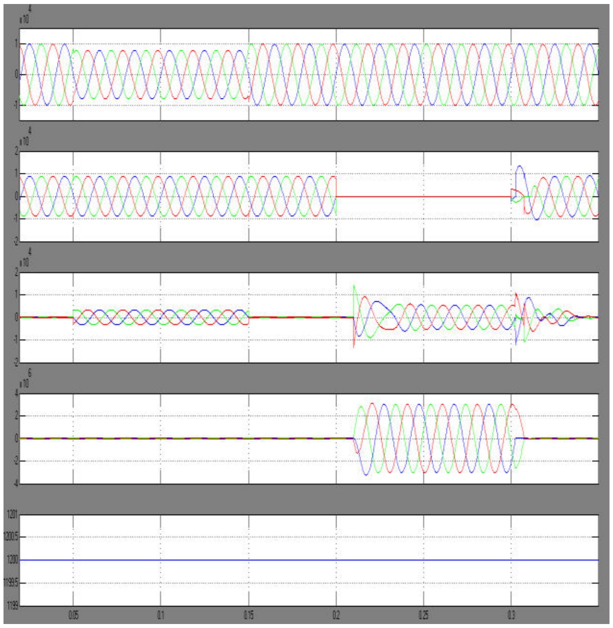

Fig.10 Simulation results of the MCDVR system. Top to bottom: (a) the supplyvoltage, (b) the load voltage, (c) the secondary voltage, (d) the load current, and (e) the dc-link voltage.

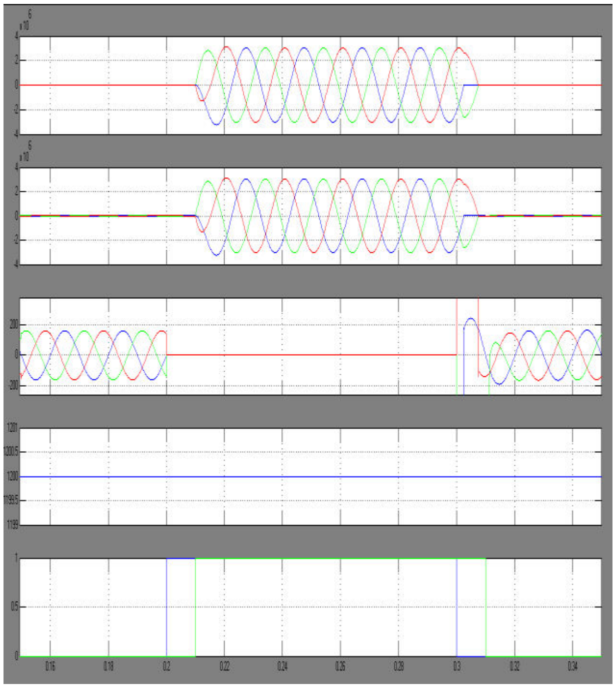

Fig.11 Forward switching simulations of the MCDVR system, top to bottom: (a) the load current, (b) the current in the thyristors path, (c) the outputcurrent of the VSI, (d) the dc-link voltage, and (e) the timing sequence.

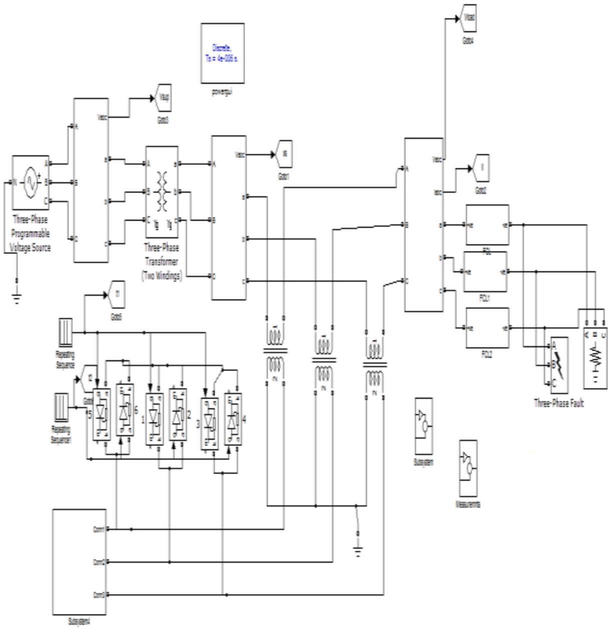

Fig.12 Simulink model of MCDVR with Fault Current Limiter (FCL)

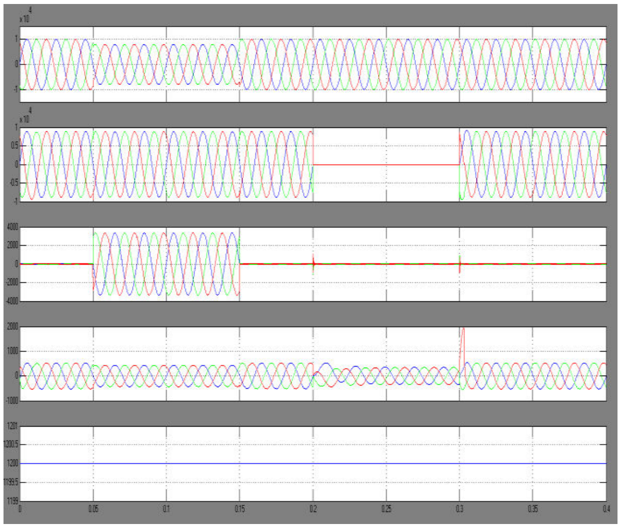

Fig.13 Simulation results of the MCDVR system. Top to bottom: (a) the supplyvoltage, (b) the load voltage, (c) the secondary voltage, (d) the loadcurrent, and (e) the dc-link voltage.

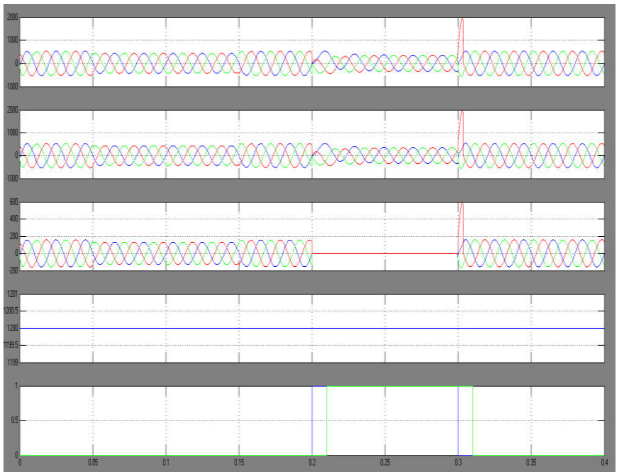

Fig.14 Forward switching simulations of the MCDVR system, top to bottom :(a) the load current , (b) the current in the thyristor's path, (c) the outputcurrent of the VSI, (d) the dc-link voltage , and (e) the timing sequence.

VII. CONCLUSION

A new FCL-DVR concept is proposed to deal with both voltage fluctuation and short current faults. The new topology uses a crowbar bidirectional thyristor switch across the output terminals of a conventional back-to-back DVR. In the event of load short, the DVR controller will deactivate the faulty phase of the DVR and activate its crowbar thyristor to insert the DVR filter reactor into the grid to limit the fault current.The FCL-DVR will operate with different protection strategies under different fault conditions.Based on theoretical analysis, simulation and experimental study, we conclude the following.

1) With the crowbar bidirectional thyristor across the output terminal of the inverter, the proposed FCLDVR can compensate voltage fluctuation and limit fault current.

2) The FCL-DVR can be used to deal with different types of short faults with minimum influence on non-fault phases. The FCL-DVR has the same power rating as a conventional DVR.

3) The delta-connection mode of the shunt transformers minimizes the influence of dc link voltage fluctuations and suppresses the 3rd harmonics.

4) The proposed control method can detect faults within two cycles.

5) The design methodology based on the analysis of the relationship between main circuit parameters and compensation capacity could be helpful to the design of FCL-DVR.

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