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IJIEMR Transactions, online available on 3rd Nov 2017. Link :http://www.ijiemr.org/downloads.php?vol=Volume-6&issue=ISSUE-10

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Volume 06, Issue 10, Pages: 27 – 36.

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International Journal for Innovative Engineering and Management Research
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ASYMMETRICAL PWM FULL BRIDGE CONVERTER BY USING CLOSED LOOP CONTROL OF RENEWABLE SOURCES

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ABSTRACT- This paper presented a closed loop control of asymmetrical PWM full bridge converter; Renewable energy and distributed generation are getting more and more popular, wind turbines, and fuel cells. The renewable energy sources need the power electronics interface to the utility grid because of different characteristics between the sources and the grid. No matter what renewable energy source is utilized, extended voltage and power output, less maintenance and higher fault tolerance, the asymmetrical PWM full bridge converter are good, for utility interface of various renewable energy sources. This dissertation proposes a new PWM converter topology and control scheme. Compared to traditional converter, they have enhanced system reliability to no shoot-through problems and lower switching loss with the help of using power closed loop control. The closed loop control, it theoretically eliminates the inherent current zero-crossing distortion of the single-unit asymmetrical type PWM full bridge converter. In addition, the closed loop control can greatly reduce the ripple current or cut down the size of passive components by increasing the equivalent switching frequency. An asymmetrical full bridge PWM technique is proposed for closed loop control of renewable energy sources. The proposed approach is to cut down the switching loss of power control. At the same time, this PWM full bridge leads to current ripple reduction, and thus reducing ripple-related loss in filter components. PWM with feedback controlling is employed for the voltage control of the system. A power management system is designed for the proposed system to manage power flow among different sources.

Key Words: Asymmetrical pulse-width modulated (PWM), full-bridge converter, soft switching, Closed loop control.

I. INTRODUCTION

An asymmetrical full bridge boost DC/DC switching converter is proposed to improve renewable systems. Such a new step-up power converter in a PV system provides a low input current ripple injected into the photovoltaic generator, and at the same time provides a low voltage ripple to the load [1-2]. Low-ripple and high boosting conditions make this converter an ideal candidate for photovoltaic systems design, in particular for grid-connected applications. The converter circuitry is analyzed, and a design procedure is proposed in terms of typical photovoltaic systems requirements [3-5]. Photovoltaic power systems are efficient alternatives to provide electrical energy providing redundancy for critical applications,

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energy generation, and the reduction of traditional energy generation that impacts the environment. Similarly, photovoltaic generators have been intensively used in residential applications and autonomous and portable applications. Photovoltaic systems require a power electronics interface to define their operating point at optimal conditions for any load. For that DC/DC and DC/AC converters are widely used [6-8]. The double-stage approach is widely accepted due to its application in distributed generation system based on multiple generators, as well as in stand-alone DC applications, where a single DC/DC converter is required [9-10].

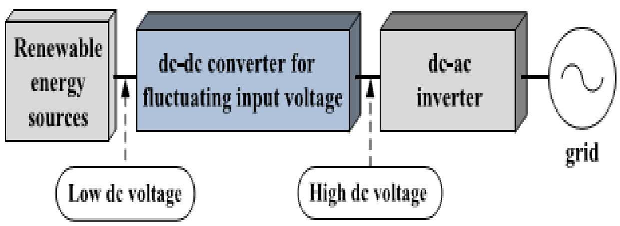

Fig.1. Renewable energy conversion system.

Generally, the renewable energy sources generate low-voltage energy. The photovoltaic cells that depend on environment conditions especially generate fluctuating low-voltage energy. Thus, a frontend converter for fluctuating low-voltage energy is required between the low-voltage source and load requiring high voltage as shown in Fig.1.

II. ANALYSIS OF A PWM FULL-BRIDGE CONVERTER

A. Circuit Configuration and Operation Principle

A circuit configuration of the highly efficient APWM full bridge converter for low input voltage range is shown in Fig.2. The configuration of the proposed converter is basically similar to that of the conventional full-bridge converter except for the dc blocking capacitor and the secondary side of the transformer. The primary side of the transformer consists of the primary winding turns N_p, the four switches, and the dc blocking capacitor C_b. The secondary side has the secondary winding N_s, the output diode D_o, and the output capacitor C_o.

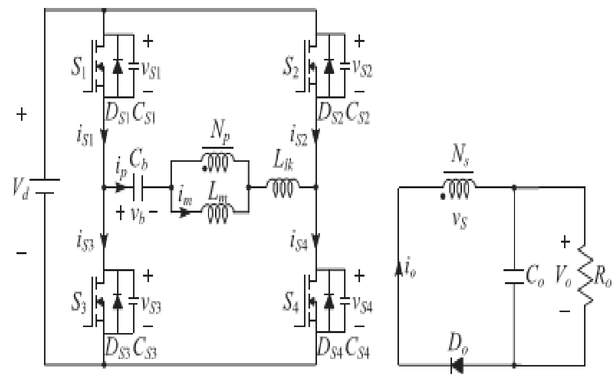

Fig.2. Circuit diagram of the proposed APWM full-bridge converter.

To analyze the steady-state operation of the proposed APWM full-bridge converter, the following assumptions are made.

1) The transformer is modeled as an ideal transformer with the primary winding turns N_p, the secondary winding turns N_s, the magnetizing inductance L_m, and the leakage inductance L_{lk}
2) All switches S_1–S_4 are considered as ideal switches except for their body diodes and output capacitors ($C_{S1}=C_{S2}=C_{S3}=C_{S4}= C_{oss}$).
3) The dc blocking capacitor C_b and the output capacitor C_o are large enough to neglect the voltage ripple on it, so the voltages across C_b and C_o are constant.

While the switch S_1 (S_4) operates with a duty ratio D, depending on the input voltage and load condition, the switch S_2 (S_3) operates with a duty ratio 1−D. In other words, the switches S_1 (S_4) and S_2 (S_3) are operated asymmetrically. Therefore, the circulating current loss of the

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primary side can be eliminated because the proposed converter has no freewheeling period. Fig. 3 represents the operating modes, and Fig.4 represents the theoretical waveforms of the proposed converter under a steady-state condition. The operation of the proposed converter can be divided into six modes during a switching period T_s.

Mode 1 ***[t_0, t_1]:*** At t_0, the switches S_2 and S_3 are turned off. The primary current i_p discharges the output capacitances C_{S1} and C_{S4} of the switches S_1 and S_4 and charges the output capacitances C_{S2} and C_{S3} of switches S_2 and S_3. The interval of this mode is very short and negligible because the output capacitances C_{oss} of the switches are very small. Thus, the primary current i_p and the magnetizing current i_m are regarded as constant value.

Mode 2 ***[t_1, t_2]:*** At t_1, when the voltages v_{S1} and v_{S4} across the switches S_1 and S_4 become zero, the negative current flows through their body diodes D_{S1} and D_{S4}before the switches S_1 and S_4 are turned on. Then, ZVS operation is achieved with the turn-on of the switches S_1 and S_4, and the resonance occurs between the dc blocking capacitor C_b and the primary inductor $L_m + L_{lk}$ of the transformer, but resonance effect does not appear because the resonant period is much longer than one switching period T_s. Thus, by the difference between the voltages of the input and the dc blocking capacitor C_b, the direction of the primary current i_p is changed and kept almost linearly as follows:

$$i_p(t) = i_p(t_1) + \frac{V_d - V_b}{L_m + L_{lk}}(t - t_1) \qquad (1)$$

Where V_d is the input voltage and V_b is the average voltage across the dc blocking capacitor C_b.

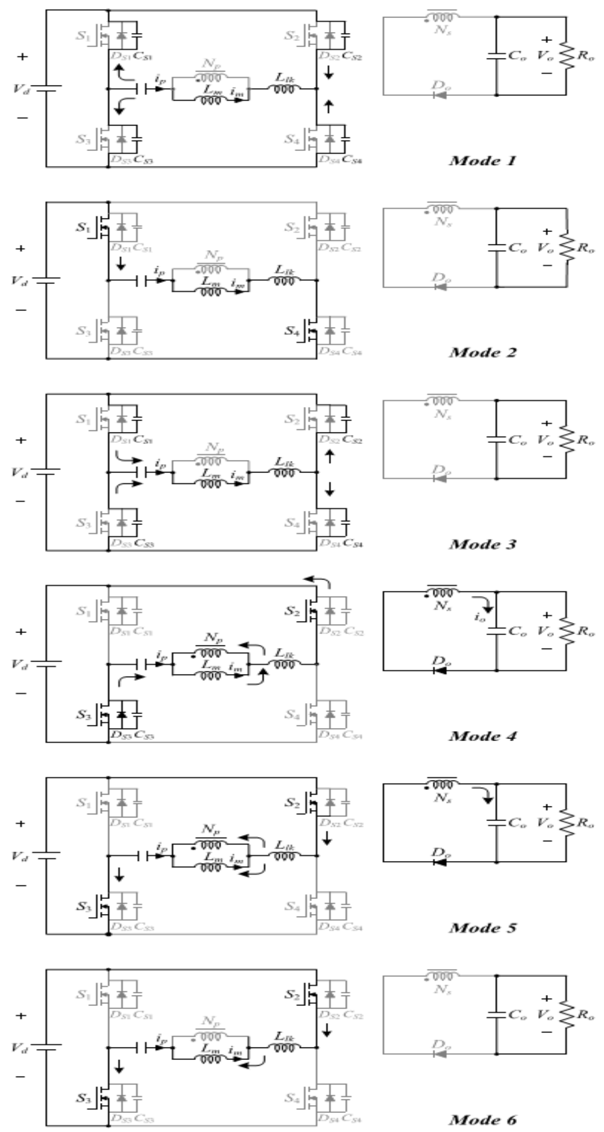

Fig.3. Operating modes of the proposed converter.

Mode 3 [t_2, t_3]: At t_2, the switches $S_1$and S_4 are turned off. The primary current ip charges the output capacitances C_{S1}, C_{S4} of S_1, S_4 and discharges the output capacitances C_{S2}, C_{S3} of S_2, S_4. Similar to Mode 1, the primary current i_p and the magnetizing current i_m are regarded as constant value.

Mode 4 [t_3, t_4]: At t_3, similar to Mode 2, ZVS turn-on of the switches S_2 and S_3 is achieved. The energy stored in the magnetizing inductance

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is delivered to the secondary side of transformer, and the voltage across the magnetizing inductance L_m is clamped by the reflected output voltage as

$$L_m \frac{di_m(t)}{dt} = -\frac{V_o}{n} \quad (2)$$

Where $n=N_s/N_p$. Because the difference between the primary current i_p and the magnetizing current i_m is reflected in the output current i_o, the magnetizing current i_m is decreased as

$$i_m(t) = i_p(t_3) - \frac{V_o}{nL_m}(t - t_3) \quad (3)$$

The resonance occurs between the dc blocking capacitor C_b and the leakage inductance L_{lk} of the transformer. The voltage across the leakage inductance L_{lk} of primary side is the difference between V_d + V_b and the reflected output voltage V_o/n from the secondary side. Thus, the state equations can be written as follows:

$$L_{lk} \frac{di_p(t)}{dt} = -V_d - V_b + \frac{V_o}{n} \quad (4)$$

$$C_b \frac{dv_b(t)}{dt} = i_p(t) \quad (5)$$

Solving (4) and (5), the primary current i_p is

$$i_p(t) = i_p(t_3) \cos \omega_r (t - t_3) + \frac{V_o/n - V_d - V_b}{Z_r} \sin \omega_r (t - t_3) \quad (6)$$

Where the resonant angular frequency ω_r and the impedance Z_r of the resonant circuit are

$$Z_r = \sqrt{\frac{L_{lk}}{C_b}} \quad \omega_r = \frac{1}{\sqrt{L_{lk} C_b}} \quad (7)$$

Mode 5 [t_4, t_5]: At t_4, the primary current i_p becomes zero and changes its direction. Also, the magnetizing current i_m changes its direction during this interval. The output current i_o approaches zero at the end of this mode with resonant characteristics. When the output current i_o becomes zero, this mode ends.

Mode 6 [t_5, t_6]: At t_5, because the resonance launched in Mode 4 is ended, the output current i_o becomes zero. However, the output diode D_o is maintained to on-state until the switches S_2 and S_3 are turned off. During this mode, the primary current i_p is equal to the magnetizing current i_m. Thus, ZCS turn-off of the output diode D_o is achieved.

B. Steady-State Analysis

While the switches S_1 and S_4 operate with a duty ratio D, the difference between the input voltage V_d and the average voltage V_b of the dc blocking capacitor C_b is applied on the inductor of the transformer primary side. While the switches S_2 and S_3 operate with a duty ratio $1-D$, the reflected output voltage V_o/n is applied on the inductor of the transformer primary side and the output diode D_o is turned-on. Since the resonant period of the resonant network is much longer than the dead-time duration, equations of the primary current i_p from (1) and (2) are derived as follows:

$$i_p(t_3) = i_p(t_1) + \frac{V_d - V_b}{L_m + L_{lk}} DT_s \quad (8)$$

$$i_p(t_1) = i_p(t_3) - \frac{V_o}{nL_m}(1 - D)T_s \quad (9)$$

From the resonance of the primary side in Modes 4 and 5, since the leakage inductance L_{lk} is much smaller than the magnetizing inductance L_m, the leakage inductance L_{lk} is negligible. Therefore, the following equation can be obtained:

$$V_d + V_b \simeq \frac{V_o}{n} \quad (10)$$

From (8) to (10), the voltage gain between the input voltage V_d and output voltage V_o is expressed as follows:

$$\frac{V_o}{V_d} \simeq \frac{L_m}{L_m + L_{lk}} 2nD \simeq 2nD \quad (11)$$

Because the leakage inductance L_{lk} is negligible, the average voltage V_b of the dc blocking capacitor C_b is expressed from (10) and (11) as shown in

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$$V_b = V_d(2D-1) \quad (12)$$

Due to the charge balance of the dc blocking capacitor C_b, the average value of the primary current I_p is zero in the steady state. Thus, the relation between the average values of the magnetizing current I_m and average output current I_o can be determined as follows:

$$I_m - I_p = I_m - \frac{1}{T_s}\int_0^{T_s} i_p(t)dt = nI_o. \quad (13)$$

From Fig.4, the average magnetizing current I_m can also be obtained by

$$I_m = \frac{i_p(t_1) + i_p(t_3)}{2}. \quad (14)$$

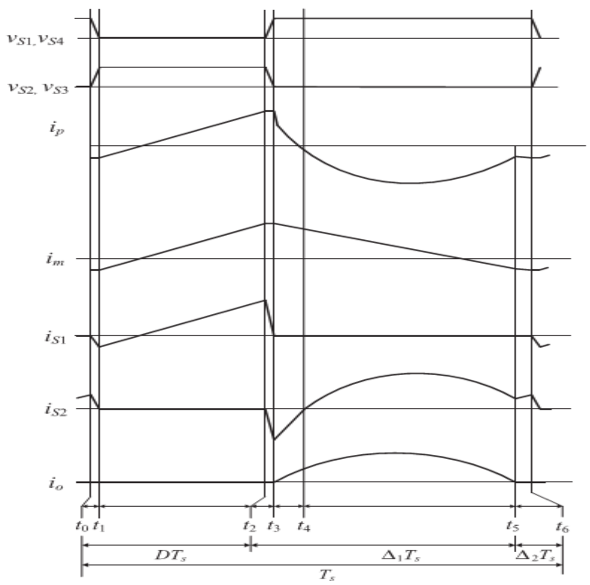


Fig.4. Theoretical waveforms of the proposed converter.

From (1), (13), and (14), the currents i_p (t_1) and ip (t_3) are given by

$$i_p(t_1) = nI_o - \frac{(1-D)T_s}{nL_m}V_o \quad (15)$$

$$i_p(t_3) = nI_o + \frac{(1-D)T_s}{nL_m}V_o \quad (16)$$

Using (13)–(16), the resonant current (6) can be represented by

$$i_p(t) = \left(nI_o + \frac{(1-D)T_s}{nL_m}V_o\right)\cos\omega_r(t-t_3) - \frac{V_o}{nL_m\omega_r}\sin\omega_r(t-t_3). \quad (17)$$

III. SOFT-SWITCHING CONDITIONS

A. ZVS Condition of the Power Switches

For ZVS turn-on of S_1 and S_4, the primary current i_p (t_1) should be negative before S_1 and S_4 are turned on. Thus, from (15), ZVS condition can be expressed as follows:

$$nI_o - \frac{(1-D)T_s}{nL_m}V_o < 0. \quad (18)$$

Equation (18) is arranged by the min–max theorem as

$$\frac{n^2L_mI_{o,\max}}{V_o} = \frac{n^2L_m}{R_{o,\min}} < (1-D_{\max})T_s \quad (19)$$

Where $I_{o,max}$ is the maximum output current, $R_{o,min} = V_o/I_{o,max}$ is the minimum output resistance, and D_{max} is the maximum duty ratio of the switches S_1 and S_4under the minimum input voltage $V_{d,min}$. From (3.11), D_{max} can be described as

$$D_{\max} \simeq \frac{V_o}{2nV_{d,\min}}. \quad (20)$$

According to the variations of the input voltage V_d and turn ratio, the duty ratio of the switches S_1 and S_4. Thus, from (19) and (20), the magnetizing inductance L_m should be designed to satisfy ZVS condition as follows:

$$L_m < \left(1 - \frac{V_o}{2nV_{d,\min}}\right)T_s \cdot \frac{R_{o,\min}}{n^2} \quad (21)$$

Where T_s is a switching period. According to the variation of the duty ratio D, the critical magnetizing inductance value L_m to satisfy the ZVS turn-on condition of the switches The ZVS turn-on condition of the switches S_2 and S_3 can be expressed with the same manner of ZVS condition of the switches $S_1$and S_4. Thus, ZVS operation of S_2 and S_3 can be achieved when the primary current i_p (t_3) is positive. From (16), ZVS condition of S_2 and S_3 is expressed as follows:

$$nI_o + \frac{(1-D)T_s}{nL_m}V_o > 0. \quad (22)$$

The left side terms of (22) are always positive regardless of load variations. Therefore, ZVS operation of the switches S_2 and S_3 can always is satisfied.Another ZVS turn-on operation requires a sufficient dead time between two switch pairs to absolutely discharge the voltage across the output capacitance C_{oss} of the switches. Because i_p (t_1) = i_m (t_1) is regarded as constant value during the dead time, the minimum dead time Δt_{dead} can be calculated as

$$\min\{|i_p(t_1)|, |i_p(t_3)|\} \geq 4C_{oss}\frac{dV_d}{dt} \quad (23)$$

From (15) and (16), the primary current i_p (t_3) is always larger than the absolute value of the primary current i_p (t_1). Therefore, (23) can be simplified as

$$\Delta t_{dead} \geq \frac{C_{oss}V_d}{|i_p(t_1)|/4}. \quad (24)$$

The primary current i_p (t_1) should be negative for ZVS operation. Thus, (3.24) can be expressed as shown in

$$\Delta t_{dead} \geq \frac{4C_{oss}V_d}{\frac{(1-D)T_s}{nL_m}V_o - nI_o} \quad (25)$$

The minimum dead time Δt_{dead} should be considered in the practical design of the magnetizing inductance because Δt_{dead} is always smaller than $(1-D_{max})$ T_s.

B. ZCS Condition of the Output Diode

To achieve the ZCS turn-off condition of the output diode $_{Do}$, the resonant angular frequency ωr should be larger than the critical angular frequency ω_{rc}. Because the critical condition is ip (Ts) = $i_m(T_s)$ at $\Delta_2 T_s = 0$ and $D = D_{max}$, the critical angular frequency ω_{rc} can be described considering the negligible dead-time duration of the power switches as follows:

$$\left(\frac{n^2L_m}{R_{o,\min}} + t_{S2,\min}\right)\cos\omega_{rc}t_{S2,\min} - \frac{1}{\omega_{rc}}\sin\omega_{rc}t_{S2,\min} - \frac{n^2L_m}{R_{o,\min}} + t_{S2,\min} = 0 \quad (26)$$

Where $t_{S2,min}$ is the minimum turn-on duration of the switches S_2 and S_3. The magnetizing inductance L_m is generally designed for the magnetizing current i_m (t_1) to be a small negative value to minimize the conduction loss of the converter. By this assumption, (26) can be obtained as follows:

$$\tan\omega_{rc}t_{S2,\min} \simeq \omega_{rc}\frac{n^2L_m}{R_{o,\min}} + \omega_{rc}t_{S2,\min}. \quad (27)$$

From (21), (27) is expressed as shown in

$$\tan\omega_{rc}t_{S2,\min} < 2\omega_{rc}t_{S2,\min} \quad (28)$$

Thus, the critical angular frequency ω_{rc} can be calculated using a numerical method as shown in

$$\omega_{rc} \approx \frac{\pi + 1.462}{t_{S2,\min}} = \frac{\pi + 1.462}{(1-D_{\max})T_s} \quad (29)$$

From (29), the dc blocking capacitance C_b must satisfy the following relation:

$$C_b \leq \frac{1}{\omega^2{}_{rc}L_{lk}} \quad (30)$$

According to the variation of the duty ratio D, the critical resonant capacitance C_b to satisfy the ZCS turn-off condition of the output diode D_o.

IV. CLOSED LOOP SYSTEM

Sometimes, we may use the output of the control system to adjust the input signal. This is called feedback. Feedback is a special feature of a closed loop control system. A closed loop control system compares the output with the expected result or command status, and then it takes appropriate control actions to adjust the input signal. Therefore, a closed loop system is always equipped with a sensor, which is used to monitor the output and compare it with the expected result. Fig.5 shows a simple closed loop system. The output signal is fed back to the input to produce a new output. A well-designed feedback system can often increase the accuracy of the output.

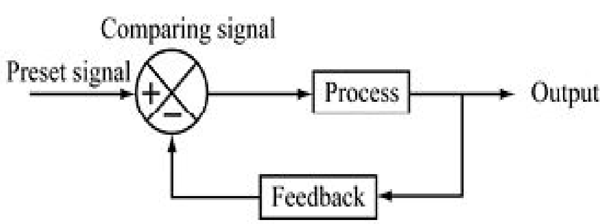


Fig.5 Block diagram of a closed loop control system

Feedback can be divided into positive feedback and negative feedback. Positive feedback causes the new output to deviate from the present command status. For example, an amplifier is put next to a microphone, so the input volume will keep increasing, resulting in a very high output volume. Negative feedback directs the new output towards the present command status, so as to allow more sophisticated control. For example, a driver has to steer continuously to keep his car on the right track. Most modern appliances and machinery are equipped with closed loop control systems. Examples include air conditioners, refrigerators, automatic rice cookers, automatic ticketing machines, etc.One advantage of using the closed loop control system is that it is able to adjust its output automatically by feeding the output signal back to the input. When the load changes, the error signals generated by the system will adjust the output. However, closed loop control systems are generally more complicated and thus more expensive to make.

V.MATLAB/SIMULATION RESULTS

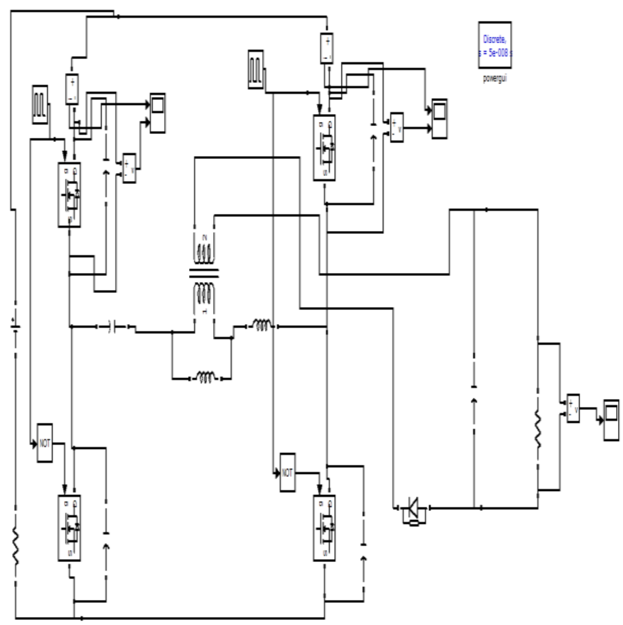
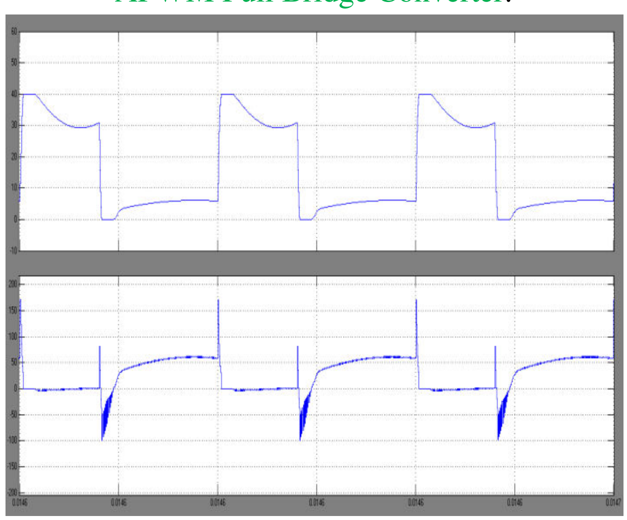


Fig.6. Matlab/Simulation model of proposed APWM Full Bridge Converter.



(a)

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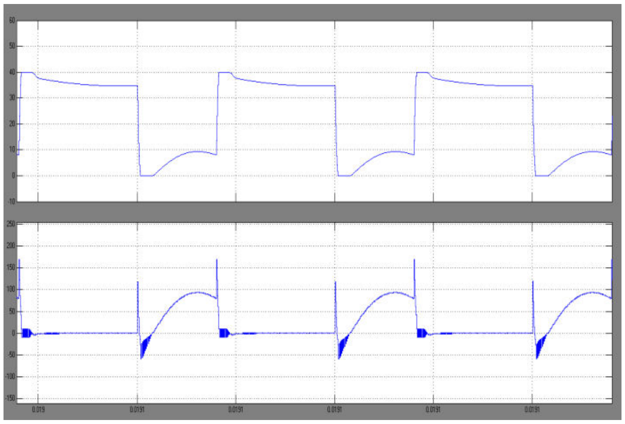


(b)

Fig.7. Simulation waveforms for ZVS turn-on of the switches S_1 and S_2 at V_d = 40 V and Po = 400 W. (a) v_{S1} and i_{S1}. (b) v_{S2} and i_{S2}.

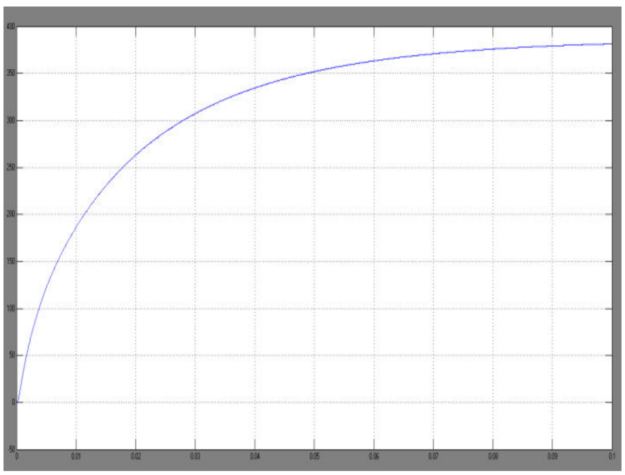
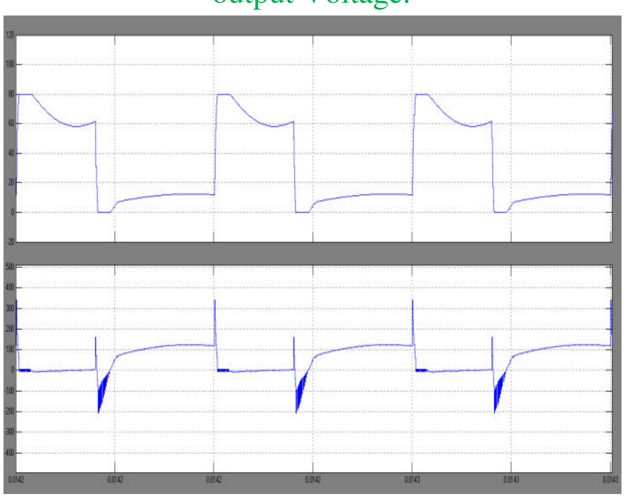
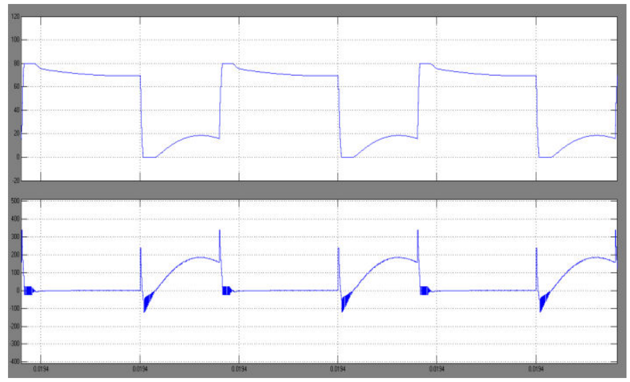


Fig.8. Simulation results for proposed converter output Voltage.



(a)



(b)

Fig.9. Simulation waveforms for ZVS turn-on of the switches S_1 and S_2 at V_d = 80 V and Po = 400 W. (a) v_{S1} and iS1. (b) v_{S2} and i_{S2}.

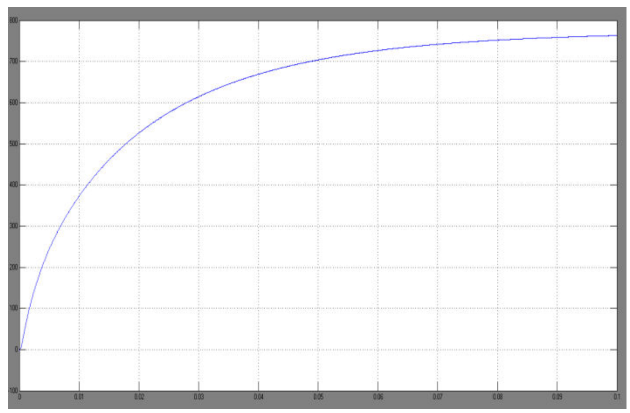


Fig.10. Simulation results for proposed converter output Voltage.

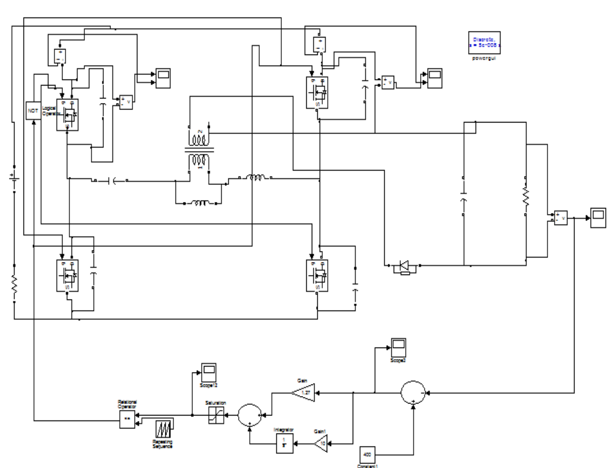


Fig.11. Matlab/Simulation model of closed loop Control of proposed APWM Full Bridge Converter.

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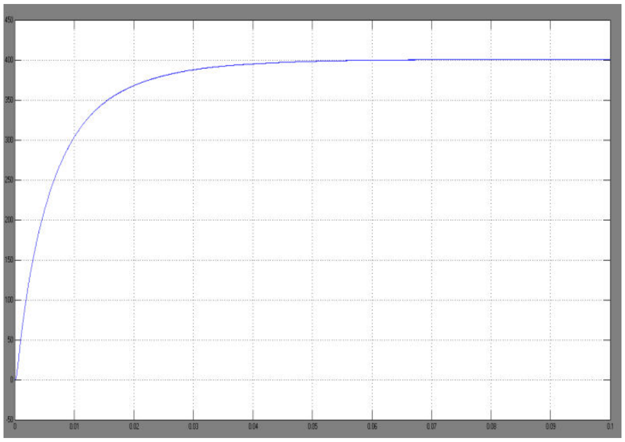

Fig.12. Simulation results for proposed converter output Voltage.

VI. CONCLUSION

Renewable system using asymmetrical boost converter with PWM controlling is designed and analyzed. The converter was developed by breaking the symmetry of traditional boost converters. The Boost converter with Coupled Inductors is used here and for a given small input dc voltage, a high gain. Different high boost ratio dc-dc converter circuit were presented to show how to design low-cost and high-efficiency converters for renewable energy such as solar panel integration applications, fuel cell, uninterruptable power supplies and designed procedure has been developed and verified by simulation. All power switches operate under ZVS and output diode operates under ZCS without extra components. Also, all power switches are clamped to the input voltage. Thus, the proposed converter has the structure to minimize power losses. These advantages make the proposed converter suitable for fluctuating input voltage on renewable energy conversion systems. Compared to traditional converter, they have enhanced system reliability to no shoot-through problems and lower switching loss with the help of using power closed loop control. The closed loop control, it theoretically eliminates the inherent current zero-crossing distortion of the single-unit asymmetrical type PWM full bridge converter. In addition, the closed loop control can greatly reduce the ripple current or cut down the size of passive components by increasing the equivalent switching frequency.

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