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Title: **A CAPACITOR VOLTAGE-BALANCING METHOD FOR NESTED NEUTRAL POINT CLAMPED (NNPC) INVERTER**

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A CAPACITOR VOLTAGE-BALANCING METHOD FOR NESTED NEUTRAL POINT CLAMPED (NNPC) INVERTER

ABSTRACT

A capacitor voltage-balancing technique for a settled nonpartisan point cinched (NNPC) inverter is proposed in this paper. To control and adjust flying capacitor voltages the proposed capacitor voltage adjusting technique exploits excess in stage exchanging states. The proposed strategy needs not very many calculations and furthermore simple to actualize. The NNPC inverter is a recently created four-level voltage source inverter for medium-voltage applications. The NNPC topology has two flying capacitors in every leg. With a specific end goal to guarantee that the inverter can work ordinarily and all exchanging gadgets share indistinguishable voltage stretch, the voltage over every capacitor ought to be controlled and kept up at 33% of dc transport voltage. The proposed strategy is anything but difficult to coordinate with various heartbeat width adjustment plans. By utilizing the recreation comes about we can break down the viability and feasibility of the proposed method.

Index Terms—Capacitor voltage-balancing method, multilevel inverter, nested neutral point clamped (NNPC) inverter, voltage source inverter

INTRODUCTION

Nowadays, Multilevel inverters are extremely prominent in medium voltage applications and engine drives because of diminishment of sounds, low voltage weight on switches, low exchanging recurrence, and less exchanging misfortunes [1]. The multilevel inverters arranged into nonpartisan point clasped (NPC) inverter, flying capacitor (FC) inverter, fell Hbridge inverter, and measured multilevel converter [2]– [3]. A few control systems and regulation procedures including capacitor voltage-adjusting techniques have been produced in the writing for multilevel inverters [4]. In this paper another multilevel topology is proposed.i.e, nested neutral point clamped (NNPC) inverter shown in Fig. 1.
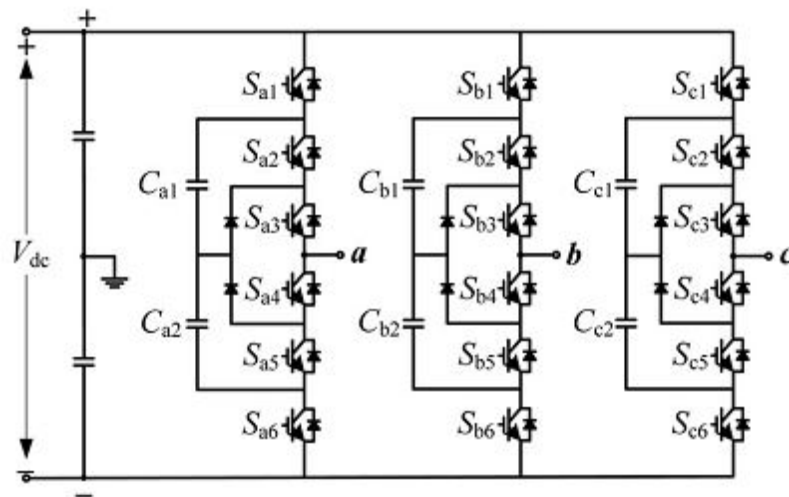

Fig 1. Three phase nested neutral-point clamped (NNPC) inverter.

This topology is a blend of a FC topology with a NPC topology, which gives four levels in yield voltage. In examination with the fourlevel NPC inverter, the NNPC inverter has less number of diodes, and in contrast with four-level FC inverter, it has less capacitors [6]. All switches in the topology have a similar voltage stretch equivalent to 33% of dc-connect voltage. The NNPC inverter can work in an extensive variety of 2.4– 7.2 kV without the requirement for associating power gadgets in arrangement. As can be seen from Fig. 1, the NNPC topology has two FCs in every leg. The voltage over every capacitor ought to be controlled and adjusted at 33% of dc-interface voltage (Vdc/3) to guarantee that the inverter can work ordinarily [6]. To alleviate the previously mentioned downsides, another capacitor voltage-adjusting technique for the NNPC inverter is proposed in this paper. In the proposed technique, straightforward rationale tables are created to control the voltages of FCs. The proposed technique has the accompanying highlights:

1) The strategy is appropriate for and can be effectively incorporated with various heartbeat width adjustment (PWM) plans, for example, SPWM and SVM, and so forth;

2) The technique utilizes basic rationale tables, needs not very many calculations, and is anything but difficult to actualize.

The distinction in the topology causes diverse conduct in capacitor voltages and along these lines require diverse voltage-adjusting strategies. With a specific end goal to control yield voltage and get FC voltage adjust, a space vector balance (SVM) method is introduced in [6] for NNPC inverter. In this strategy, a cost work is characterized in view of the vitality put away in capacitors. The cost work should be ascertained over and again for each excess exchanging state in each examining period to locate the best changing state to adjust FC voltages.

OPERATION OF THE NNPC INVERTER AND BEHAVIOR ANALYSIS OF THE CAPACITOR VOLTAGES

A. Operation of the NNPC Inverter

The three-phase NNPC inverter is appeared in Fig. 1. Each period of the inverter comprises of six switches, two clipping diodes, and two FCs. The voltages of the FCs ought to be kept at 33% of dcphase voltage and guarantee that all the power switches share a similar voltage push. Table I demonstrates the stage voltagev_k (k=a, b, c), yield levelL_k, and also the relating stage exchanging stateS_k. For each stage, the four particular yield voltages are −Vdc/2, −Vdc/6, Vdc/6, and Vdc/2, comparing to the four yield levels 0, 1, 2, and 3, separately. The relationship of vk and Lk can be expressed as

B. Behavior Analysis of the Capacitor Voltages in the NNPC Inverter

Different redundant switching states have different impacts on FC voltages. The analysis of this impact is illustrated in Fig. 2, in which the six overall switching states are analyzed. In Fig. 2, Ck1 andCk2 are the two series FCs in the phase k(k=a, b, c), whose voltages are denoted byV_{Ck1} andV_{Ck2}. The behavior of the capacitor voltages depends on the switching state Sk and the phase current ik. (a) Switching state 0.
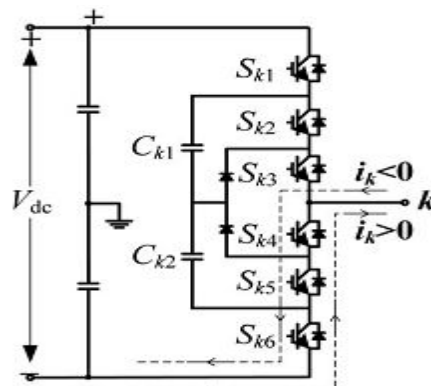

Fig. 2. Impacts of different phase switching states

and phase current on capacitor voltages in NNPC inverter As shown in Fig. 2(a) and (f), the switching states 0 and 3 (corresponding to levels 0 and 3, respectively) have no impact on the capacitorAs can be seen from Table I, levels 0 and 3 have no redundant switching state, while levels 1 and 2 both have two redundant switching states. The redundant switching states for level 1 are 1A [001101]

SIMULATION RESULTS

To verify the proposed capacitor voltage balancing method, simulation studies have been done by using MATLAB/ Simulink(3), in which Vref is the given peak phase voltage reference, and Vdc is dc bus voltage   = √3   /   (3) Two PWM schemes, SPWM and SVM, integrated with the proposed capacitor voltage balancing method, have been studied in both steady state and transient state the simulation results of NNPC inverter when SVM and the proposed voltage balancing method are applied, with ma=0.8whent<0.1s, and ma =0.5whent>0.1s. respectively.

CONCLUSION

In this paper, proposes a capacitor voltage adjusting technique for a four-level NNPC inverter. At diverse PWM plans the proposed technique is anything but difficult to coordinated. The proposed technique exploits repetition in stage changing states to control and adjust the FC voltages. For the control of capacitor adjusting basic and viable rationale tables are produced. The technique is anything but difficult to actualize and needs not very many calculations. The restriction of the NNPC inverter as far as the voltage adjusting and capacitor estimate is additionally explored. The viability and possibility of the proposed strategy is resolved by using the simulation results and also analyze the proposed method.

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