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Title: **High Step-Down Isolated Three-Phase AC–DC Converter fed Induction Motor Drive**

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High Step-Down Isolated Three-Phase AC–DC Converter fed Induction Motor Drive

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Abstract- A single-phase, three-level, single-stage power-factor corrected AC/DC converter operated under Induction motor Drive is presented. That operates with a single controller to regulate the output voltage and the input inductor act as a boost inductor to have a single stage power factor correction with good output response. The paper deals a single-stage three-phase isolated ac-dc converter topology utilizing SiC MOSFETs is proposed for power rectification with a stepped-down output voltage. Unlike the conventional two-stage [front-end power factor correction (PFC) stage and isolated dc–dc stage] ac–dc converters, the full/half bridge structure in dc–dc stage is eliminated in this structure. The high-frequency pulsating voltage is obtained directly from the PFC stage and is applied across the high frequency transformer, leading to a more compact design.
In addition, there is an advantage of zero voltage switching (ZVS) in four PFC MOSFETs connected to the high-frequency tank, which is not achievable in the case of a conventional two-staged ac–dc converter. A sine-pulse width modulation (PWM)-based control scheme is applied with the common-mode duty ratio injection method to minimize the current harmonics without affecting the power factor. An LC filter is used after the PFC semi stage to suppress the line-frequency voltage ripple. Furthermore, the intermediate dc-link capacitor value can be greatly reduced through no additional ripple constraints. The proposed converter is having an input power factor close to unity and better voltage regulation compared to the conventional ac-dc converter topologies and able to provide variable output voltages. Proposed topology is evaluated through Matlab/Simulink platform and simulation results are conferred.

Keywords: Power Factor Correction, Single Stage Converters, AC–DC Power Factor Correction, Three Level Converters.

(1) .INTRODUCTION

Power-electronic converters are becoming popular for various industrial drives applications. In recent years also high-power and medium-voltage drive applications have been installed. To overcome the limited semiconductor voltage and current ratings, some kind of series and/or parallel connection will be necessary. Due to their ability to synthesize waveforms with a better harmonic spectrum and attain higher voltages, multi-level inverters are receiving increasing attention in the past few years. The ac–dc power supplies with transformer isolation are typically implemented with some sort of input power factor correction (PFC) to comply with harmonic standards such as IEC 1000-3-2 [2]-[4]. Although it is possible to satisfy these standards by adding passive filter elements to the traditional passive diode rectifier/LC filter input combination, the resulting converter would be very bulky and heavy due to the size of the low-frequency inductors and capacitors. The most common approach to PFC is to use two-stage power conversion schemes.These two-stage schemes use a front-end ac–dc converter stage to perform ac–dc conversion with PFC with the output of the front-end converter fed to a back-end dc–dc converter stage that produces the desired isolated dc output voltage

[5]. Using two converter stages in this manner, however, increases the cost, size, and complexity of the overall ac–dc converter, and this has led to the emergence of single-stage power-factor-corrected converters.

In order to reduce the cost, size, and complexity associated with two-stage ac–dc power conversion and PFC, researchers have tried to propose single-stage converters that integrate the functions of PFC and isolated dc–dc conversion in a single power converter. Several single-phase [6]–[12] and three-phase [5] converters have been proposed in the literature, with three-phase converters being preferred over single-phase converters

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for higher power applications.Previously proposed three-phase single-stage ac–dc converters, however, have at least one of the following drawbacks that have limited their widespread use.

1) They are implemented with three separate ac–dc single stage modules

2) The converter components are exposed to very high dc bus voltages so that switches and bulk capacitors with very high voltage ratings are required.

3) The input currents are distorted and contain a significant amount of low-frequency harmonics because the converter has difficulty performing PFC and dc–dc conversion simultaneously.

4) The converter must be controlled using very sophisticated techniques and/or nonstandard techniques [6]–[12]. This is particularly true for resonant-type converters that need variable-switching-frequency control methods to operate.

5) The output inductance must be very low, which makes the output current to be discontinuous. This results in a very high output ripple so that secondary diodes with high peak current ratings and large output capacitors to filter the ripple are needed.

6) Most of them are in discontinuous conduction mode at the input and need to have a large input filter to filter out large high-frequency harmonics [5].

The most common topologies for dc–dc stage are phase-shifted full-bridge type [8]–[11] and resonant type (LLC or CLLC) [12] converters. Fig. 1 presents one possible solution, where the first stage is implemented by an active six-switch boost PFC converter [7] and the second stage is implemented by a phase-shifted full-bridge converter [8]–[11]. These two stages are connected by the intermediate dc link and each stage is controlled separately.

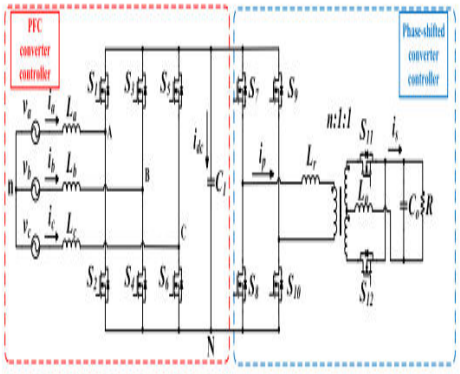

Fig. 1. Circuit topology of a conventional two-stage ac–dc converter

As can be seen from Fig. 1, the conventional two-stage ac–dc converter contains twelve active switches. Every switch is affiliated with a gate driver circuit and a heat sink, which all contribute to higher weight, size, and cost. In addition, the intermediate dc-link capacitor is usually very large in order to limit the voltage ripple, which is another nonnegligible portion of size and cost [13]. To overcome these challenges, recent literature has reported efforts to develop ac–dc power supplies with simpler, cheaper, and more compact methods. These can be usually divided into three categories.

1.1 Parallel Single-Phase Converter

One possible approach is to use three independent single phase boost PFC converters in parallel, with each module connected to two of the three-phase voltages [14], [15]. The three output dc voltages are then combined in parallel to generate a uniform dc-link voltage. This approach is attractive due to the simplicity of control of single-phase converters and less number of switches; however, the main drawback lies in the complexity to achieve synchronization and equal power distribution.

1.2 Reduced-Switch PFC Converter

The front-end PFC stage can be implemented by different topologies to reduce the number of active devices. Four-switch, three-switch, and even single-switch converters have been proposed, which are originated from the boost topology. In four-switch topology, the two switches in one phase leg are replaced by two capacitors [16], [17]. In three-switch converter, also referred as “Vienna rectifier,” each phase leg has bidirectional current flow by a combination of a single

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switch and the multiple diodes [18]. The main drawback of these two topologies is the complicated controller design.

The increased number of diodes in "Vienna rectifier" could also result in more conduction loss. In single-switch topology, three-phase single-switch ac–dc boost converter is widely used for its simple control and no need for input current sensors [3]. But the phase currents could contain low-frequency harmonic distortion.

1.3 Single-Stage AC–DC Converter

Although the former techniques can lower the component counts and complexity in a front-end PFC converter, a second stage dc–dc converter still is an unavoidable requirement. This is another motivation to combine the two stages into one single stage and to be regulated by a single controller to satisfy both the power factor and voltage regulation requirements [19]–[27]. Besides, isolation is achieved by the high-frequency transformer in dc–dc semistage. Single-stage topology has advantages in terms of lower cost, smaller size, simpler structure and higher reliability. One possible solution is combining a PFC buck-boost converter and a dc–dc forward converter [19]. The dc-link voltage can be kept low and its sixth line frequency harmonic ripple can be reduced, which leads to a smaller dc-link capacitance. But there are many passive inductors and diodes used in the topology. In order to achieve higher efficiency, zero voltage switching (ZVS) technique is employed in [20] and [21], where the circuit is a combination of a boost PFC converter and a full-bridge dc–dc converter. One common disadvantage of the above topologies is that they all operate in discontinuous current conduction mode (DCM), leading to a higher peak and RMS phase current, and thus experiences a higher conduction loss in switches. In addition, due to the high-frequency variation of currents, the inductor core loss would be higher and the electromagnetic interface could be worse.

In order to alleviate the aforementioned constraints and limitations, a novel single-stage three-phase isolated ac–dc converter is proposed in this paper. This topology consists of a PFC semi stage followed by a dc–dc semi stage, isolated through a high-frequency transformer in a center-tapped configuration. One of the major contributions is that it operates in continuous current conduction mode (CCM), so there is no need for additional input filter, and the stress on the semiconductor devices can be reduced. The other contribution is that the combination of two stages reduces the number of switches to eight from twelve, where six of them (four in PFC and two in dc–dc semi stage) can achieve ZVS during operation. This makes the converter topology more efficient and compact. Furthermore, the two switches in the dc–dc semi stage can achieve ZCS during the turn-OFF interval.

Another significant contribution is achieving a lower total harmonic distortion (THD) by injection of a common mode duty ratio term to each current compensator's output. In addition, the controller is easy to implement based on sine-pulse width modulation (PWM) technique. The dc-link capacitor value can also be greatly reduced without affecting the PFC operation, since there is no additional ripple constraint imposed on it, which reduces a portion of weight in the system.

2 Principle of Operation

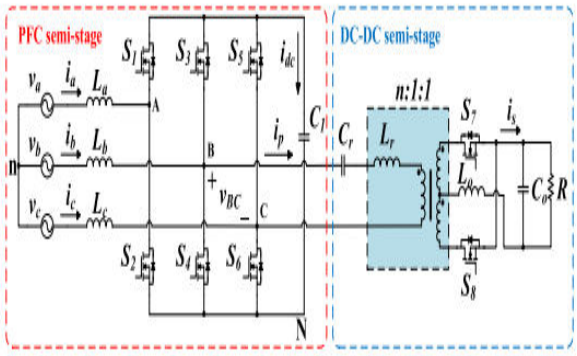

Fig. 2. Proposed single-stage ac–dc converter topology.

In this section, the operating principle of the proposed three-phase single-stage ac–dc converter, shown in Fig. 2, is presented. To clarify the structure, the left-hand side part is called PFC semistage and the right-hand side part is called dc–dc semistage. This topology comes from combining the ac–dc and dc–dc stages in a conventional two-stage converter (Fig. 1). Four switches from the full-bridge topology in the former dc–dc stage are eliminated. The input port of the dc–dc semistage is directly connected to B and C (or any other two phase-leg midpoints) points. As can be seen from Fig. 2, the intermediate capacitor is no longer directly connected to the dc–dc semistage. In the PFC semistage, there are three inductors in series with the ac source to boost the input ac voltage and filter the input current as well. The high side and low-side switches are driven complementarily with a dead band. The voltage across the phase-leg midpoints (vBC) consists of both the line frequency and switching frequency components. Cr and Lr serve as the second-order LC filter to offer attenuation as high as 40 dB to the line-frequency component and to pass the switching frequency component to

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the transformer, which helps in keeping the size of the transformer smaller. The inductor Lr is implemented by the leakage inductance of an n:1:1center-tapped transformer, which forms isolation and steps down the voltage. The output capacitor Co and inductor Lo form a low-pass filter to reduce the current and voltage ripple. Since the secondary and tertiary leakage inductors are much smaller than Lo and the magnetizing inductance is built large to only allow a very small current to flow, hence they are not drawn in the figure. This converter is regulated by a centralizedcontroller. The secondary side of the converter consists of a rectifier bridge, which typically contains two diodes but in order to reduce the conduction loss, these are replaced by synchronous rectification (SR) MOSFETs.

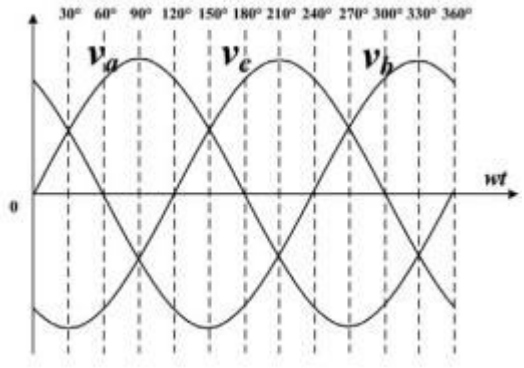

Fig. 3. Three-phase line to neutral (L to N) voltage.

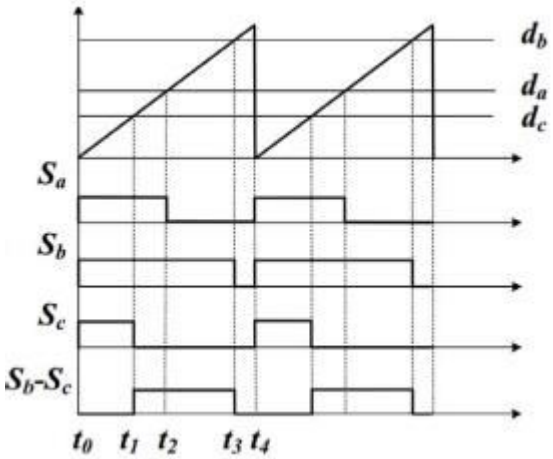

Fig. 4. Timing diagram.

The three input phase voltages in a balanced ac system have 120° phase difference, which can be divided into 12 intervals as shown in Fig. 3. ω denotes the angular line frequency. Without loss of generality, the following operating principle is analyzed in 0° <ωt< 30°, which leads to vb>va>vc.

In the proposed circuit, sine-PWM-based control scheme is applied in the PFC semistage. The PWM signal to each switch is generated by comparing each phase modulation wave with a common saw-tooth waveform. The modulation wave is generated by the PI controller, which takes the input of phase current error. The proportional coefficient (k p) amplifies the difference without phase change and the integral coefficient (ki) improves the controller dynamics, reflected by the ripple on the modulation wave. Thus, modulation wave remains in phase with the phase voltage. Therefore, within the range where vb>va>vc, the duty ratio also has similar relationship as db> da > dc, which is shown in Fig. 4. Due to their relative positions, there are four possible switching statesfrom t0 to t4. Since the switching frequency is much higher than the line frequency, the following assumptions can be made in one switching cycle: 1) constant input line voltage and 2) constant modulation wave. It should be noted that the intermediate dc-link voltage is not directly controlled, thus it would have some variation. But such variation is small in a switching cycle, so it can also be considered a denoted by Vdc.Suppose Sk represents the switching state (“0” if OFF, “1” if ON) of the high-side MOSFET in “k” phase (“k” represents “a” or “b” or “c”). According to the timing diagram in Fig. 4, there are overall four operation modes. They are expressed in (SA SB SC) format as followed: (111), (110), (010), and (000). Due to the power factor requirement, the phase currents should always have such relationship: ib>ia> 0 >ic. Based on active six-switch boost converter operation principle, input current slopes in PFC semistage can be calculated as follows:

$$\frac{di_a}{dt} = \frac{1}{L}\left(v_{an} - \frac{2}{3}v_{AN} + \frac{1}{3}v_{BN} + \frac{1}{3}v_{CN}\right) \quad (1)$$

$$\frac{di_b}{dt} = \frac{1}{L}\left(v_{bn} - \frac{2}{3}v_{BN} + \frac{1}{3}v_{AN} + \frac{1}{3}v_{CN}\right) \quad (2)$$

$$\frac{di_c}{dt} = \frac{1}{L}\left(v_{cn} - \frac{2}{3}v_{CN} + \frac{1}{3}v_{AN} + \frac{1}{3}v_{BN}\right) \quad (3)$$

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vkN can be expressed in terms of the switching states Sk according to (4)

$$v_{kN} = S_k V_{\mathrm{dc}}. \tag{4}$$

Considering the dc–dc semistage, the input voltage of this stage is formulated as follows:

$$V_{\mathrm{BC}} = (S_B - S_C) V_{\mathrm{dc}} \tag{5}$$

where (SB − SC) could either be 1 or 0, so the input voltage vBC is a square wave signal (either Vdc or 0) with the duty ratio of (dB − dC) at the switching frequency. Because of the large output inductor, the secondary side current is could be considered constant, denoted by IS. In addition, only one of S7 or S8 can be turned on at steady state and therefore, the primary side current i p would be pulsing from Is/n to −Is/n. The transition time is small due to a small leakage inductor Lr . One important fact about this converter is that the energy should always flow to the load under the required power factor. Under such constraint, i p should be positivewhen vBC> 0 to transfer the energy. Similarly, i p should be negative when vBC = 0. Furthermore, Is/n can be assumed to be much larger than phase currents under high power condition. For a comprehensive understanding, the operations under different modes are described in detail and shown in Fig. 5. In order to clarify the modes of operation, the circuit is divided into two semistages in Fig. 5.

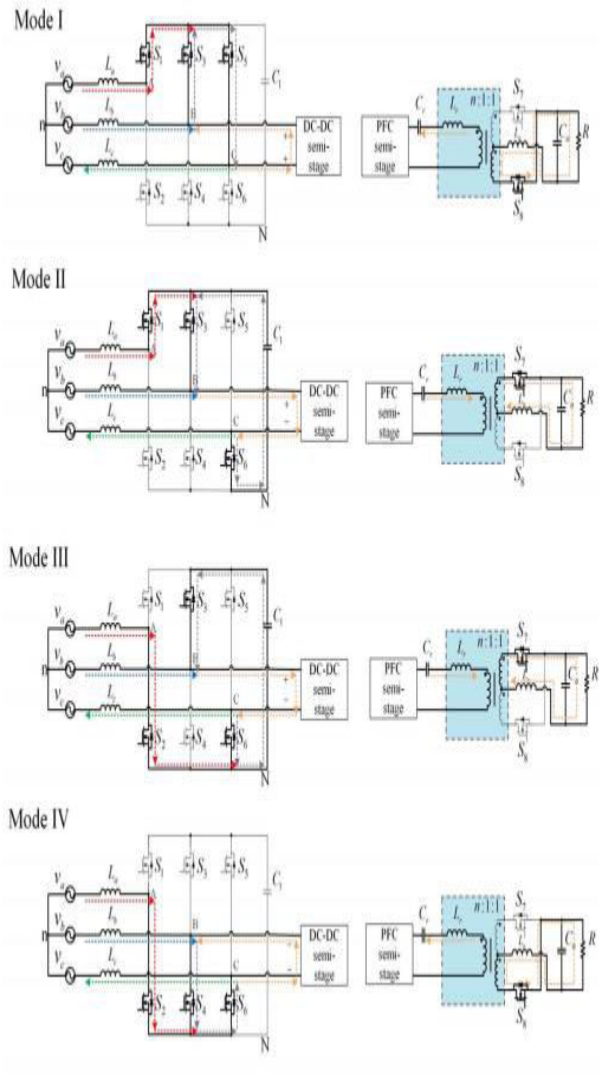

Fig. 5. Operation modes of the proposed converter.

1) Mode 0 (Initial Mode): S1, S3, and S5 are OFF. S2, S4, and S6 are ON. As can be seen from the converter structure during this mode, there will be circulating current through three boost inductors and the input phases and no power would be transferred to the output in this interval.

2) Mode I: During the interval [t0, t1], S1, S3, and S5 are ON and S2, S4, and S6 are OFF. ia and ib increase, and ic decreases linearly. There is no current flowing through the intermediate capacitor C1, when vBC is zero. According to the former analysis, i p = −Is/n. Thus, S8 turns on. Zero power is transferred to the dc–dc semistage.

3) Between Mode I and Mode II: S5 is turned OFF. i p and ic should remain the same because of the inductors holding the currents in the switching cycle interval. So C1 would charge

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the output capacitor of S5 to Vdc and discharge the output capacitor of S6 to zero, leading to a potential ZVS turn-ON of S6. After the output capacitor of S6 becomes zero, the anti-parallel diode turns ON and starts conducting. After the completion of deadtime interval, S6 starts conducting. Therefore, the deadtime value should be kept more than the time taken to fully discharge the output capacitor.

4) Mode II: During the interval [t1, t2], S6 is turned ON. ib increases, and ia and ic decrease linearly. The voltage across B and C is vBC = Vdc. In such case, i p > 0 and the PFC semistage transfers power to the dc–dc semistage. S7 is turned ON. At high power, i p is larger than the phase input current, so the currents through S3 and S6 are both flowing downward and C1 gets discharged.

5) Between Mode II and Mode III: S1 is turned OFF. The current is freewheeling through the body diode of S1.

6) Mode III: During the interval [t2, t3], S2 is turned ON. ia and ic increase, and ib decreases linearly. vBC remains constant, so the current operation in dc–dc semistage does not change. C1 still gets discharged.

7) Between Mode III and Mode IV: S3 is turned OFF. ip and ib remain the same. So C1 would charge the output capacitor of S3 to Vdc and discharge that of S4 to zero, leading to a potential ZVS turn-ON of S4.

8) Mode IV: During the interval [t3, t4], S4 is turned ON. ia and ib increase, and ic decreases linearly. There is no current flowing into C1 when vBC = 0, so i p < 0. S8 turns ON and S7 turns OFF. Zero power is transferred into the dc–dc semistage. After mode IV, the system comes back to mode I and repeats such process periodically.

9) Between Mode IV and Mode I: S2, S4, and S6 are turned OFF. The output capacitors of S2 and S4 would be charged to Vdc and those of S1 and S3 would be discharged to zero, leading to ZVS turn-ON potential in S1 and S3.

To sum up, with proper tuning of deadtime, the four switches (S1, S3, S4, and S6) in the PFC semistage can achieve ZVS turn-ON during any periodic cycle of operation. In addition, the two switches (S7, S8) in the secondary/tertiary sides are controlled in SR mode, so they can achieve both ZVS turn-ON and ZCS turn-OFF.

3 Modelling and Control Scheme

In this section, the primary side LC filter design is discussed in detail. It is followed by the explanation of the control scheme and stress analysis.

3.1 Line-Frequency LC Filter Design

The input voltage of dc–dc semistage (vBC) has a linefrequency component, due to the sine-PWM control method. This would result in a slow variation in the output voltage. Cr and Lr serve as a second-order LC filter to attenuate the low-frequency ripple, and to keep the high switching frequency component, which passes through the transformer. By taking the average value in one switching period, the voltage drop across the output inductor Lo and the current flow through the output capacitor Co are both zero. Therefore, the equivalent input resistance of the secondary/tertiary sides would be R. After it is transferred to the primary side, the equivalent circuit of the dc–dc semistage is then depicted in Fig. 6.

By using the Laplace transform, the voltage transfer function is formulated in (6)

$$\frac{v_o}{v_i} = \frac{n^2 R}{L_r} s \Big/ \left(s^2 + \frac{n^2 R}{L_r} s + \frac{1}{C_r L_r} \right) \quad (6)$$

This topology acts as a bandpass filter, where the maximum gain is located at the resonant frequency ω0 = 1/√(Lr Cr) and the quality factor is Q = (Lr /Cr)1/2/(n2 R). The transfer function in (6) can be changed to (4.7) using w0 and Q.

$$\frac{v_o}{v_i} = \frac{w_0}{Q} s \Big/ \left(s^2 + \frac{w_0}{Q} s + w_0^2 \right). \quad (7)$$

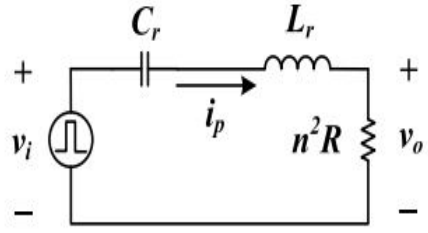

Fig. 6. DC–DC semistage equivalent circuit.

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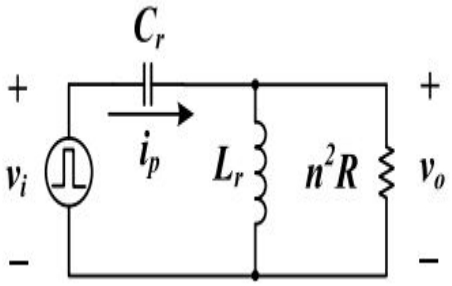

Fig. 7 High-pass LC filter.

It should be noted that the second-order high-pass LC filter (Fig. 7) has a better performance in terms of keeping all the higher order harmonics. However, the parallel filter inductor Lr offers a lower network impedance, thus allowing a higher circulating current in the dc–dc semistage. Since two phaseleg midpoints are connected to the LC tank, the effective RMS currents through the corresponding two pairs of switches become higher. Therefore, there is higher conduction loss in the converter, degrading its overall conversion efficiency, especially at higher power operation.

3.2 Duty Compensation

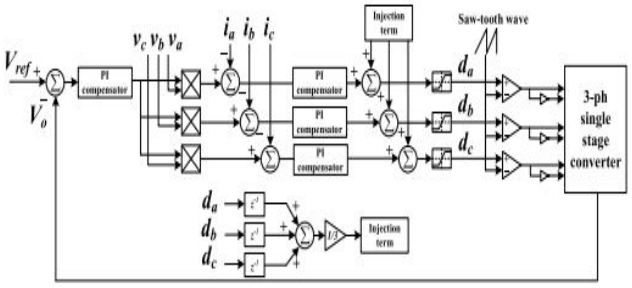

Fig. 8. Control strategy for the proposed three-phase ac–dc converter.

The main control objective is to achieve a >0.99 power factor operation in three-phase currents and to obtain a regulated output dc voltage. The proposed control block diagram is shown in Fig. 8, where the phase duty ratios act as modulation waves.

The control diagram is composed of an outer voltage loop and an inner current loop. The output voltage is compared with a fixed voltage reference and fed to a PI compensator. The product of voltage PI output and each phase voltage is regarded as the corresponding phase current reference, and is further compared with the phase current. The current loop PI compensators are designed to achieve a very high bandwidth (at least ten times larger than the line frequency) to let the phase current track its reference. In this way, the steady state error can be greatly reduced to ∼1% of the reference value.

A common-mode duty ratio injection technique is applied to minimize the input current harmonics, which is caused by the floating potential between the ac source neutral and intermediate dc-link negative node. Based on PFC semistage topology in Fig. 2, (8) can be formulated to express the voltage relation in a single-phase loop

$$v_{kn} + v_{nN} = L\frac{di_k}{dt} + V_{dc}S_k \tag{8}$$

Where "k" denotes the phase symbol ("a," "b," or "c" phase). By taking the average value of one switching cycle, (8) now becomes

$$v_{kn} + \langle v_{nN}\rangle_0 = L\frac{di_k}{dt} + V_{dc}d_k \tag{9}$$

where vnN0 denotes the average value of vnN . The highfrequency ripple in the phase current ik is filtered and only contains the line-frequency component. The average of Sk represents the duty ratio dk, which represents the high-side duty ratio of phase "k." For a balanced three-phase voltage source, the subsequent relation is always valid

$$v_{an} + v_{bn} + v_{cn} = 0. \tag{10}$$

By applying summation of (9) for all three-phases, one can get

$$3\langle v_{nN}\rangle_0 = L\frac{d}{dt}\left(\sum_{k=a}^{c} i_k\right) + V_{dc}\left(\sum_{k=a}^{c} d_k\right). \tag{11}$$

The ultimate goal is to achieve zero higher order harmonics in ik, so that sum of all the higher order inductor voltages is zero. However, in conventional feedback only control scheme in sine-PWM technique, the duty ratio signals would have 120° phase difference in line frequency, and thus adds up to zero.

According to (11), this would lead to nonzero result in the sum of three inductor voltages, which in turn represents the unwanted harmonics in the phase currents. Therefore, in order to minimize these harmonics, the duty ratio signal should contain an additional duty compensation term to satisfy the constraint in (12)

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$$3\langle v_{nN}\rangle_0 = V_{\rm dc}\left(\sum_{k=a}^{c} d_k\right). \tag{12}$$

Based on (9) and (12), each duty ratio signal could be chosen as follows:

$$d_a[n] = \frac{V_i}{V_{\rm dc}}\sin(\omega t) + \frac{1}{3}(d_a[n-1] + d_b[n-1] + d_c[n-1]) \tag{13}$$

$$d_b[n] = \frac{V_i}{V_{\rm dc}}\sin\left(\omega t - \frac{2\pi}{3}\right) + \frac{1}{3}(d_a[n-1] + d_b[n-1] + d_c[n-1]) \tag{14}$$

$$d_c[n] = \frac{V_i}{V_{\rm dc}}\sin\left(\omega t + \frac{2\pi}{3}\right) + \frac{1}{3}(d_a[n-1] + d_b[n-1] + d_c[n-1]). \tag{15}$$

The second term in (13)–(15) represents the common-mode duty ratio injection part added to each modulation waveform after the PI compensators. More details of calculation can be found in [30]. By summing (13)–(15), the three-phase terms are added to be zero, and the summation of the duty ratios has the following relationship:

$$d_a[n] + d_b[n] + d_c[n] = d_a[n-1] + d_b[n-1] + d_c[n-1] = d_{\rm tot}. \tag{16}$$

From (16), the summation (dtot) is the same in different sampling cycles. By applying dtot to (13), the duty ratio of phase "A" can be expressed as

$$d_a[n] = \frac{V_i}{V_{\rm dc}}\sin(\omega t) + \frac{1}{3}d_{\rm tot} \le \frac{V_i}{V_{\rm dc}} + \frac{1}{3}d_{\rm tot}. \tag{17}$$

Since the PFC semistage is a boost type converter, the intermediate voltage is larger than the input phase voltage. Thus Vi/Vdc < 1. A sufficient condition to ensure da[n] < 1 is that dtot< 3(1 − Vi/Vdc) holds at steady state, which can be ensured by appropriate selection of PI compensator coefficients. Therefore, duty saturation would not happen at the steady state even after including the additional injection term. Furthermore, since the injection term is constant (dtot/3) at steady state, it would not affect the phase of the modulation wave.

3.3 First-Harmonic Approximation Modeling and DC-Link Stress Calculation

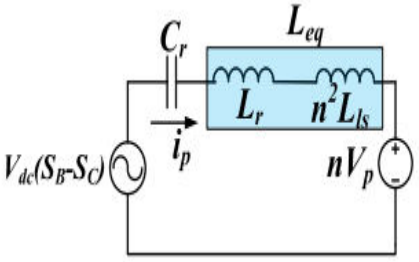

Fig. 9 Reduced structure of semi-dc/dc stage by FHA.

The dc–dc semistage can be modeled as an equivalent firstharmonic approximation (FHA) circuit structure, as shown in Fig. 9. The secondary side leakage inductance is transferred to the primary side and hence, the equivalent primary inductance becomes L eq = Llp + n2Lls. The magnitude of the voltage across the transformer primary winding will be the difference between the output voltage and the secondary filter inductor voltage. The polarity of the transformer primary voltage in the transformed circuit will be in the same polarity of the primary current (i p). This discontinuous voltage couldbe mathematically expressed in terms of sgn(i p) function, as shown in (18). The expression assumes the filter inductor current to be equal to VO/R.

$$V_p = \left(V_O - \frac{L_O}{R}\frac{dV_O}{dt}\right)\mathrm{sgn}(i_p). \tag{18}$$

In the equivalent circuit shown in Fig. 9, vBC acts as an input to the semi dc–dc stage CL tank and can be expressed as follows:

$$v_{\rm BC} = \frac{1}{C_r}\int_{-\infty}^{t} i_p dt + L_{eq}\frac{di_p}{dt} + n\left(V_O - \frac{L_O}{R}\frac{dV_O}{dt}\right)\mathrm{sgn}(i_p). \tag{19}$$

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Since our aim is to eliminate the modulating component of the line–line voltage and just utilize the switching frequency component in order to transfer the power through transformer action, FHA could be applied to the semi dc–dc stage of the converter. VBC would depend on the dc-link voltage, switching states of phase "B" and "C" and thus, taking its first harmonic using generalized state-space averaging (GSSA) technique, the following relationship could be formed. It is assumed that the first-harmonic component of the output voltage is negligible in comparison with its average value i.e.,

$$\langle v_{\mathrm{BC}}\rangle_1 = \frac{\langle i_p\rangle_1}{j\omega C_r} + j\omega L_{eq}\langle i_p\rangle_1 + nV_O\langle \mathrm{sgn}(i_p)\rangle_1 - nV_O\frac{j\omega L_O}{R}\langle \mathrm{sgn}(i_p)\rangle_1 \quad (20)$$

Substituting vBC = VDC(SB − SC) in the above relationship, the following expression is derived:

$$\langle \mathrm{sgn}(i_p)\rangle_1 = \frac{V_{\mathrm{dc}}\langle S_B - S_C\rangle_1 - \langle i_p\rangle_1[j\omega L_{eq} + \frac{1}{j\omega C_r}]}{nV_O(1 - \frac{j\omega L_O}{R})}. \quad (21)$$

Since the reduced circuit structure is modeled according to the FHA, the instantaneous power balance could be applied by equating the output power to the sum of the products of vBC and i p with taking their dc and first-harmonic components, presented in (22)

$$P = \langle v_{\mathrm{BC}}\rangle_0\langle i_p\rangle_0 + \langle v_{\mathrm{BC}}\rangle_1\langle i_p\rangle_1 = \frac{V_O^2}{R}. \quad (22)$$

Further reduction of the above equation is achieved by applying the fact that the average current through the resonant capacitor i.e., i p0 is zero and also, the convolution principle of GSSA is applied, which generates the following relation:

$$\begin{aligned} P &= \langle V_{\mathrm{dc}}\rangle_1\langle (S_B - S_C)\rangle_0\langle i_p\rangle_1 \\ &\quad + \langle V_{\mathrm{dc}}\rangle_0\langle (S_B - S_C)\rangle_1\langle i_p\rangle_1 \\ &= V_{\mathrm{dc}}\langle (S_B - S_C)\rangle_1\langle i_p\rangle_1. \end{aligned} \quad (23)$$

Furthermore, the fact that the average current through the intermediate dc-link capacitor is zero implies idc0 = 0. The currents through the three high-side switches of threephase legs are ia, ib − i p, ic + i p, respectively. Therefore, the instantaneous dc-link current is sum of these three currents weighted by their individual switching functions SA, SB, and SC, respectively, presented in (24)

$$\begin{aligned} i_{\mathrm{dc}} &= S_A i_a + S_B(i_b - i_p) + S_C(i_c + i_p) \\ &= (S_A - S_C)i_a + (S_B - S_C)i_b - (S_B - S_C)i_p. \end{aligned} \quad (24)$$

Taking the first harmonic of the above equation using GSSA and assuming the line currents to be constant over a switching period, the following is obtained:

$$\begin{aligned} &\langle i_{\mathrm{dc}}\rangle_1 \\ &= \langle (S_A - S_C)\rangle_1 i_a + \langle (S_B - S_C)\rangle_1 i_b \\ &\quad - \langle (S_B - S_C)\rangle_0\langle i_p\rangle_1 \\ &= \langle (S_A - S_C)\rangle_1 i_a + \langle (S_B - S_C)\rangle_1 i_b - (d_b - d_c)\langle i_p\rangle_1. \end{aligned} \quad (25)$$

Assuming a p% voltage ripple appearing on the intermediate dc-link capacitor i.e., Vdc = pVdc, the ac component of the dc-link capacitor current is given by: idc1 = CpVdc/Ts, where Ts is the switching period. Thus, substituting

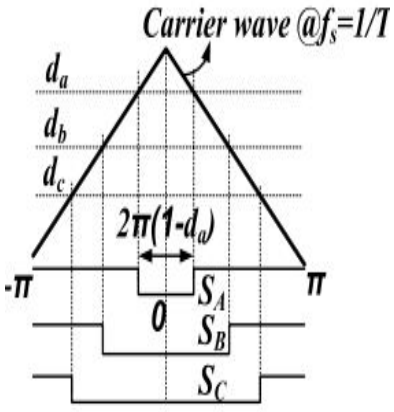

Fig. 10. Switching function generation.

this idc1 in (23), the expression of i p1 can be determined as follows:

$$\langle i_p\rangle_1 = \frac{pCV_{\mathrm{dc}}/T_s - \langle (S_A - S_C)\rangle_1 i_a - \langle (S_B - S_C)\rangle_1 i_b}{-(d_b - d_c)}. \quad (26)$$

The switching function SA with an instantaneous duty ratio da can be graphically represented by comparing a constant value with a triangular carrier signal, which has the same function as saw-tooth signal but gives more simplicity to the calculation. It is demonstrated in Fig. 10.

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$$FV_{dc}^2 + GV_{dc} + H = 0$$

$$\text{where} F = \frac{pC\langle (S_B - S_C)\rangle_1}{T_s(d_c - d_b)}$$

$$G = \frac{\langle (S_A - S_C)\rangle_1 i_a + \langle (S_B - S_C)\rangle_1 i_b}{(d_b - d_c)}$$

$$H = \frac{-V_0^2}{R}. \qquad (27)$$

4. INDUCTION MOTOR

An asynchronous motor type of an induction motor is an AC electric motor in which the electric current in the rotor needed to produce torque is obtained by electromagnetic induction from the magnetic field of the stator winding. An induction motor can therefore be made without electrical connections to the rotor as are found in universal, DC and synchronous motors. An asynchronous motor's rotor can be either wound type or squirrel-cage type.

Three-phase squirrel-cage asynchronous motors are widely used in industrial drives because they are rugged, reliable and economical. Single-phase induction motors are used extensively for smaller loads, such as household appliances like fans. Although traditionally used in fixed-speed service, induction motors are increasingly being used with variable-frequency drives (VFDs) in variable-speed service. VFDs offer especially important energy savings opportunities for existing and prospective induction motors in variable-torque centrifugal fan, pump and compressor load applications. Squirrel cage induction motors are very widely used in both fixed-speed and variable-frequency drive (VFD) applications. Variable voltage and variable frequency drives are also used in variable-speed service.

In both induction and synchronous motors, the AC power supplied to the motor's stator creates a magnetic field that rotates in time with the AC oscillations. Whereas a synchronous motor's rotor turns at the same rate as the stator field, an induction motor's rotor rotates at a slower speed than the stator field. The induction motor stator's magnetic field is therefore changing or rotating relative to the rotor. This induces an opposing current in the induction motor's rotor, in effect the motor's secondary winding, when the latter is short-circuited or closed through external impedance. The rotating magnetic flux induces currents inthe windings of the rotor; in a manner similar to currents induced in a transformer's secondary winding(s). The currents in the rotor windings in turn create magnetic fields in the rotor that react against the stator field. Due to Lenz's Law, the direction of the magnetic field created will be such as to oppose the change in current through the rotor windings. The cause of induced current in the rotor windings is the rotating stator magnetic field, so to oppose the change in rotor-winding currents the rotor will start to rotate in the direction of the rotating stator magnetic field. The rotor accelerates until the magnitude of induced rotor current and torque balances the applied load. Since rotation at synchronous speed would result in no induced rotor current, an induction motor always operates slower than synchronous speed.The difference, or "slip," between actual and synchronous speed varies from about 0.5 to 5.0% for standard Design B torque curve induction motors. The induction machine's essential character is that it is created solely by induction instead of being separately excited as in synchronous or DC machines or being self-magnetized as in permanent magnet motors.

For rotor currents to be induced the speed of the physical rotor must be lower than that of the stator's rotating magnetic field (n_s); otherwise the magnetic field would not be moving relative to the rotor conductors and no currents would be induced. As the speed of the rotor drops below synchronous speed, the rotation rate of the magnetic field in the rotor increases, inducing more current in the windings and creating more torque. The ratio between the rotation rate of the magnetic field induced in the rotor and the rotation rate of the stator's rotating field is called slip. Under load, the speed drops and the slip increases enough to create sufficient torque to turn the load. For this reason, induction motors are sometimes referred to as asynchronous motors. An induction motor can be used as an induction generator, or it can be unrolled to form a linear induction motor which can directly generate linear motion.

Synchronous Speed:

The rotational speed of the rotating magnetic field is called as synchronous speed.

$$Ns = \frac{120 \text{ x } f}{P} \quad (RPM) \qquad (28)$$

Where, f = frequency of the supply

P = number of poles

Slip:

Rotor tries to catch up the synchronous speed of the stator field, and hence it rotates. But in practice, rotor never succeeds in catching up. If rotor catches up the stator speed, there won't be any relative speed between the stator flux and the rotor, hence no induced rotor current and no torque production to maintain the rotation. However, this won't stop the motor, the rotor will slow down due to lost of torque, and the torque will again be exerted due to relative speed. That is why the rotor rotates at speed which is always less the synchronous speed.

The difference between the synchronous speed (Ns) and actual speed (N) of the rotor is called as slip.

$$\% \text{ slip} \quad s = \frac{Ns - N}{Ns} \text{ x } 100 \qquad (29)$$

(5) SIMULATION RESULTS:

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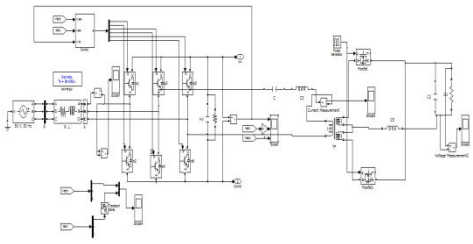

Fig 11
Simulink diagram of Proposed AC-DC Converter

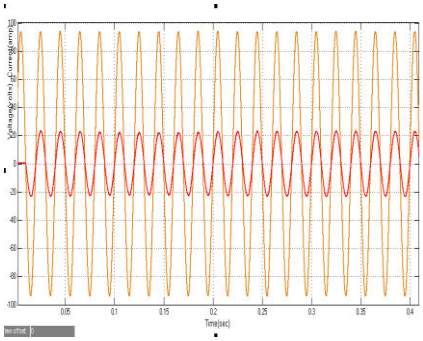

Fig 12
Simulation results of the proposed ac–dc converter. Phase "A" voltage (V) and current (A).

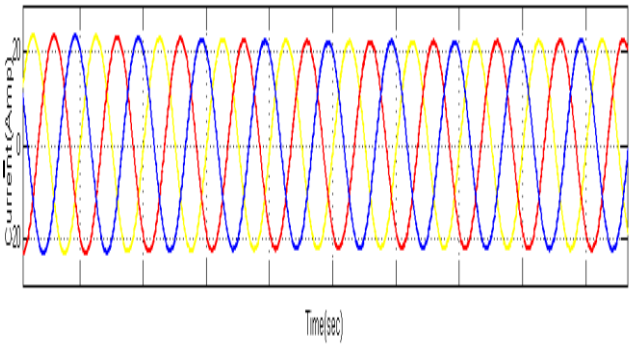

Fig 13 Simulation results of the proposed ac–dc converter of Three-phase currents (A).

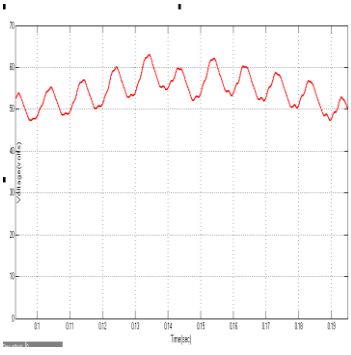

Fig 14 Simulation results of the proposed ac–dc converter of Output dcvoltage (V).

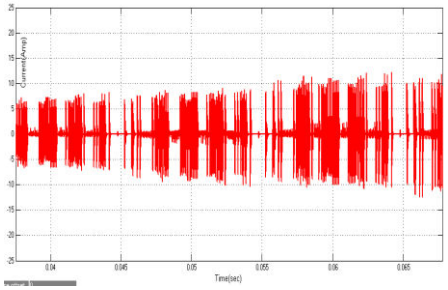

Fig 15 Simulation results of the proposed ac–dc converter of Primary side transformerCurrent (A).

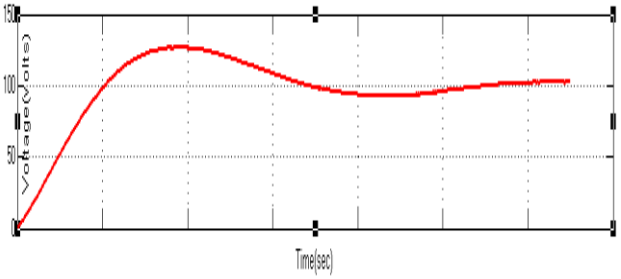

Fig 16 Simulation results of the proposed ac–dc converter of Intermediate dc-link voltage (V)

The converter is simulated in PSIM with an input ac voltage of 115 V (phase-neutral RMS) at 400 Hz. The output voltage is regulated at 28 V. Fig. 12-16. Demonstrates some simulation results for a 2.1-kW converter. The input current is in phase with the input voltage with power factor of 0.99.

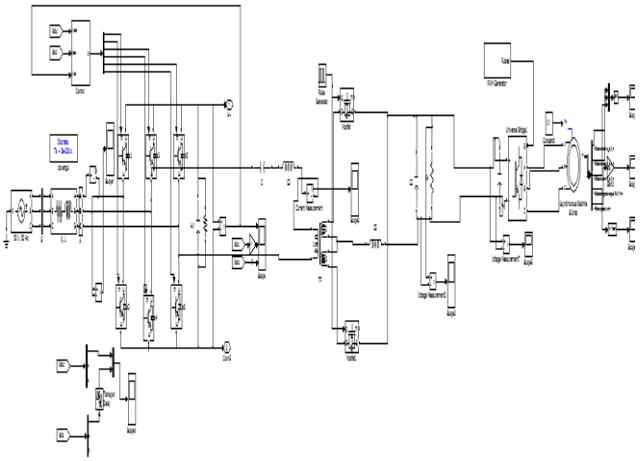

Fig 17 Simulink diagram of Proposed System power converter with Induction Motor drive

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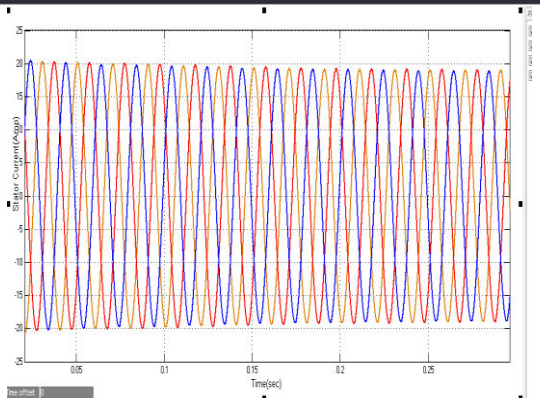

Fig 18 Simulation waveforms of Induction motor drive stator current characteristics

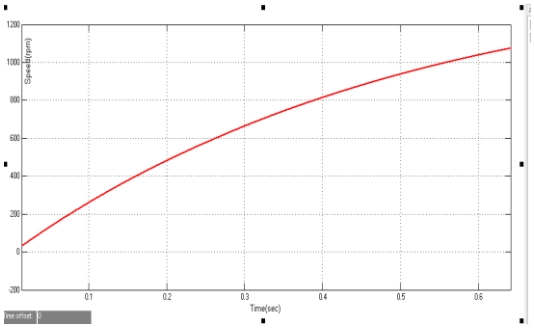

Fig 19 Simulation waveforms of Induction motor drive speed characteristics

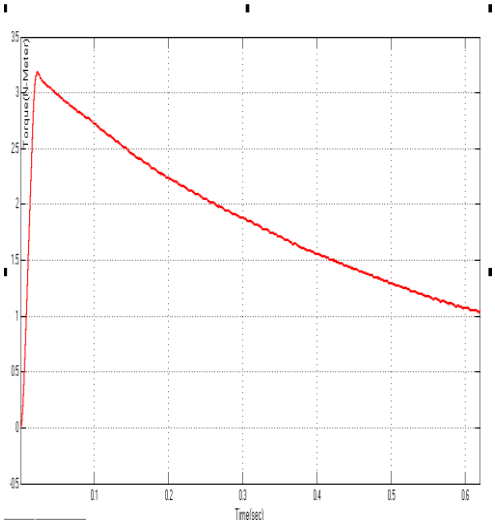

Fig 20 Simulation waveforms of Induction motor drive Torque characteristics

(6) CONCLUSION

Numerous industrial applications have begun to require higher power apparatus in recent years. Power-electronic converters are becoming popular for various industrial applications. In this concept a new three level AC to DC converter for a novel three-phase single-stage ac–dc converter with Induction motor Drive is proposed and analyzed. This topology eliminates four switches and their associated heat sinks from the dc–dc stage in the conventional two-stage structure. Only eight switches are utilized to implement >0.99 power factor and a stepped down isolated regulated output dc voltage, which makes it a cost-effective and compact solution for ac–dc conversion. In addition, the intermediate dc-link capacitor can be smaller to further reduce the weight and size. Furthermore, six switches in the converter can achieve ZVS to minimize the switching loss. Compared with other single-stage converters operating in DCM mode, the prospective converter works in CCM mode, which reduces the current stress through the semiconductor devices. By injecting an additional duty ratio component in the control loop, the harmonics in phase currents are reduced.The converter can operate with lower peak voltage stresses across the switches and the DC bus capacitors as it is a three-level converter. This converter provides variable output voltage with improved power factor. The all simulation results are verified through Matlab/simulink software.

REFERENCES

[1] P. Barbosa, F. Canales, and F. C. Lee, “A front-end distributed power system for high-power applications,” in Proc. IEEE Ind. Appl. Conf., Oct. 2000, pp. 2546–2551.
[2] Y. Jang and M. M. Jovanovic, “A novel, robust, harmonic injection method for single switch, three-phase, discontinuous-conductionmode boost rectifiers,” in Proc. IEEE Power Electron. Specialists Conf. (PESC), Jun. 1997, pp. 469–475.
[3] A. Prasad, P. D. Ziogas, and S. Manias, “An active power factor correction technique for three-phase diode rectifiers,” IEEE Trans. Power Electron., vol. 6, no. 1, pp. 83–92, Aug. 2002.
[4] J. R. Rodriguez, J. W. Dixon, J. R. Espinoza, J. Pontt, and P. Lezana, “PWM regenerative rectifiers: State of the art,” IEEE Trans. Ind. Electron., vol. 52, no. 1, pp. 5–22, Feb. 2005.
[5] J. W. Kolar and T. Friedli, “The essence of three-phase PFC rectifier systems—Part I,” IEEE Trans. Power Electron., vol. 28, no. 1, pp. 176–198, Jan. 2013.
[6] C. Shi and A. Khaligh, “An interleaved SEPIC power factor pre-regulator using coupled inductors in discontinuous conduction mode with wide output voltage,” IEEE Trans. Ind. Appl., vol. 53, no. 1, pp. 501–511, Jan. 2017.
[7] Y. Jiang, H. Mao, F. C. Lee, and D. Borojevic, “Simple high performance three-phase boost rectifiers,” in Proc. IEEE Power Electron. Specialists Conf. (PESC), Taipei, Taiwan, Jun. 1994, pp. 1158–1163.

[8] G.-B. Koo, G.-W. Moon, and M.-J. Youn, "New zero-voltage-switching phase-shift full-bridge converter with low conduction losses," IEEE Trans. Ind. Electron., vol. 52, no. 1, pp. 228–235, Feb. 2005.
[9] Y. Jang and M. M. Jovanovic, "A new PWM ZVS full-bridge converter," IEEE Trans. Power Electron., vol. 22, no. 3, pp. 987–994, May 2007.
[10] P. K. Jain, W. Kang, H. Soin, and Y. Xi, "Analysis and design considerations of a load and line independent zero voltage switching full bridge DC/DC converter topology," IEEE Trans. Power Electron., vol. 17, no. 5, pp. 649–657, Sep. 2002.
[11] A. Mallik and A. Khaligh, "Reduced-state-observer-based feedback control system design of a two-staged AC-DC converter," IEEE Trans. Ind. Electron., vol. 64, no. 8, pp. 6371–6382, Aug. 2017.
[12] C. Shi, H. Wang, and A. Khaligh, "A SiC based PEV onboard charger with ultra-wide DC link voltage range," IEEE Trans. Ind. Appl., vol. 52, no. 4, pp. 3461–3471, Apr. 2016.
[13] H. Wang and H. Chung, "A novel concept to reduce the DC-link capacitor in PFC front-end power conversion systems," in Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC), Orlando, FL, USA, Feb. 2012, pp. 1192–1197.
[14] B. Fuld, S. Kern, and R. Ridley, "A combined buck and boost powerfactor-controller for three-phase input in power electronics and applications," in Proc. IEEE Eur. Conf. Power Electron. Appl., Brighton, U.K., Sep. 1993, pp. 144–148.
[15] R. Ridley, S. Kern, and B. Fuld, "Analysis and design of a wide input range power factor correction circuit for three-phase applications," in Proc. 8th Annu. Appl. Power Electron. Conf. Expo. (APEC), Mar. 1993, pp. 299–305.
[16] J. Klima, J. Skramlik, and V. Valouch, "Three-phase four-switch PFC and its analytical model," in Proc. IEEE Power Eng., Energy Elect. Drives, Apr. 2007, pp. 66–71.
[17] V. F. Pires and J. F. Silva, "Three-phase single-stage four-switch PFC buck-boost-type rectifier," IEEE Trans. Ind. Electron., vol. 52, no. 2, pp. 444–453, Apr. 2005.
[18] J. W. Kolar, F. Stogerer, J. Minibock, and H. Ertl, "A new concept for reconstruction of the input phase currents of a three-phase/switch/level PWM (VIENNA) rectifier based on neutral point current measurement," in Proc. IEEE Power Electron. Specialists Conf. (PESC), Galway, Ireland, Jun. 2000, pp. 139–146.
[19] J. S. Yang, T. J. Liang, J. F. Chen, and R. L. Lin, "Analysis and design of a novel, single-stage, three-phase AC/DC step-down converter with electrical isolation," IET Power Electron., vol. 1, no. 1, pp. 154–163, Mar. 2008.
[20] Y. Panov, J. F. Cho, and F. C. Lee, "Zero-voltage-switching three-phase single-stage power factor correction convertor," IEE Proc.-Electr. Power Appl., vol. 144, no. 5, pp. 343–348, Aug. 2002.
[21] M. Tao, B. Hongqi, W. Daqing, and J. Zhang, "Research on a novel three-phase single-stage boost DCM PFC topology and the dead zone of its input current," in Proc. IEEE Appl. Power Electron. Conf. Expo., Washington, DC, USA, Feb. 2009, pp. 1862–1866.
[22] F. Canales, P. Barbosa, C. Aguilar, and F. C. Lee, "A quasi-integrated AC/DC three-phase dual-bridge converter," in Proc. IEEE Power Electron. Specialists Conf. (PESC), Vancouver, BC, Canada, Jun. 2001, pp. 1893–1898.
[23] M. Baumann, U. Drofenik, and J. W. Kolar, "New wide input voltage range three-phase unity power factor rectifier formed by integration of a three-switch buck-derived front-end and a DC/DC boost converter output stage," in Proc. IEEE INTELEC, Phoenix, AZ, USA, Sep. 2000, pp. 461–470.
[24] J. G. Contreras and I. Barbi, "Modeling and control of a three-phase high power factor PWM-ZVS power supply with a single power stage," in Proc. IEEE Int. Power Electron. Congr., Tech. (CIEP), Oct. 1996, pp. 149–154.
[25] J. G. Contreras and I. Barbi, "A three-phase high power factor PWM ZVS power supply with a single power stage," in Proc. IEEE Power Electron. Specialists Conf., Taipei, Taiwan, Jun. 1994, pp. 356–362.
[26] F. S. Hamdad and A. K. S. Bhat, "A novel soft-switching high-frequency transformer isolated three-phase AC-to-DC converter with low harmonic distortion," IEEE Trans. Power Electron., vol. 19, no. 1, pp. 35–45, Jan. 2004.
[27] D. Wijeratne and G. Moschopoulos, "Three-phase single-stage AC-DC converters," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), Paris, France, May 2010, pp. 3701–3704.
[28] 3C94 Material Specification, Ferroxcube, Taipei, Taiwan, Sep. 2008.
[29] A. Mallik and A. Khaligh, "Variable switching frequency state feedbackcontrol of a phase shifted full bridge DC/DC converter," IEEE Trans. Power Electron., vol. 32, no. 8, pp. 6523–6531, Aug. 2017.
[30] A. Mallik, W. Ding, C. Shi, and A. Khaligh, "Input voltage sensorless duty compensation control for a three-phase boost PFC converter," IEEE Trans. Ind. Appl., vol. 53, no. 2, pp. 1527–1537, Mar. 2017.