International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

COPY RIGHT

IJIEMR Transactions, online available on 25th Oct 2017. Link :http://www.ijiemr.org/downloads.php?vol=Volume-6&issue=ISSUE-9

Title: LOW POWER OPTIMIZED LOGIC SYNTHESIS OF REVERSIBLE PLA

Volume 06, Issue 09, Pages: 271 – 275.

Paper Authors

KUKKAMUDI.NAGENDRA, KANNEKANTI VINAY KUMAR

Nalgonda Institute Of Technology And Science (NITS)

.

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per UGC Guidelines We Are Providing A Electronic Bar Code

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

LOW POWER OPTIMIZED LOGIC SYNTHESIS OF REVERSIBLE PLA

[1]KUKKAMUDI.NAGENDRA, [2]KANNEKANTI VINAY KUMAR
[1]M.Tech Scholar,Dept of E.C.E(VLSI & ES), Nalgonda Institute Of Technology And Science (NITS)
[2]Assistant Professor, Dept of E.C.E, Nalgonda Institute Of Technology And Science (NITS)

ABSTRACT—Reversible logic have been motivated by consideration of zero energy computation.Reconfigurability and structural regularity of Programmable Logic Devices caused wide use of it by the logic designers. In this paper, we propose a design algorithm for a PLA(Programmable Logic Array) with a newly designed low cost3 × 3 reversible NMG (New Mux Gate) circuit for Implementing multi-output ESOP (Exclusive-OR Sum of Product) functions. In addition, we propose a heuristic to sort and to realize the product terms of ESOP functions in order to share the internal sub-products to reduce the number of gates in the proposed circuit. The proposed Algorithms make the design efficient with improvement in number of gates, garbage count and quantum cost metric than existing technique save ragely. Performance is also analyzed by using MCNC benchmark circuits.. The proposed architecture of this paper analysis the logic size and area using Xilinx 14.3.

Index Terms—Reversible logic, Quantum Computing, PLA,non-reversible counterparts.

I. INTRODUCTION

Hardware used. Then using the same reversible adder, a Wallace tree multiplier has been implemented, and compared with the conventional Wallace tree multiplier. With the known fact that sequential circuits are the heart of digital designing, the design for the control unit of a reversible GCD processor has been proposed using Reversible logic gates.

II. REVERSIBLE LOGIC

Logic gates is said to be reversible if the set of inputs mapped have an equal number of outputs mapped i.e. they have one-to-one correspondence. This is realized employing reversible gates in the designs. Any circuit having only reversible gates is capable of dissipating no power.

Factors of Reversible Logic:

1. Quantum Cost: Quantum cost of a circuit is the measure of implementation cost of quantum circuits. More precisely, quantum cost is defined as the number of elementary quantum operations needed to realize a gate Reversible logic is widely used in low power VLSI for higher speed of operation. Reversible circuits are capable of back-computation and reduction in dissipated power, as there is no loss of information [1]. Basic reversible gates are employed to achieve the required functionality of a reversible circuit. The uniqueness of reversible logic is that, there is no loss of information since there is one-to-one correspondence between inputs and outputs. This enables the system to run

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

backwards and while doing so, any intermediate design stage can be thoroughly examined. The fan-out of each block in the circuit has to be one. This research paper focuses on implementation of reversible logic circuits in which main aim is to optimize speed of the design. A Reversible adder is designed using basic reversible gates. Using this adder, an 8-bit reversible ripple-carry adder is devised and then compared with the conventional 8-bit adder in terms of speed, critical paths,

2. Speed of Computation: The time delay of the circuits should be as low as possible as there are numerous computations that have to be done in a system involving a quantum processor; hence speed of computation is a very important parameter while examining such systems.

3. Garbage Outputs: Garbage outputs are those output signals which do not contribute in driving further blocks in the design. These outputs become redundant as they are not required for computation at a later stage. The garbage outputs make the system slower; hence for better efficiency it is necessary to minimize the number of garbage outputs.

4. Feedback: Looping is strictly prohibited when designing reversible circuits.

5. Fan-out: The output of a certain block in the design can only drive at most one block in the design. Hence it can be said that the Fan-out is restricted to 1.

III. REVERSIBLE GATES

There are many reversible gates such as Feynman, Toffoli, TSG, Fredkin, Peres, etc [3]. As the universal gates in boolean logic are Nand and Nor, for reversible logic, the universal gates are Feynman and Toffoli gates.

1. Feynman Gate: Feynman gate is a universal gate which is used for signal copying purposes or to obtain the complement of the input signal. The block diagram of Feynman gate is shown in fig.1:

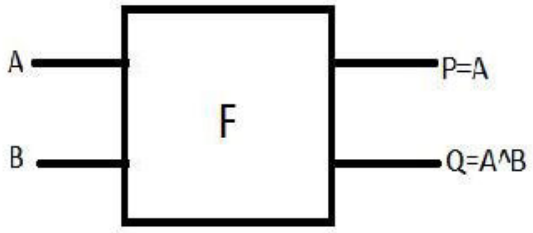

Fig. 1: Feynman Gate

2. Fredkin Gate: It is a basic reversible 3-bit gate used for swapping last two bits depending on the control bit. The control bit here is A, depending on the value of A, bits B and C are selected at outputs Q and R. When A=0, (Q=B, R=C) whereas when A=1, (Q=C, R=B). Its block diagram is as shown in fig. 2:

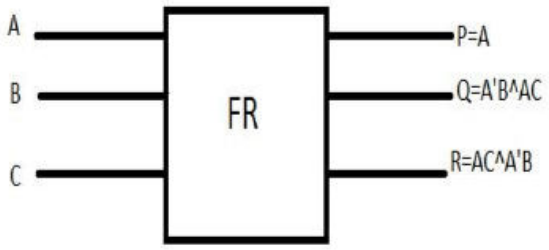

Fig. 2: Fredkin Gate

3. Peres Gate: It is a basic reversible gate which has 3-inputs and 3-outputs having inputs (A, B, C) and the mapped outputs (P=A, Q=A^B, R=(A.B)^C). The block diagram is as shown in fig. 3:

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

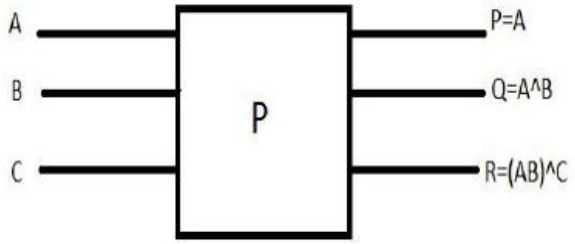

Fig. 3: Peres Gate

4. Toffoli Gate: Toffoli gate is a universal reversible gate which has three inputs (A, B, C) mapped to three outputs (P=A, Q=B, R= (A.B)^C). The block diagram of Toffoli gate is shown in fig. 4:

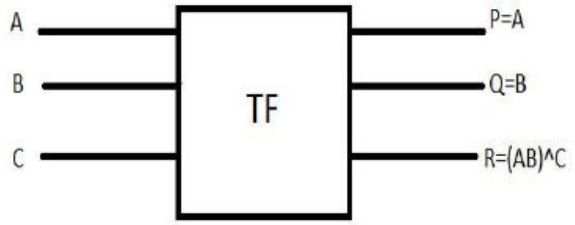

Fig. 4: Toffoli Gate

5. TSG Gate: TSG gate is a reversible gate which has four inputs (A, B, C, D) mapped to four outputs (P=A,Q=A^B,R=A^B^D,S=(A^B)^D^AB^C). The block diagram of TSG Gate is shown in fig. 5:

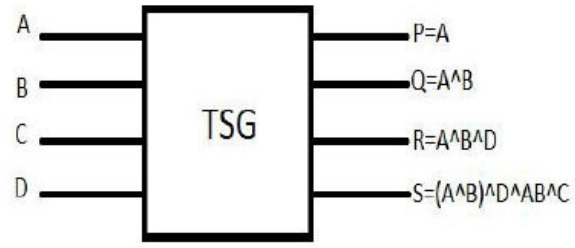

Fig. 5: TSG Gate

IV. LOGIC ANALYSIS IN THE PROPOSED REVERSIBLE PLA

A. Proposed Reversible gate:

A 3×3 reversible gate namely "New Mux Gate" gate or "NMG" is proposed which is drawn in Fig.6. The NMG gate can be defined as I = (A ,B ,C) and O = (P = A⊕B), Q = B'C⊕AC', R= BC⊕AC'), Where I and O are the input and output vectors respectively. The corresponding truth table of the NMG gate is shown in TABLE I. It can be verified from the truth table that the input pattern corresponding to a particular output pattern can be uniquely determined.

B. Design of Reversible Programmable Logic Array (RPLA)

In this section, we will describe our proposed design of Reversible Programmable Logic Array. In this structure,we will synthesize the multiple-output ESOP functions using different configurations of NMG gates. In multi-output ESOP, some products may be common among different output functions. We will also take the advantage of those terms like as irreversible PLA. The main constraint is that the fan-out of all signals in a reversible gate is one. Therefore, a single wire for a single product, having several cross points like those that irreversible PLA is not allowed in the proposed design. So, the appropriate copy in each product should be ensured to handle fan-out problem. In the synthesis method for multi-output ESOP using the RPLA, it is assumed that the multi-output circuit has been already minimized and is available in an ESOP format. For convenience we will denote different modes of operation of NMG, Feyman and Feyman Double gate as shown in Fig. 7.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

Table I. Truth Table of The Proposed Reversible Nmg Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	1	1	0
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	1	0	1	0

V. SIMULATION RESULT AND PERFORMANCE ANALYSIS

Our algorithms for realization and minimization of RPLA have been written using language C and have tested extensively on windows microcomputer. Several experimental results are given below using an Intel core i5 Desktop CPU 2.3 GHz under Microsoft Windows 7 edition with 2 GB RAM. During the execution it was ensured that no other application is running. Table III shows the experimental results comparing the proposed methods with the methods presented in [11, 12, 13] in terms of the number of garbage outputs and the number of gates for ESOPs given in Equation (1). Comparisons are also given in Table IV for corresponding benchmark functions. Fig. 9. Simulation result of NMG gate.

Table II. Comparison Among Different Designs For Equation (1).

	Gate	Garbage	Quantum cost
Existing[11]	19	11	47
Existing[12]	18	7	39
Existing[13]	17	19	55
Proposed design	14	6	31

VI. CONCLUSION

In this paper, compact structure of Reversible Programmable Logic Array (RPLA) is presented. A reversible gate with low cost is proposed to generate the AND terms of RPLA which can produce two different AND terms at the same time. Using this property we can ensure the reduction of gate count. Two algorithms are proposed to minimize the previous architecture of RPLA that can realize any multi-output ESOP (Exclusive-OR Sum of Product) function. In addition, simulation of the proposed gate has shown that it works correctly. Finally, benchmark analysis proves the optimization of all the parameters. This design methodology improved 14.9%, 2.29% and 9.96% than [11], [12] and [13], respectively in terms of number of gates. It produced 39% and 12% less garbage outputs than [12] and [13], respectively. Whereas, quantum cost is reduced 17% with respect to [11] and 12% to [12]. The different number of input-output plays a major role in computing these comparisons. Working with more benchmark function is open for future research. In embedded circuits and other technologies for making low power consumption, reversible PLAs are useful [3, 7].

REFERENCES

[1] R. Landauer,“Irreversibility and heat generation in the computing pro-cess.” IBM J. Res. Dev., vol.5,no. 3, pp. 183-191, 1961.

[2] C.H. Bennett,“Logical reversibility of computation”. IBM J. Res. Dev.,vol.17, no. 6, pp. 525-532, 1973.

[3] G. Schrom and S. Selberherr. Ultra-low-power cmos technology. In

Semiconductor Conf., Romania, 2002. E.Knill, R. Laamme, and G. J. Milburn. A scheme fore-cient quantum computation with linear optics. Nature, 409:46–52, January 2001.

[4] M. A. Nielsen and I. L. Chuang. Quantum computation and quantum information, 2001.

[5] R. C. Merkle. Two types of mechanical reversible logic. Nanotechnology, 4(2):114–131, January 1993.

[6] H. Fleisher and L. I. Maissel. An introduction to array logic. IBM J. of Research and Development, 19, 1975.

[7] T. Sasao. Exmin2: A simplification algorithm for exclusive-or-sum-of-products expressions for multiple- valued input two-valued output functions. IEEE Transactions on Computer-Aided Desig n of Integrated Circuits and Systems, 12(5):621–632, 1993.

[8] A. Mishchenko and M. Perkowski. Logic synthesis of reversible wave cascades. In International Workshop on Logic Synthesis, pages 197–202, June 2002.

[9] M. Perkowski, A. B. P. Kerntof and et al. Regularity and symmetry as a base of efficient realization of reversibl logic circuits. In International Workshop on Logic Synthesis, pages 245–252, June 2001.

[10] D. Maslov and G. Dueck. Reversible cascades with minimal garbage. IEEE Transactions on CAD, 23(11):1497–1509, November 2004.