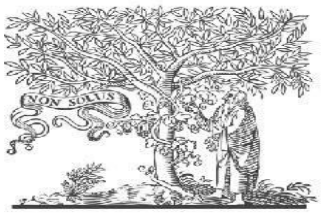
International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

COPY RIGHT



ELSEVIER SSRN

IJIEMR Transactions, online available on 5th Mar 2021. Link :http://www.ijiemr.org/downloads.php?vol=Volume-10&issue=ISSUE-03

DOI: 10.48047/IJIEMR/V10/I03/23

Title **DESIGN A HIGH-SPEED AND AREA-EFFICIENT VLSI ARCHITECTURE OF RCA USING 9T FULL ADDER**

Volume 10, Issue 03, Pages: 153-157

Paper Authors

N.ARCHANA, VENKATARAO TIRUMALASETTY

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per UGC Guidelines We Are Providing A Electronic Bar Code

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

DESIGN A HIGH-SPEED AND AREA-EFFICIENT VLSI ARCHITECTURE OF RCA USING 9T FULL ADDER

[1]N.ARCHANA, [2]VENKATARAO TIRUMALASETTY
[1]M.Tech Scholar, Dept of ECE, Mallineni Laxmaiah Women's Engineering College, Andhra Pradesh, India.
[2]Assistant Professor, Dept of ECE, Mallineni Laxmaiah Women's Engineering College, Andhra Pradesh, India.

ABSTRACT: Adders are the main components in digital designs not only in additions but also in filter designing, multiplexing, and division. The circuit performance depends on the design of base adder. The demand of high-performance VLSI (very large scale integration) systems is increasingly rapidly for used in small and portable devices. The speed of operation is depends on the delay of the basic adder and it is a very important parameter for high performance. There are so many research works have been so far done on the adder to reduce the delay of it. In this paper, Design a High-Speed and Area-Efficient VLSI Architecture of RCA using 9T Full adder is implemented. The main intent of full adder is to increase the speed of operation in the system. By using CMOS technology the entire design is designed. From results it can observe that the proposed system utilizes nodes and MOSFET' in very effective way and reduce the delay very effectively.

KEY WORDS: Full Adder, CMOS, Boundary nodes, independent nodes, total nodes.

I. INTRODUCTION

With the continuously increasing demand of laptops, portable personal communication systems and the evolution of shrinking technology, the research effort in low-power micro-electronics has been intensified and low-power VLSI systems have emerged high in demand [1]. Digital integrated circuits commonly use CMOS circuits as building blocks. The continuing decrease in feature size of CMOS circuits and corresponding increase in chip density and operating frequency have made power consumption a major concern in VLSI design.

In recent years, the growing demand for high-speed arithmetic units in CPU (central processing unit), ALU (Arithmetic logic unit), DSP (Digital signal processors) architectures and microprocessors has led to the development of high-speed adders as addition is an obligatory and indispensable function in these units. Adder is the core element of complex arithmetic circuits like addition, subtraction, multiplication, division, exponentiation etc. Thus, enhancing the performance of the full adder block leads to the enhancement of the overall system performance [2].

As a result, design of a high-performance full adder is very useful and important. Power dissipation has become a prime constraint in high performance applications, especially in portable and battery operated systems so it is necessary to reduce power consumption. With the development of CMOS technology, the minimum gate length of transistors continues to decrease, and the characteristic frequency also will be rising. With the lowering of threshold voltage in ultra deep submicron technology, lowering the supply voltage appears to be the most eminent means to reduce power

consumption. However, lowering supply voltage also increases circuit delay and degrades the drivability of cells designed with certain logic styles.

It is time we explore the well-engineered deep submicron CMOS technologies to address the challenging criteria of these emerging low-power and high-speed communication digital signal processing chips. The performance of many applications as digital signal processing depends upon the performance of the arithmetic circuits to execute complex algorithms such as convolution, correlation, and digital filtering. Fast arithmetic computation cells including adders and multipliers are the most frequently and widely used circuits in very-large-scale integration (VLSI) systems.

The semiconductor industry has witnessed an explosive growth of integration of sophisticated multimedia-based applications into mobile electronics gadgetry since the last decade. However, the critical concern in this arena is to reduce the increase in power consumption beyond a certain range of operating frequency. Moreover, with the explosive growth, the demand, and the popularity of portable electronic products, the designers are driven to strive for smaller silicon area, higher speed, longer battery life, and enhanced reliability. The XOR-XNOR circuits are basic building blocks in various circuits especially arithmetic circuits (adders & multipliers), compressors, comparators, parity checkers, code converters, error-detecting or error-correcting codes and phase detector.

II. TOPOLOGY OF FULL ADDER

In recent years, several variants of different logic styles have been proposed to implement 1-bit adder cells. There are two types of full adders in case of logic structure. One is static and the other is dynamic style. Static full adders are commonly more reliable, simpler and are lower power consuming than dynamic ones. Dynamic is an alternative logic style to design a logic function. It has some advantages over the static mode such as faster switching speeds, no static power consumption, nonratioed logic, full swing voltage levels, and lesser number of transistors. An N input logic function requires N+2 transistors versus 2N transistors in the standard CMOS logic. The area advantage comes from the fact that the pMOS network of a dynamic CMOS gate consists of only one transistor. This also results in a reduction in the capacitive load at the output node, which is the basis for the delay advantage. There are various issues related to the full adder like power consumption, performance, area, noise immunity, regularity and good driving ability. Many researchers have combined these two structures and have proposed hybrid dynamic-static full adders. They have investigated different approaches realizing adders using CMOS technology each having its own pros and cons.

These full adders usually have low number of transistors- (3T-) based XOR-XNOR circuit, less power consumption, and less area occupation. The nonfull swing full adders are useful in building up larger circuits as multiple bit input adder and multipliers. One such application is the Manchester Carry-Look Ahead chain. The full adders of first group have good driving ability, high number of transistors, large area, and usually higher power consumption in comparison to the second group.

There are standard implementations for the full-adder cells which are used as the basis

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

of comparison in this paper. Some of the standard implementations are as follows.

CMOS logic styles have been used to implement the low-power 1-bit adder cells. In general, they can be broadly divided into two major categories: the Complementary CMOS and the Pass-Transistor logic circuits. The complementary CMOS (C-CMOS) full adder (Figure 1) is based on the regular CMOS structure [3, 4, 29]. The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing, which are essential to provide reliable operation at low voltage with arbitrary transistor sizes.

III. PROPOSED SYSTEM

The below figure (1) shows the schematic of proposed system. In this 89 transistors are used. To design this circuit 72 MOSFET's are used. Basically, total nodes are classified into two types they are boundary nodes and independent nodes. 51 total nodes are utilized for this designing, 25 independent nodes and 26 boundary nodes are required in total.

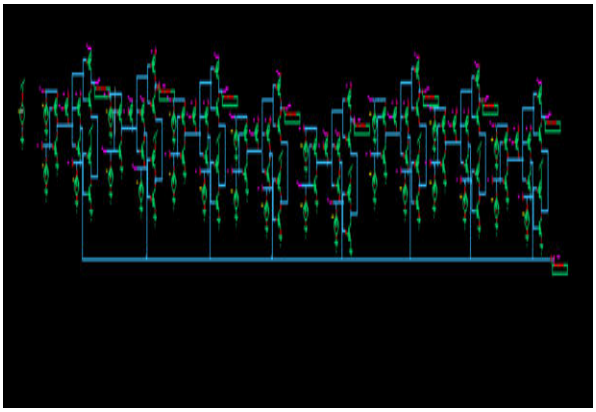


Fig. 1: SCHEMATIC OF PROPOSED SYSTEM

The pass-transistor logic (PTL) is a better way to implement circuits designed for low power applications. The low power pass-transistor logic and its design analysis procedures were reported. Its advantage is that one pass-transistor network (either pMOS or nMOS) is sufficient to implement the logic function, which results in lower number of transistors and smaller input load. Moreover, direct-to-ground paths, which may lead to short-circuit energy dissipation, are eliminated.

Pseudo nMOS full adder cell operates on pseudo logic, which is referred to as ratioed style. This full adder cell uses 14 transistors to realize the negative addition function. The advantage of pseudo nMOS adder cell is its higher speed (compared to conventional full adder) and less transistor count. The disadvantage of pseudo nMOS cell is the static power consumption of the pull-up transistor as well as the reduced output voltage swing, which makes this adder cell more susceptible to noise. To increase the output swing, CMOS inverter is added to this circuit.

Transmission gate consists of a pMOS transistor and an nMOS transistor that are connected in parallel, which is a particular type of pass-transistor logic circuit. There is no voltage drop at output node, but it requires twice the number of transistors to design similar function. Some designs of the full adder circuit based on transmission gates are shown in Figure 1. Transmission gate logic circuit is a special kind of pass-transistor logic circuit. It exhibits better speed and less power dissipation than the conventional CMOS adder due to the small transistor stack height.

Intermediate XOR and XNOR are generated using three transistor (9T) XOR and XNOR gate. Sum and Carry are generated using two double transistors multiplexers. 9T XOR and XNOR consume high energy due to short circuit current in ratio logic. They all have double threshold losses in full adder output terminals.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

IV. RESULTS

The below figure (2) shows the output waveform of proposed system.

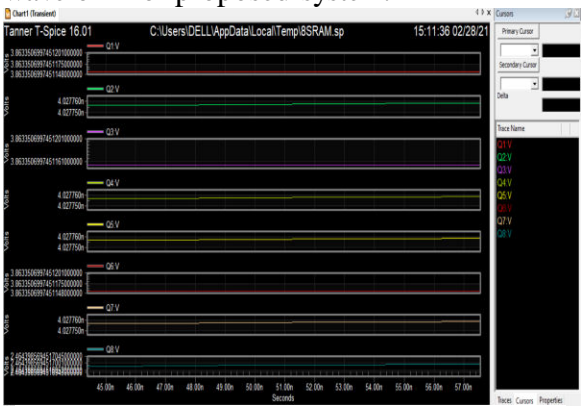
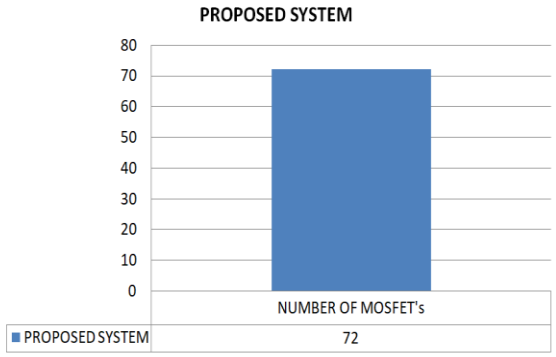


Fig. 2: OUTPUT WAVEFORM OF PROPOSED SYSTEM

The below figure (3) shows the utilization of number of MOSFET's in proposed system.



Fig, 3: MOSFTE's UTILIZATION

The below figure (4) shows the number of nodes used in proposed system.

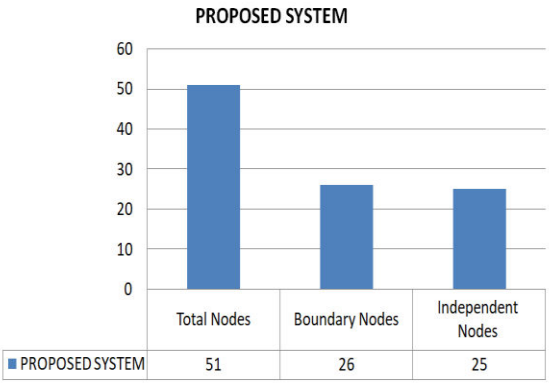


Fig. 4: NODES UTLIZATION IN PROPOSED SYSTEM

The below figure (5) shows the graph of delay reduction in proposed system.

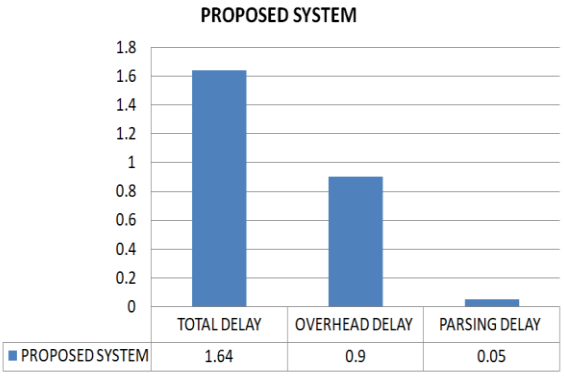


Fig. 5: DELAY IN PROPOSED SYSTEM

V. CONCULSION

An alternative internal logic structure for designing full adder cells is introduced. In order to demonstrate its advantages, full adders were built in combination with logic styles. Using the adder categorization and CMOS design style, many full adders can be conceived.. Hence in this paper, Design a High-Speed and Area-Efficient VLSI Architecture of RCA using 9T Full adder is implemented. From results, it can observe the utilization of nodes, MOSFET's and reduction of delay in very effective way.

VI. REFERENCES

[1] Vishwa Shah, Urvisha Fata, Jagruti Makwana, " Design and Performance Analysis of 32 Bit VLSI Hybrid adder", Proceedings of the Third International Conference on Trends in Electronics and Informatics (ICOEI 2019) IEEE Xplore Part Number: CFP19J32-ART; ISBN: 978-1-5386-9439-8.

[2] R. Zimmermann, "Binary adder architectures for cell-based VLSI and their synthesis," Ph.D. thesis, Swiss Federal Institute of Technology, (ETH) Zurich, Zurich, Switzerland, 1998, Hartung-Gorre Verlag.

[3] R. P. Brent and H. T. Kung, "A regular

layout for parallel adders," *IEEE Trans. Comput.*, vol. C-31, no. 3, pp. 260–264, Mar. 1982.
[4] P. M. Kogge and H. S. Stone, "A parallel algorithm for the efficient solution of a general class of recurrence equations," *IEEE Trans.Comput.*, vol. C-22, no. 8, pp. 786–793, Aug. 1973.
[5] J. Sklansky, "Conditional-sum addition logic," *IRE Trans. Electron. Comput.*, vol. EC-9, pp. 226–231, Jun. 1960.
[6] T. Han and D. A. Carlson, "Fast area-efficient VLSI adders," in *Proc. IEEE 8th Symp. Comput. Arith. (ARITH)*, May 18–21, 1987, pp. 49–56.
[7] R. E. Ladner and M. J. Fischer, "Parallel prefix computation," *J. ACM*, vol. 27, no. 4, pp. 831–838, Oct. 1980
[8] Bernd Becker, "Efficient testing of optimal time adders," Proc. IEEE, Vol. 37, pp. 1113-1120, Sept. 1988.
[9] I. Flores, "The Logic of Computer Arithmetic," Chaps. 4, 5 and 7, Englewood Cliffs, N.J, Prentice Hall, 1963.
[10] O.L. Macsorley, "High-Speed Arithmetic in Binary Computers," Proc. IRE, Vol. 49, pp. 67-91, Jan. 1961.
[11] J. Slansky, "Conditiona1-Sum Additional Logic," Proc. IRE Trans. Electronic Computers, Vol. 9, pp. 226-231, June 1960.
[12] J.B. Gosling, "Conditional-Sum Early Completion Logic," IRE Trans. Electronic Computers, Vol. 59, pp. 226-231.

[1]**N.ARCHANA** Completed B.Tech from Vijaya Institute of Technology, Andhra Pradesh, India and pursuing M.Tech from Mallineni Laxmaiah Women's Engineering college, Andhra Pradesh, India. Her M.Tech specialization is VLSI Design.

[2]**VENKATARAO TIRUMALASETTY** completed B.Tech at Mallineni Laxmaiah Women's Engineering college, Andhra Pradesh, M.Tech from Vignan University, Andhra Pradesh, India. He has 8 years of teaching experience and working as Assistant professor at Mallineni Laxmaiah Women's Engineering college, Guntur, A.P, India. He has professional membership in IAENG. His interested area of research is Low power VLSI..