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PERFORMANCE ANALYSIS OF SYNCHRONOUS RECTIFIER BASED ZVS CONVERTER FED INDUCTION MOTOR DRIVER

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ABSTRACT- The generalized methodology allows multiphase SDSRs to be designed to replace the multiphase diode rectifiers. Unlike the traditional SR that is designed for high-frequency power converters, the SDSR proposed here can be a direct replacement of the power diode bridges for both low- and high-frequency operations. The SDSR utilizes its output dc voltage to supply power to its control circuit. No start-up control is needed because the body diodes of the power MOSFETs provide the diode rectifier for the initial start-up stage. The generalized method is demonstrated in 2-kW one-phase and three-phase SDSRs for inductive, capacitive, and resistive loads. Power loss reduction in the range of 50%-69% has been achieved for the resistive load. In this project, a soft-switching buck power-factor-correction (PFC) converter for a high-efficiency AC-DC light-emitting diode (LED) driver is proposed. By replacing a freewheeling diode with a self-driven synchronous rectifier (SR), efficiency improvement is achieved due to the reduced conduction loss on the SR. In addition, there is no switching loss on switching devices because zero-voltage-switching (ZVS) operations of both switches are easily performed. Since the SR is self-driven without an additional control circuit, the proposed converter has competitive price. In order to verify efficiency improvement of the proposed converter, it is compared with a conventional critical-conduction-mode (CRM) buck PFC converter. For verifying soft-switching and efficiency improvement of the proposed converter, design consideration by using MATLAB/Simulink.

Index Terms—Buck-boost converter, LED driver, power factor correction (PFC), synchronous rectifier, zero-voltage-switching (ZVS).

I. INTRODUCTION

Electric Lighting is an essential part of our lives, and is a major component in energy consumption. The types of lighting devices commonly adopted for electric lighting is the incandescent lamps, the gas-discharge lamps and solid state lighting devices. There are various dimming techniques introduced for different types of lighting devices. For incandescent lamps, dimming is typically performed by controlling the firing angle of a thyristor [1-2].For Gas discharge lamps, dimming technique revolve around the control of voltage level, duty cycle and frequency. For solid-state lighting devices, the dimming technique is to vary the dc level of the forward current [3].The high efficiency LED system needs the high-efficiency power supply to feed the LED[4]. LEDs are very attractive lighting

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sources due to their excellent characteristics. Many types of power switching converter used to adapt primary energy sources to the requirements [5]. HB LEDs have been widely accepted because of superior longevity, low-maintenance requirements and improved luminance. For an LED load,a small variation in driving voltage leads to large variation in the LED current. LED current with large ripple will lead to seriously affect the reliability and longevity [6].On the other hand, a buck PFC converter and a buck-boost PFC converter have high efficiency owing to the simple structure and low output voltage in a LED driver[7]–[9]. These converters are usually operated in the discontinuous conduction mode (DCM) and critical conduction mode(CRM). Among them, CRM control is highly preferred becauseits turn-on switching loss and the diode reverse-recovery loss are almost eliminated. In addition, the input filter design is easier than the DCM operation [10]–[12]. Nevertheless, conduction loss of the diode still exists, and it decreases the power conversion efficiency. For this reason, a synchronous rectifier(SR) is proposed to be used instead of a diode. The synchronous rectification controller proposed in uses an auxiliary winding of the transformer for detecting voltage and current. In a Smart Rectifier control, IC and a dual-mode SR controller were used for driving the SR [13]-[15].

II.ANALYSIS OF PROPOSED CONVERTER

The circuit diagram of the proposed AC-DC converter is shown in Fig.1. The EMI input filter includes a filter inductor $L_f$and a filter capacitor C_f. The main structure of the proposed AC-DC converter is similar to that of a conventional buck-boost converter, which consists of an input capacitor C_{in}, an output capacitor C_o, a buck-boost inductor Lb, and a main switch S_m, the only difference being that the output diode is replaced with SR Sa. Diodes D_{sm} and D_{sa} are the intrinsic body diodes of S_m and S_a, respectively. Capacitors C_{sm} and C_{sa} denote the parasitic output capacitances of S_m and S_a, respectively. For the analysis of the proposed AC-DC converter in a steady state, several assumptions are made during one switching period Ts. All the semiconductor devices are ideal components except for the output capacitances C_{sm} and C_{sa} of S_m and S_a,respectively.

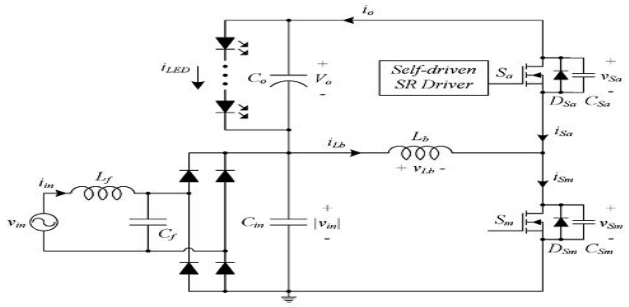

Fig.1. Proposed AC-DC converter with a self-driven synchronous rectifier.

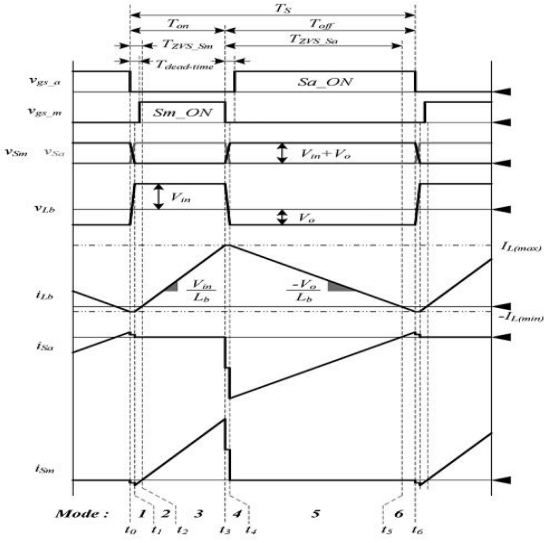

Fig. 2. Theoretical waveforms of proposed converter.

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The capacitance of the output capacitor, C_o, is large enough to consider the output voltage V_o as a constant. The rectified line voltage $|v_{in}|$ is considered as a constant value V_{in} during a switching period because the switching frequency f_{sw} is much higher than the line frequency f_L. The theoretical waveforms of the proposed converter in a switching period Ts are shown in Fig.2. The buck-boost inductor current i_{lb} varies from its maximum value $I_{L(max)}$ to its minimum value$I_{L(min)}$.

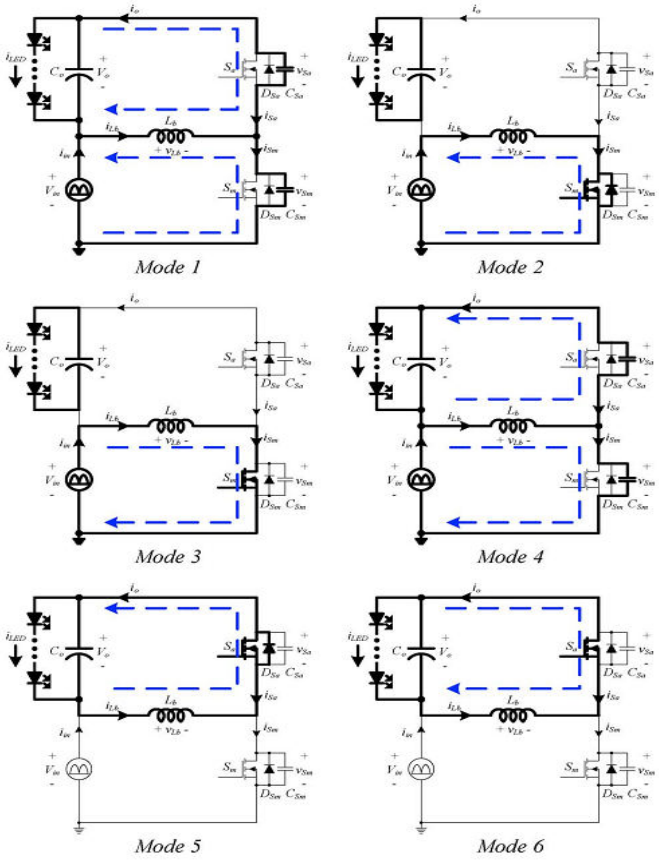

Fig.3. Operating modes of proposed converter.

The operation of the proposed converter in a switching period is divided into six modes as shown in Fig.3. Before t_o, the main switch $S_m$is turned off, and the synchronous switch $S_a$conducts. The inductor current i_{lb}decreases linearly and reaches its minimum value $-I_{L\ (min)}$ at t_o.

Mode 1 [t_0-t_1]: When switch $S_a$is turned off, this mode begins. The parasitic output capacitor C_{sa} begins charging and Csm begins discharging. By assuming that the capacitances of the parasitic output capacitors, $C_{sm}$and C_{sa}, are very small and the time interval between $t_0$and t_1 is very short, the inductor i_{Lb} current is regarded as a constant value $I_{L(min)}$. Voltages $V_{sm}$and V_{sa} vary linearly. The transition time interval T_{t1} is expressed as follows:

$$T_{t1} = (C_{Sm} + C_{Sa})\frac{V_{in} + V_o}{I_{L(min)}} \quad (1)$$

Mode 2 [t_1,t_2]: At t_1, capacitor $C_{sm}$is fully discharged, and voltage V_{sm}reaches zero when $D_{sm}$is turned on. ZVS operation of $S_m$is performed because the switch voltage V_{sm} is zero even before the gate pulse of Sm is applied. Furthermore, gate pulse $V_{gs_m}$is applied to the gate to turn switches$S_m$on. As the inductor voltage $V_{Lb}$is V_{in}, the inductor current i_{Lb}increases linearly as follows:

$$i_{Lb}(t) = -I_{L(min)} + \frac{V_{in}}{L_b}(t - t_1). \quad (2)$$

Mode 3 [t_2,t_3]: This mode begins when the inductor current i_{Lb}changes direction from negative to positive. Voltage V_{Lb} is equal to V_{in}, and current i_{Lb} increases linearly with the slope V_{in}/V_b. At the end of this mode, iLb current reaches its maximum value $I_{L(max)}$.

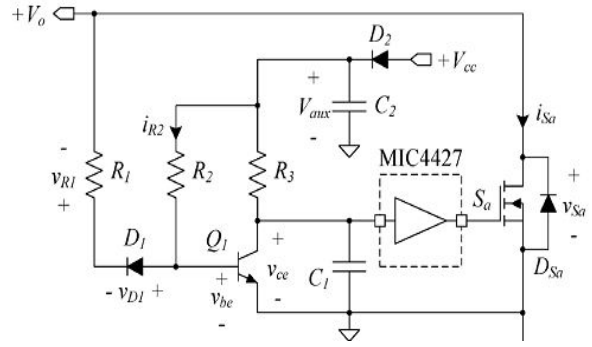

Fig.4. Proposed self-driven synchronous rectifier driver.

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$$I_{L(\max)} = -I_{L(\min)} + \frac{V_{\text{in}}}{L_b} T_{\text{on}}, \tag{3}$$

Where T_{on} is the time interval between t_1 and t_3. Time T_{t1} is very short; therefore, it is not considered.

Mode 4 [t_3,t_4]: When switch S_m is turned off, this mode begins. The parasitic output capacitor C_{sm} begins charging, and C_{sa} begins discharging. By assuming that the capacitances of the parasitic output capacitors, C_{sm} and C_{sa}, are very small and the time interval between t_3 and t_4 is very short, the inductor current i_{Lb} is regarded as a constant value $I_{L(max).}$ Voltages V_{sm} and V_{sa} vary linearly. The transition time interval T_{t2} is expressed as follows:

$$T_{t2} = (C_{\text{Sm}} + C_{\text{Sa}}) \frac{V_{\text{in}} + V_o}{I_{L(\max)}}. \tag{4}$$

Mode 5 [t_4,t_5]: At t4, capacitor C_{sa} is fully discharged, and voltage V_{sa} reaches zero when D_{sa} is turned on. ZVS operation of S_a is performed because the switch voltage V_{sa} is zero even before the gate pulse of Sa is applied. Furthermore, gate pulse V_{gs_a} is applied to the gate to turn switches S_a on. As the inductor voltage V_{Lb} is -Vo, the inductor current I_{Lb} decreases linearly as follows

$$i_{\text{Lb}}(t) = I_{L(\max)} - \frac{V_o}{L_b}(t - t_4) \tag{5}$$

Mode 6 [t_5,t_6]: This mode begins when the inductor current I_{Lb} changes direction from positive to negative. Voltage V_{Lb} is equal to $-V_o$, and current i_{Lb} decreases linearly with the slope of V_o/L_b. At the end of this mode, current i_{Lb} reaches its minimum value-$I_{L(min).}$ where T_{off} is the time interval between t_4 and t_6. Time T_{t2} is very short; therefore, it is not considered.

$$-I_{L(\min)} = I_{L(\max)} - \frac{V_o}{L_b} T_{\text{off}}, \tag{6}$$

III. ANALYSIS OF SELF-DRIVEN SR CIRCUIT

The circuit diagram of the proposed self-driven SR driver is shown in Fig.4. The SR driver is composed of three resistors: R_1, R_2 and R_3; diodes: D_1 and D_2; capacitors: C_1 and C_2; a transistor Q_1; and a MIC4427 MOSFET driver. The auxiliary control power is bootstrapped from the main control power $+V_{cc}$. Diode D_2 is used as a bootstrap diode. Diode D_1 is employed to detect the polarity of the switch voltage V_{sa}. Resistors and R_2 and R_3 transistor Q_1 are used to obtain high and low signals according to the polarity of V_{sa}. Furthermore, the collector emitter voltage V_{ce} is applied to MIC4427 for driving the SR.

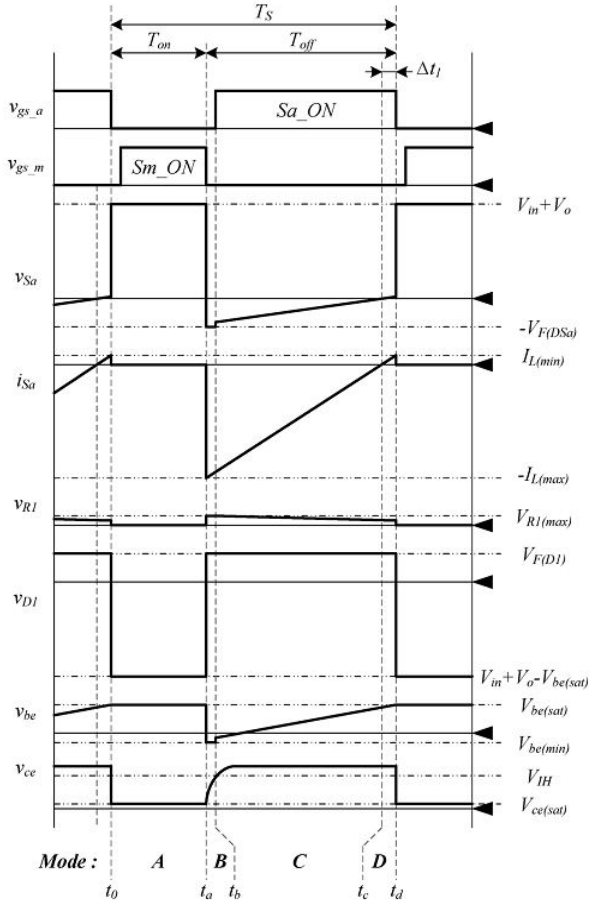

Fig.5. Theoretical waveforms of proposed SR driver.

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For generating the dead time in the proper ZVS operation of S_a, a small capacitance $C_1$is added to the SR driver. In addition, a small resistance R1 is added to compensate for the difference in the forward voltage drop $V_{F(D1)}$ and the base-emitter saturation voltage $V_{be(sat)}$. The basic operation of the SR driver is as follows. When voltage $V_{sa}$is negative, diode D_1conducts and the base-emitter voltage V_{be}becomes lower than $V_{be(sat)}$. Thus, the turn-on gate pulse from MIC4427 is applied to S_a. For the analysis of the proposed SR driver in a steady state, several assumptions are made during one switching period Ts. Capacitor $C_2$is large enough to consider the control power V_{aux}as a constant. Diode $D_1$is an ideal component. Transistor Q_1acts as a switching device, not as a signal amplifier. In addition, the base-emitter input capacitor and collect-emitter output capacitor are not considered. Switch $S_a$is an ideal component, except for the drain-source on-resistance $R_{DS(on)}$. The theoretical waveforms of the proposed SR driver in a switching period Ts are shown in Fig.5. All the operating modes of the proposed SR driver are shown in Fig.6. Before t_o, switch $S_a$is turned on, and diode D_1 conducts. The base-emitter voltage V_{be}increases linearly and reaches its base-emitter saturation voltage $V_{be(sat)}$ at t_0 .

Mode A [t_0,t_a]: When voltage V_{be}becomes $V_{be(sat)}$, transistor $Q_1$is saturated, and this mode begins. The corrector emitter voltage Vce is equal to its saturation voltage $V_{ce(sat)}$ because $Q_1$is in the saturation region, and switch S_a is turned off.

Mode B [t_a, t_b]: At t_a, the main switch $S_m$is turned off, and the inductor current flows through the body diode D_{sa}. In

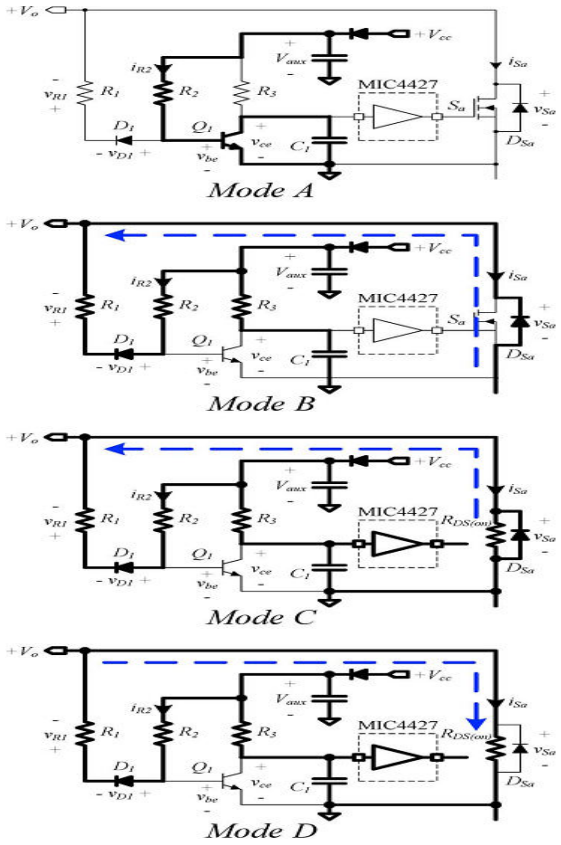

Fig.6. Operating modes of proposed SR driver.

This mode, the switch voltage Vsa is clamped as the forward voltage drop of the body diode-$V_{FD(sa)}$. In addition, diode D1 is turned on with the forward voltage drop $V_{F(D1)}$. The base emitter voltage Vbe and voltage $V_{R1}$are also constant as the minimum voltage $V_{be(min)}$ and the maximum voltage$V_{R1(max)}$, respectively, because $V_{sa}$and V_{D1} are constant.

$$V_{be(\min)} = V_{F(D1)} + V_{R1(\max)} - V_{F(DSa)}, \quad (7)$$

$$V_{R1(\max)} = R_1 \frac{V_{\text{aux}} - V_{be(\min)}}{R_2} \quad (8)$$

Transistor Q1 enters the breakdown region, because voltage V_{be} is lower than $V_{be(sat)}$, and the corrector-emitter voltage V_{ce} increases nonlinearly with the time constant of the RC circuit, which consists of V_{aux},R_3 and C_1.

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$$v_{ce}(t) = V_{aux}\left(1 - e^{-\frac{t}{R_3 C_1}}\right) \quad (9)$$

Mode C [t_b,t_c]: When the collect-emitter voltage Vce is higher than V_{IH}, which is the logic 1 input voltage of the MOSFET driver, gate pulse V_{gs_a} is applied to switch S_a. In this mode, switch $S_a$is expressed as a parallel circuit of $R_{DS(on)}$and D_{Sa} . base-emitter voltage $v_{be}(= v_{D1} + v_{R1} + v_{Sa})$ is expressed as follows

$$v_{be}(t) = V_{F(D1)} + R_1 \cdot i_{R2}(t - t_b) + R_{DS(on)} \cdot i_{Sa}(t - t_b). \quad (10)$$

Furthermore, currents $i_{R2}$and i_{Sa} are obtained as

$$i_{R2}(t) = \frac{V_{aux} - v_{be}(t - t_b)}{R_2}, \quad (11)$$

$$i_{Sa}(t) = -I_{L(max)} + \frac{V_o}{L_b}(t - t_b) \quad (12)$$

Mode D [t_c, t_d]: At, switch current changes direction from negative to positive. Switch conducts because the base emitter voltage is still lower than, and its current increases linearly until is equal to . Switch continuously conducts owing to the difference in the forward voltage drop and the base-emitter saturation voltage, and it is the key feature in the ZVS operation of the main switch. When the difference in and is equal to the sum of and, this mode ends, and switch is turned off. A small resistance is added to compensate for the difference in and because the drain-source on-resistance is constant according to the MOSFET, and it is related to the system efficiency. In this mode, voltage and current are similar to those mentioned in (10), (11), and (12). At the end of this mode, voltage and current are expressed as follows:

$$V_{be(sat)} = V_{F(D1)} + R_1 \cdot i_{R2}(t_d) + R_{DS(on)} \cdot i_{Sa}(t_d), \quad (13)$$

$$i_{R2}(t_d) = \frac{V_{aux} - V_{be(sat)}}{R_2}, \quad (14)$$

$$i_{Sa}(t_d) = \frac{V_o}{L_b}\Delta t_1, \quad (15)$$

Where is the time interval between and . By substituting (14) and (15) into (13), the time interval is expressed as

$$\Delta t_1 = \left(\frac{R_1 + R_2}{R_2}V_{be(sat)} - V_{F(D1)} - \frac{R_1}{R_2}V_{aux}\right) \times \frac{L_b}{V_o \cdot R_{DS(on)}}. \quad (16)$$

Therefore, the time interval, which is related to the ZVS operation, is easily controlled by adjusting resistance .In the proposed converter, the ZVS conditions for and are expressed as

$$T_{dead-time} < T_{ZVS\_Sm}, \quad (17)$$

$$T_{dead-time} < T_{ZVS\_Sa}, \quad (18)$$

Where is the dead time of switches and for a proper ZVS operation, and and are the times when each switch is reverse-biased and the reverse current flows through the intrinsic body diode of each switch. The gate pulse should be applied to each switch after voltage or has decreased to zero and before the current flowing though the intrinsic body diode changes its direction. Thus, the dead time should be considered. The ZVS operation of is always satisfactory because is sufficiently longer than. By assuming that the time interval between and

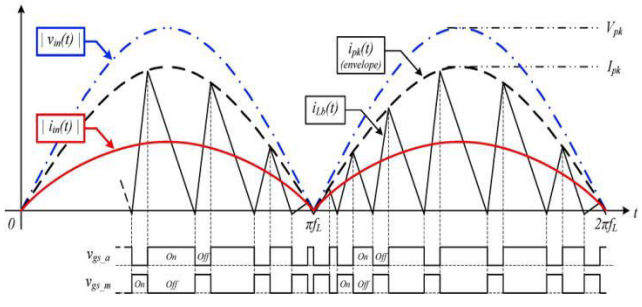

Fig.7. Theoretical Waveforms of Rectified Input Line Voltage, Input Current, and Inductor Current in a Line Period.

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IV.INDUCTION MOTOR

Induction Motor (IM) An induction motor is an example of asynchronous AC machine, which consists of a stator and a rotor. This motor is widely used because of its strong features and reasonable cost. A sinusoidal voltage is applied to the stator, in the induction motor, which results in an induced electromagnetic field. A current in the rotor is induced due to this field, which creates another field that tries to align with the stator field, causing the rotor to spin. A slip is created between these fields, when a load is applied to the motor. Compared to the synchronous speed, the rotor speed decreases, at higher slip values. The frequency of the stator voltage controls the synchronous speed [12]. The frequency of the voltage is applied to the stator through power electronic devices, which allows the control of the speed of the motor. The research is using techniques, which implement a constant voltage to frequency ratio. Finally, the torque begins to fall when the motor reaches the synchronous speed. Thus, induction motor synchronous speed is defined by following equation,

$$n_s = \frac{120f}{p}$$

Where f is the frequency of AC supply, n, is the speed of rotor; p is the number of poles per phase of the motor. By varying the frequency of control circuit through AC supply, the rotor speed will change.

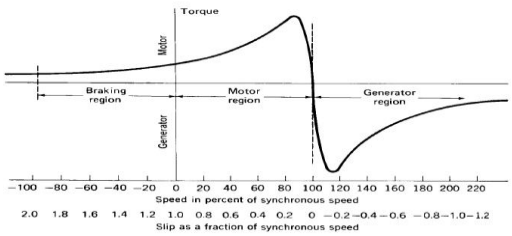

Fig.9.Speed torque characteristics of induction motor.

V.MATLAB/SIMULATION RESULTS

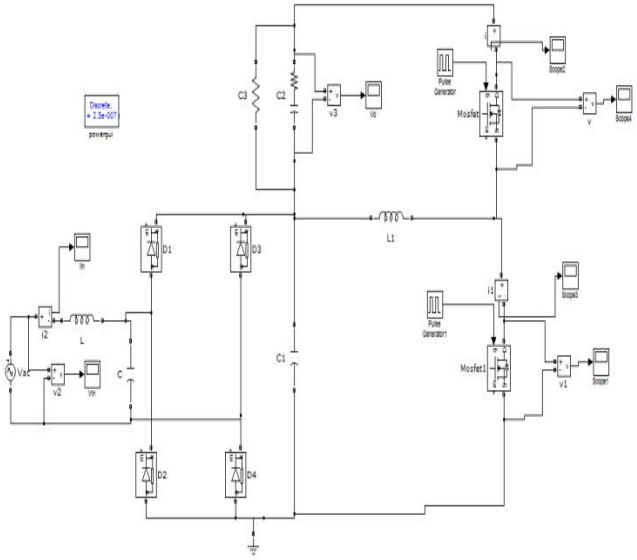

Fig.8.Matlab/Simulation Model of Proposed AC-DC Converter with a Self-Driven Synchronous Rectifier.

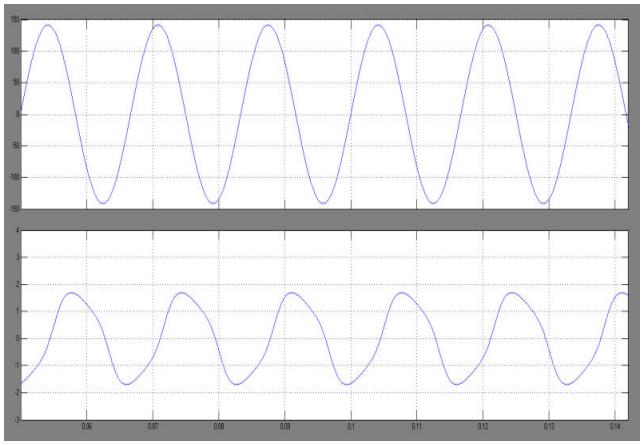

Fig.9.Simulation Waveforms At Vin=100,Input Voltage (Vin) And Current(Iin).

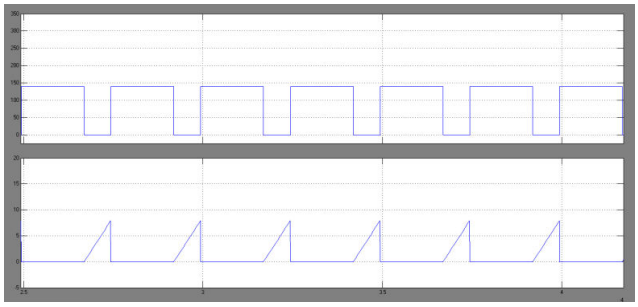

Fig.10.Switch Voltage (Vgsm) And Current(Igsm).

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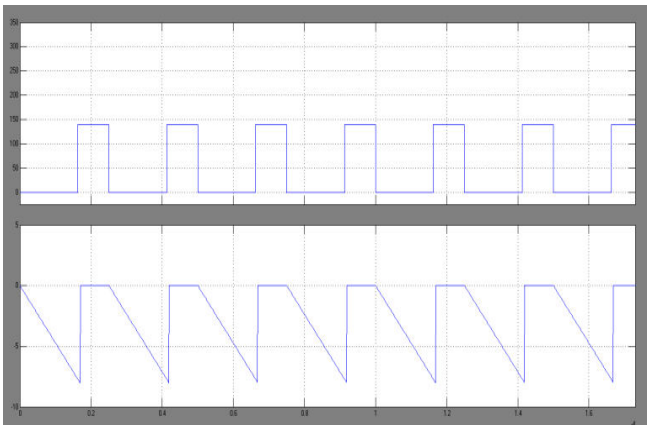

Fig.11.Switch Voltage (Vgs_a) and Current (Igsa).

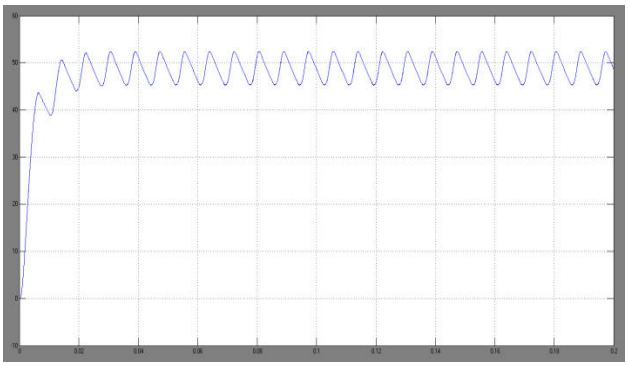

Fig.12.Output Voltage.

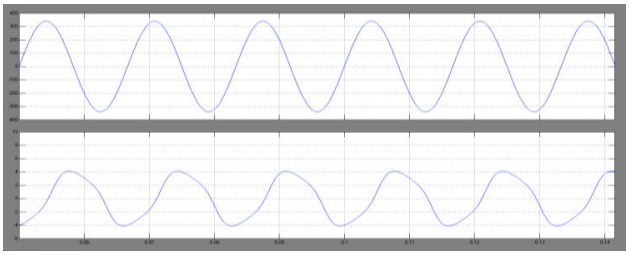

Fig.13.Simulation Waveforms at Vin=240, Input Voltage (Vin) and Current (Iin).

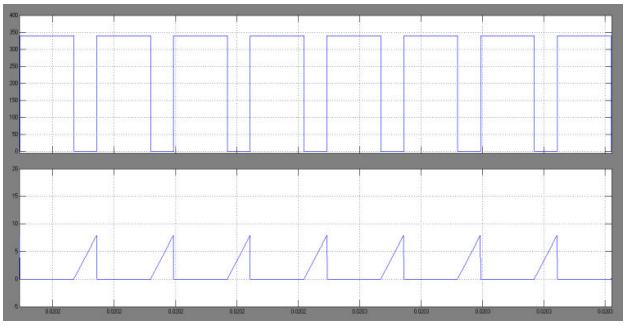

Fig.14.Switch Voltage (Vgsm) and Current(Igsm).

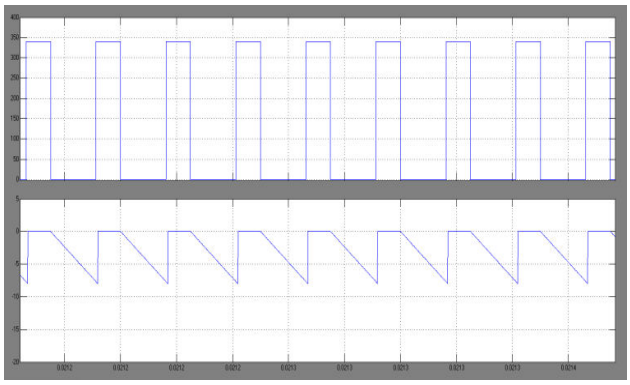

Fig.15.Switch Voltage (Vgs_a) and Current (Igsa).

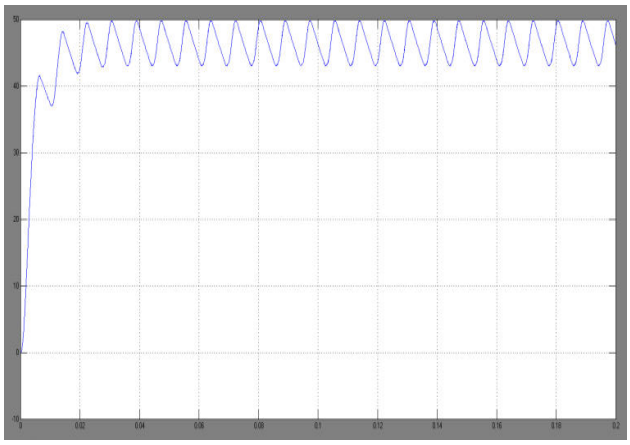

Fig.16.Output Voltage.

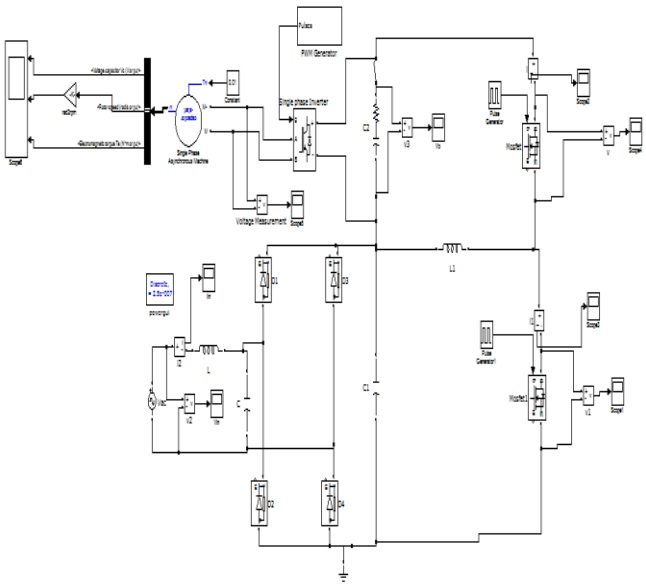

Fig.17. Matlab/Simulation Model of a Self-Driven Synchronous Rectifier with Induction motor drive.

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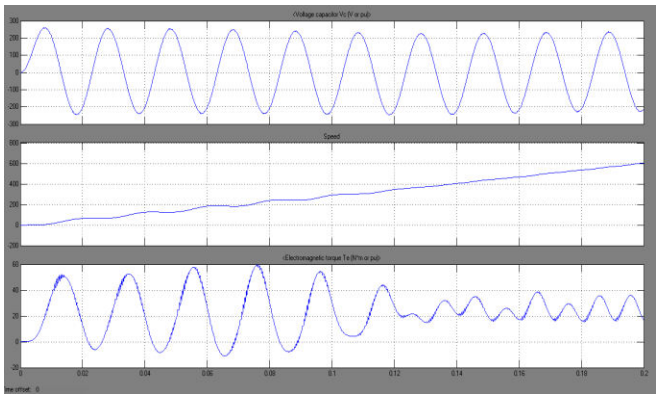

Fig.18.Capacitor voltage, torque and speed of Self-Driven Synchronous Rectifier with Induction motor drive.

VI.CONCLUSION

In this paper, a ZVS AC-DC LED driver using a self-driven SR has been proposed. In the proposed converter, ZVS operation of both and is performed. In addition, by using a self-driven SR driver, the conduction loss of the output rectifier is significantly reduced, and high efficiency is achieved. Moreover, the power factor is also improved by means of the time interval. The Proposed AC-DC Converter with a self-driven Synchronous Rectifier with DC Motor. DC motor application based on this paper we can performer the speed-torque characteristics.

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