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Paper Authors

GUJJARI UDAYASRI, JADAPALLI.SREEDHAR

Annamacharya Institute Of Technology & Sciences, Hyderabad, Telangana

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A NOVEL CONTROL METHOD FOR NESTED NEUTRAL POINT CLAMPED (NNPC) CONVERTER FOR MEDIUM-VOLTAGE

[1]GUJJARI UDAYASRI, [2]JADAPALLI.SREEDHAR

[1]M.tech Scholar Dept of EEE(Power Electronics), Annamacharya Institute of Technology & Sciences, Hyderabad,Telangana

[2]Associate professor & HOD, Dept of EEE, Annamacharya Institute of Technology & Sciences, Hyderabad,Telangana

[1]udayasri.g42@gmail.com,[2]sreedharmtech@gmail.com

ABSTRACT—In this paper, a new volt age source converter for medium voltage applications is presented which can operate over a wide range of voltages (2.4–7.2 kV) without the need for connecting the power semiconductor in series. The operation of t he proposed converter is studied and analyzed. In order to control t he proposed converter, a space-vector modulation (SVM) strategy with redun -dant switching states has been proposed. SVM usually has redun - dant switching state anyways. What is the main point we are trying to get to? These redundant switching states help to control the out - p utvoltage and balance voltages of the flying capacitors in the proposed converter. The performance of t he convert er under different operting conditions is investigated in MAT LAB/Simulink environment. The feasibility of the proposed converter is evaluated experiment ally on a 5-k VA p rot ot y p e.

Index Terms—DC–AC power conversion, multilevel converter, space vector modulation (SVM).

I. INTRODUCTION

MEDIUM-VOLTAGE high-power conversion applications such as motor drives, microgrids, and distributed generation systems use various converter topologies to achieve the desired voltage and performance [1]. Recent developments in semiconductor technology and commercial availability of high-power switches, such as the insulated gatebipolar transistor and the integrated gate commutated thyristor, haveresulted in a potential acceptance of the two-levelvoltage source converter (VSC) for high-power applications as well. However, for somemapplications, e.g., medium voltage drives, HVDC converters, and flexible alternating current transmission system controllers, the voltage ratings of power semiconductor devices are still insufficient to meet the required voltage levels by one singlemodule of a two-level VSC. Multilevel VSC configurations are the preferred option to meet the desired high voltage and power levels. The main features of these configurations, as compared with the two-level VSC, are their capabilities to reduce:

1) har- monic distortion of the ac-side waveforms; 2)*dv/dt* switching stresses; 3) switching losses; and

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4) minimize or even eliminate the interface transformer [1]–[5].

The multilevel VSC topologies can be categorized into twogroups: classic multilevel topologies and advanced multilevel topologies. The classic multileveltopologies include theneutralpoint clamped (NPC), flying capacitor (FC), and the cascaded H-bridge (CHB). [1]. The classic multilevel converters have been commercialized successfully by major manufacturers; however, they have some drawbacks which limit their applications. For instance, the NPC structure with higher number of levels is less attractive because of its limitations which include:

1) higher losses and uneven distribution of losses in the outer and inner devices,

2) dc-link capacitor voltage balance becomes unattainable in higher level topologies with a passive front end when using conventional modulation strategies

3) the number of clamping diodes increases substantially with the voltage level. The FC structure needs to have higher switching frequencies to keep the capacitors properly balanced, whether a selfbalancing or a control-assisted balancing modulation method is used (e.g., greater than 1200 Hz). Also, the number of FCs increases with the voltage level. The CHB structure can reach higher voltage and higher power level with the modular structure; however, this topology needs: a large number of isolated dc sources, an expensive and bulky phase-shiftingtransformer, and a substantially higher number of active devices to achieve a regenerative option. A number of variants and new multilevel converters have been proposed in the literature [6]–[16]. These are variations or hybrids of the three classic multilevel topologies and are called advanced multilevel topologies. Among recent proposals, the following topologies have found practical application, which are commercialized by manufacturers:

the five-level H-bridge\ NPC (5 L-HNPC), the three-level active NPC (3 L-ANPC), the five-level active NPC (5 L-ANPC), and the four-level hybridclamped converter (4 L-HC). The main features of these converters are:

1) A 5L-HNPC is the H-bridge connection of two classic 3L-NPC phase legs which makes a five-level converter[6]–[9]. This topology can reach higher levels and higher output voltages; however, like an H-bridge topology, it requires isolated dc sources with the phase shifting

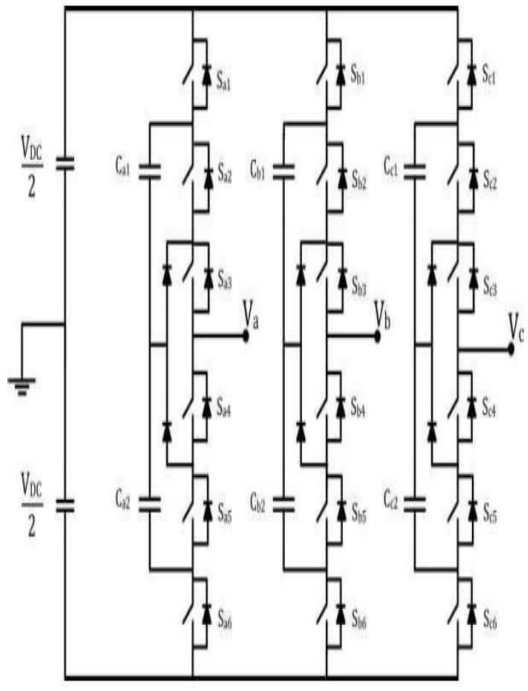

Fig. 1. Proposed NNPC converter.

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transformer which increases the cost and complexity of the converter.

2) A 3L-ANPC is an improved three-level NPC where the neutral clamping diodes are replaced with clamping switches to provide a controllable path for the neutral current, and hence, control the loss distribution among the switches of the converter [10], [11]. This topology distributes the losses between the inner and outer switching devices in each converter leg and thus improves the cooling system design and increases the maximum power ratio of the converter. However, although higher number of the devices as compared to the three-level NPC, the same number of output voltage levels is achieved. This decreases the reliability and increases the cost and complexity of the overall converter.

3) A 5L-ANPC is a combination of a 3L-ANPC and 3L-FC, which increases the number of voltage levels [12]–[15]. This converter can reach higher output levels without the need to add series-connected diodes. Moreover, the problem of capacitor voltage balancing when using passive front ends is avoided. This converter, however, is complex as it needs to control the FC voltages and their initialization, aside from the NPC dc-link capacitors voltage unbalance control. Another drawback of the 5L-ANPC is that the switch voltage ratings are different in different converter branches (in fact two devices may have to be connected in series for the top and bottom switches). In other words, the voltage stresses of the switches for a 5LANPC are different, the outer switches are subjected to half of the dc-link voltage but the inner devices have just 1/4 of the dc-linkvoltage.

TABLE I
NUMBER OF ELEMENTS IN DIFFERENT TOPOLOGIES AND THE PROPOSED TOPOLOGY

Topology	Number of Switches	Number of Diodes	Number of Flying Capacitors	DC Sources
4-L NPC	18	18	-	1
4-L FC	18	-	9	1
NNPC Topology	18	6	6	1

4) A 4L-HC converter is an improved ANPC converter that makes four levels at the outputvoltage [16]. This converter can reach four levels without the needfor series-connected power switches and all the switches have the same voltage stress. In comparison to the classic multilevel topologies, although the 4L-HC converter has less number of passive components, it does need two more powerswitches in each phase which could have a negative impact on the cost and control complexity of theconverter. In this paper, a new multilevel topology, shown in Fig. 1, is presented for medium-voltage high-power application. The proposed converter has the following features:

1) It can operate over a wide voltage range of 2.4–7.2 kV without the need for connecting the power semiconductor in series.

2) It has four levels at the output voltage and unlike aforementioned converters, all switches have the same voltage stress (equal to one-third of the dcvoltage).

3) Compared to the classic four-leveltopologies, as shown in Table I, it has fewer number of components and complexity. In comparison to the four-level

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NPC, the number of diodes has been reduced significantly and in comparison

TABLE II
SWITCHING STATES OF THE FOUR-LEVEL NNPC AND CONTRIBUTION OF THE AC-SIDE CURRENTS TO THE FC VOLTAGES

S_{X1}	S_{X2}	S_{X3}	S_{X4}	S_{X5}	S_{X6}	V_{Cx1}	V_{Cx2}	V_{ax}
1	1	1	0	0	0	No Impact	No Impact	$\frac{V_{DC}}{2}$
1	0	1	1	0	0	Charging (ix > 0) Discharging (ix < 0)	No Impact	$\frac{V_{DC}}{6}$
0	1	1	0	0	1	Discharging (ix > 0) Charging (ix < 0)	Discharging (ix > 0) Charging (ix< 0)	
1	0	0	1	1	0	Charging (ix >0) Discharging (ix < 0)	Charging (ix > 0) Discharging (ix < 0)	$-\frac{V_{DC}}{6}$
0	0	1	1	0	1	No Impact	Discharging (ix > 0) Charging (ix< 0)	
0	0	0	1	1	1	No Impact	No Impact	$-\frac{V_{DC}}{2}$

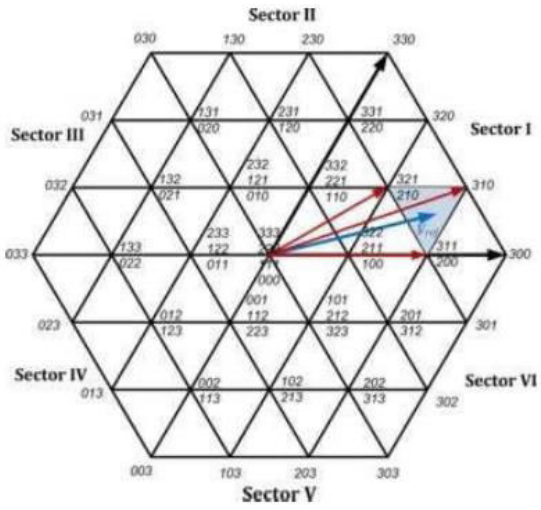

Fig. 2. Space-vectordiagram ofa four-level converter.

to the four-level FC it has fewer capacitors. In comparison to a 4L-HC converter, it has less number of power switches. Also, unlike CHB converters, it does not need to have a transformer for isolated dc sources. The proposed multilevel converter is studied and analyzed, and a space-vector modulation (SVM) strategy has been developed to control and balance the capacitor voltages.

The performance of the converter under different operating conditions is investigated in MATLAB/Simulink environment. A 5-Kva laboratory prototype has been built and results are presented.

II. CONVERTERTOPOLOGY

A. Operation ofthe Proposed Converter

The proposed multilevel topology, as shown in Fig. 1, is a combination of an FC topology and a NPC topology named nested neutral point-clamped (NNPC) converter which provides a four-level output voltage. To ensure equally spaced steps in the output voltages, the capacitor Cx1 and Cx2 , x = *a,b,c* are charged to one-third of the total dc-link voltage. The proposed topology in comparison to the classic four-level topologies, as shown in Table I, has a fewer number of components and hence
is less complex to control.

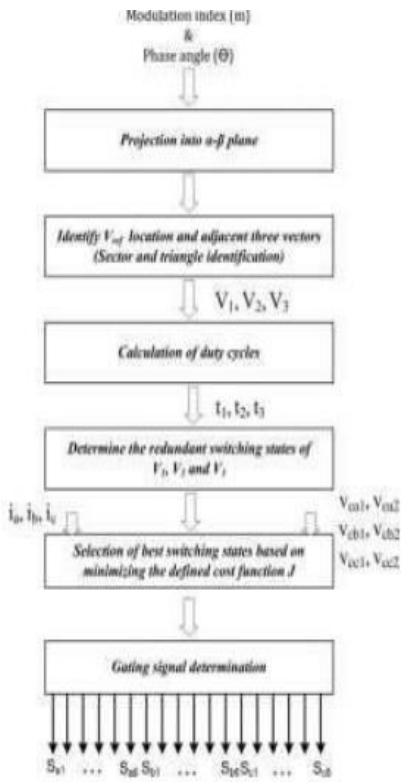

Fig. 3. Block diagram for the implementation of the developed SVM-based strategy.

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TABLE III
PARAMETERS OF THE SYSTEM (SIMULATION STUDIES)

Converter Parameters	Values	Values (p.u)
Converter Rating	5 MVA	1.0
Output Voltage	7.2 kV	1.0
Flying Capacitors	1000 μF	4.0
Input DC Voltage	11.8 kV	-
Output Frequency	60 Hz	1.0
Output Inductance	5.5mH	0.2
Output Load	10.5 Ω	1.0

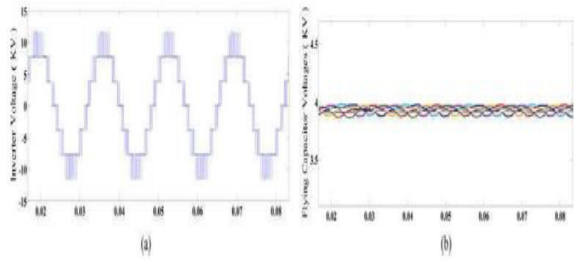

Fig. 4. Simulation waveforms: (a) invertervoltage and (b) voltages of FCs (m = 0.95, PF = 0.9)

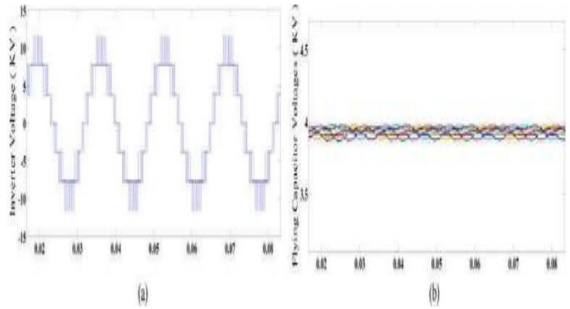

Fig. 5. Simulation waveforms: (a) invertervoltage and (b) voltages of FCs (m = 0.9, PF = 0.7).

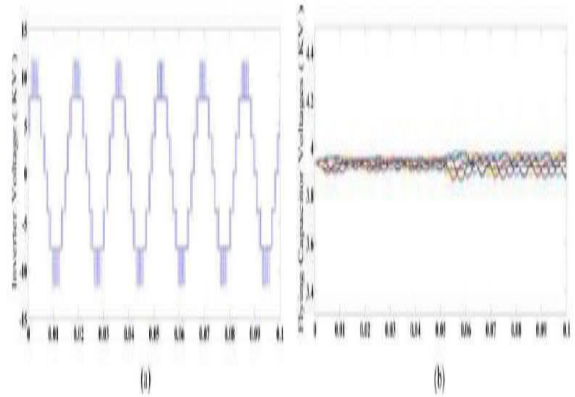

Fig. 6. Simulation waveforms: (a) inverteroutput voltage and (b) voltages of FCs (step change from half-load to full load).

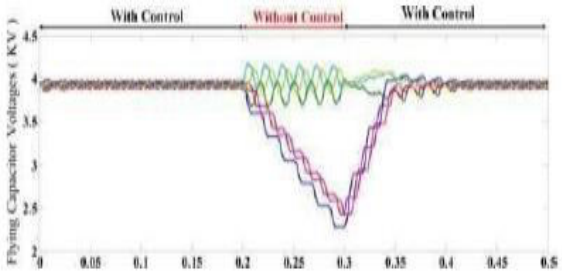

Fig. 7. Simulation waveforms; voltage of FCs with and without an SVM controller

Four output levels are achieved from six distinct switching combinations. The list of switching combinations is shown in Table II. It should be noted that all switch devices are rated to one-third of the dc-link voltage. Another advantage of the proposed converter is the redundancy in switch combination to produce output levels. For example, there are two redundant switching states (as can be seen in Table II) to generatevoltage levels of 1/6Vdc and −1/6Vdc . Each redundant state provides a specific charging and discharging current path for each floating capacitor. This is a specific feature of redundant switching states that can be used to achieve voltage balancing of the capacitors

TABLE IV
PARAMETERS OF THE SYSTEM (EXPERIMENTAL STUDIES)

Converter Parameters	Values
Converter Rating	5 kVA
Flying Capacitors	1000 μF
Input DC Voltage	300 V
Output Frequency	60 Hz
Output Inductor	5 mH
Output Load	10 Ω

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The main technical challenge is to identify the best redundant switching state to achieve this.

B. SVM for the Proposed NNPC Converter

The NNPC converter is a combination of a FC topology with NPC topology, which provides four level at the output voltage. The capacitor $Cx1$ and $Cx2$, $x = a, b, c$ are charged to one third of the total dc-link voltage to ensure equally spaced steps in the output voltages. The NNPC converter in compare to the classic four-level topologies has less number of components and complexity. In compare to a four-level NPC converter, the number of diodes has been reduced from 18 to 6. In compare to a four-level FC converter, the number of FCs has been reduced from 9 to 6. Also, unlike the CHB converter, the NNPC converter does not need to have any isolated dc sources or phase-shifting transformers. The list of switching combinations is shown in Table I. Four different output levels are achieved from six distinct switching combinations. The NNPC converter can take the advantage of redundancy in switching states to regulate the voltages of the FCs. For generating medium-voltage level $1/6V$dc and $-1/6V$dc, there are two redundant switching states. Each redundant state provides a specific charging and discharging current path for each floating capacitor. This is a specific feature of redundant switching states that can be applied to achieve voltage balancing of the FCs. The main technical challenge is to identify the best switching state.

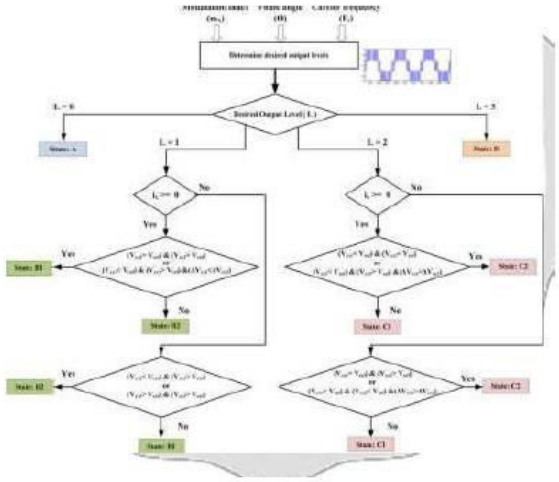

Fig8 : Procedure of the proposed SPWM approach for phase x ($x = a,b,c$).

The SVM technique can be applied to the converter to control the output voltage and keep the capacitor voltages balanced and constant [16]. The space vector diagram of a four-level converter on the $\alpha - \beta$ plane is a hexagon centered at the origin of the plane, as shown in Fig. 8

$$\begin{aligned} &\vec{V}_1 t_1 + \vec{V}_2 t_2 + \vec{V}_3 t_3 = \vec{V}_{\text{ref}} T_s \\ &t_1 + t_2 + t_3 = T_s \\ &\vec{V}_{\text{ref}} = \left|\vec{V}_{\text{ref}}\right| e^{j\theta}, \quad \theta = < \vec{V}_{\text{ref}} \end{aligned} \tag{1}$$

where Ts is the switching period, _V1 ,_V2 , and _V3 are the three switching vectors adjacent to Vref and t1, t2 , and t3 are the calculated on-duration time intervals of the switching vectors,
respectively. A cost function, J, can be defined based on the energy stored in the capacitors as follows:

$$\begin{aligned} J &= J_a + J_b + J_c \\ &= \sum_x \sum_{i=1}^{2} \frac{1}{2} C_{cxi} \left(V_{C_{cxi}} - V_{\text{Dc}}/3\right)^2 \\ x &= a, b, c. \end{aligned} \tag{2}$$

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SVM technique has been applied to the proposed converter to control the output voltage and to keep the capacitor voltages balanced and constant. As described in Table II, there are six distinct switching states for each phase of the proposed fourlevel converter of Fig. 1 The space-vector diagram of a fourlevel on the plane is a hexagon centered at the origin of the plane, as shown in Fig. 2. The reference vector is synthesized

3.1 NEW AND SIMPLE SINGLE-PHASE MODULATOR FOR THE NNPC CONVERTER

The proposed single-phase modulator is based on an SVPWM technique, which is described in Section I. This technique uses threelevel- shifted triangular carriers, all having the same frequency and the same amplitude. The in- phase disposition method, where all carriers are in phase, has been employed for the four-level NNPC converter as shown in Fig. 4. Comparing carriers and modulation signal, the desired output levels can be obtained, as shown in Fig. 5. Based on the desired level at the output, the corresponding switching
state can be selected from Table I, and then, applied to the power switches. Table I also shows that there are redundancy states for two middle levels (level 1 and 2). The redundancy states based on the direction of the output current can charge or discharge the FCs. Therefore, after determining the desired output level (by comparing
carriers and modulation signal), the direction of the phase current should be measured, and then, the controller will decide which states should be chosen to apply to the converter to control and balance the voltages of capacitors. The selected switching state can charge or discharge the FCs to minimize the difference between the nominal voltage values and the measured voltage values. The diagram shown in Fig. 6 shows the procedure of the proposed SPWM approach. As can be seen from Fig. 5, this procedure is very simple and easy to implement in hardware in compare to the huge amount of calculations for the SVM technique. In the proposed approach, the amount of calculation is independent from the modulation index. The main feature of the proposed SPWM technique is that it can be applied to each leg separately to control the FCs of that leg and at the same time, generate output waveforms. In different phases, just the modulating signals have ±120° phase shift respect to each other

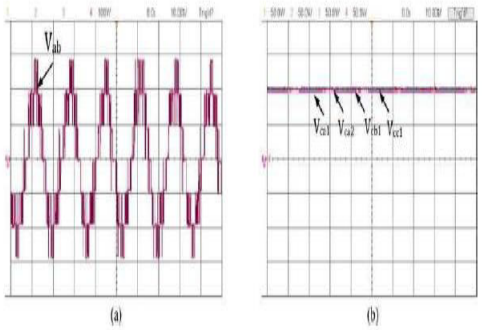

Fig. 9. Experimental results, steady state: (a) inverteroutput line voltage and (b) voltages of FCs, m = 0.95, PF = 0.9.

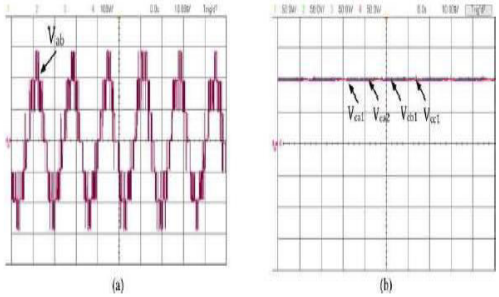

Fig. 10. Experimental results, steady state: (a) inverter output linevoltage and (b) voltages of FCs, m = 0.9, PF = 0.7.

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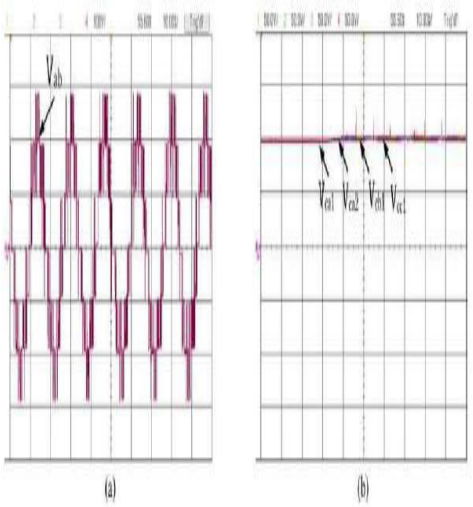

Fig. 11. Experimental results, transient state: (a) inverter output line voltage and (b) voltages of FCs, step change from half-load to full load.

by the three adjacent switching vectors [5], [17] and the can be described as

$$\dot{V}_1 t_1 + \dot{V}_2 t_2 + \dot{V}_3 t_3 = \dot{V}_{ref} T_s$$
$$t_1 + t_2 + t_3 = T_s$$
$$\dot{V}_{ref} = V_{ref} \angle \theta \quad (1)$$

where Ts is the switching period, V1 , V2 , and V3 are the three switching vectors adjacent to Vref and t1 , t2 , and t3 are the calculated on-duration time intervals of the switching vectors, respectively [18].The procedure of the SVM strategy can be summarized in Fig. 3 [18]. In order to achieve voltage balancing for the capacitor, the best switching states should be selected among the available redundant switching state to minimize the voltage deviation of the capacitors. Therefore, a cost function, J , can be defined based on the energy stored in the capacitors as follows:

$$J = J_a + J_b + J_c$$
$$J_x = \frac{1}{2} C_{cxi} \left(V_{Ccxi} - \frac{V_{dc}}{3} \right)^2$$
$$x = a, b, c. \quad (2)$$

To minimize the cost function J, the following condition should be satisfied:

$$\frac{dJ_x}{dt} = \sum_{i=1}^{2} C_{cxi} \left(V_{Ccxi} - \frac{V_{dc}}{3} \right) \frac{dV_{Ccxi}}{dt} \leq 0$$
$$x = a, b, c \quad (3)$$

where

$$i_{Ccxi} = C_{cxi} \frac{dV_{Ccxi}}{dt}$$
$$x = a, b, c \quad (4)$$

and i_{Ccxi} is the current of the capacitor $C_{cxi}, x = a, b, c, i = 1, 2$. Equation (3) can be rewritten as

$$\sum_{i=1}^{2} \left(V_{Ccxi} - \frac{V_{dc}}{3} \right) i_{Ccxi} \leq 0, \quad x = a, b, c. \quad (5)$$

The best switching states should be found to minimize (5). If an averaging operator is applied to (5) over a one sampling period

$$\frac{1}{T_s} \int_{kT_s}^{(k+1)T_s} \sum_{i=1}^{2} \left(V_{Ccxi} - \frac{V_{dc}}{3} \right) i_{Ccxi} \leq 0, \quad x = a, b, c. \quad (6)$$

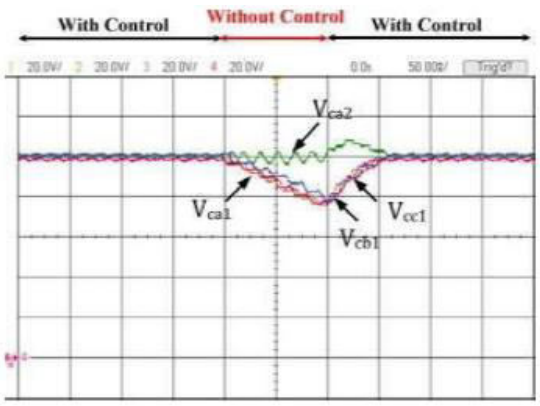

Fig. 12. Experimental results, the effectiveness of the SVM controller to control voltages of the FCs.

where , ¯ iC cxi is the avera g e value of the Ccx i capac it o r curren t. This current can be calculated based on the switching states and their relationship to ac-side currents ia , ib , and ic , as can be seenin Table-II

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III. SIMULATION RESULTS

In order to showthe performance of the proposed NNPC four-level converter, simulation studies have been done in MATLAB/Simulink environment for a 5-MVA/7.2-kV inverter. The parameters of the system are shown in Table III. The simulation also demonstrates the effectiveness of the developedSVM to generate output voltages, and to regulate and balance the voltage of FCs.The performance of the proposed NNPC converter and SVM controller has been studied during both the steady-state and transient-state.

A. Steady-State Analysis

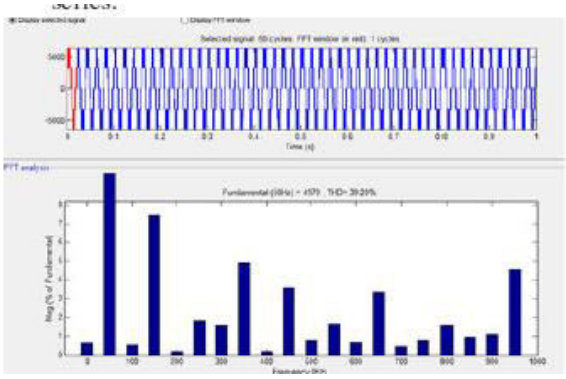
Figs. 4 and 5 show the performance of the proposed converter using SVM technique with different load power factors. Fig. 4 shows the inverter output voltage, output currents, and FC voltages, where modulation index m = 0.95 and load PF is 0.9. Fig. 5 also shows the inverter output voltage, output currents, and FC voltages, where modulation index m = 0.9 and load If the capacitor voltages is assumed to be constant over one Ts , then

$$\sum_{i=1}^{2} V_{Ccxi} - \frac{V_{dc}}{3} \Big|_{kT_s}^{(k+1)T_s} i_{Ccxi} \le 0,\ x = a,\ b,\ c \quad (7)$$

and consequently

$$\sum_{i=1}^{2} V_{Ccxi} - \frac{V_{dc}}{3} \le 0,\ x = a,\ b,\ c \quad (8)$$

the proposed converter which can workwith a wide range of voltages (2.4–7.2 kV) without the need for connecting the power semiconductor in series.

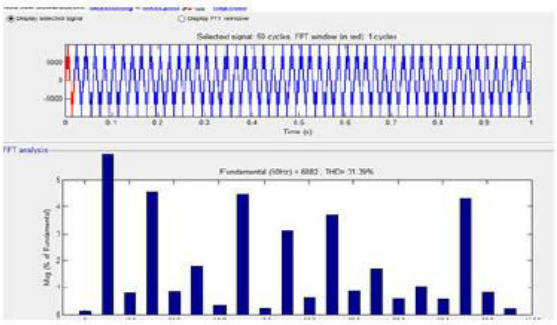


Transient-State Analysis

In this case, step change from half-load to full load (m = 0.95, PF = 0.95) is considered as indicated in Fig. 6. As observed from Fig. 6, voltages of FCs are maintained at the nominal values.

B. Evaluation of the ControlPerformance

In order to show the performance of the controller, this simu- lation study has been done. In this case, assume that the NNPC converter is operating under normal condition and suddenly at t = 0.15 s, the SVM controller has been deactivated and at t = 0.3 s, the SVM controller reactivated again. As can be seen from Fig. 7, when the controller is deactivated, the volt- age of capacitors diverges and when the controller reactivates the capacitor voltages start converging. This study shows the performance of the SVM controller.



CONCLUSION

This paper introduces a new four-level VSC for mediumvoltage applications called NNPC. The proposed topology can operate over a wide range of 2.4–7.2 kVwithout any power semiconductor in series. The proposed converter has fewer components as compared with classic multilevelconverters. Moreover, the voltage across the power semiconductors is only one-third of the dc link (and equal for all semiconductors). An SVM strategy which benefits fromthe switching state redundancy has been used to controlthe output voltage and stabilize voltages of the FCs. The feasibility of the proposed converter is evaluated experimentally and results are presented.

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