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EFFICIENT DESIGN OF TESTABLE REVERSIBLE CIRCUITS USING VERILOG HDL

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Abstract: This article includes the design of testable sequential circuits by two vectors using conservative-logic. The proposed sequential circuits based on conservative logic and its design makes reliable to the traditional sequential circuits built using classical gates in terms of testability. Any of the sequential circuit among all based on conservative logic can test for stuck-at-0 fault and stuck-at-1 fault by using two vectors i.e., 0 and 1. The design of testable Master-slave D flip-flop, Double Edge triggered flip flop (DET) flip-flop using two vectors 0 and 1 are discussed here. The importance of the proposed work is that we are designing sequential circuits suitable for testing by using reversible circuits which makes design efficient. Hence here both conservative logic and reversible logic is presented. In the proposed work, we are presenting a design of reversible sequential circuit using Fredkin gate. Fredkin gate is one of the reversible gates and this one is the only reversible gate which supports both conservative and reversible logic and also having special advantage of less quantum delay.

Index terms: Reversible gate, fredking gate, faults

I.INTRODUCTION

Conservative logic is a logic family that shows the property of a logic circuit where we can observe the equal numbers of 1's in the output as there as the input. Conservative logic is not only a normal one but also a reversible in nature. Mainly in the sector of performance we can go for it because of its power dissipation i.e., theoretically zero. It makes design more effective in terms of performance. Reversibility is the asset which displays one-to-one mapping linking input and output vectors; thus the input vectors always be recreated from the vector of output states. Reversible logic does not permit fanout to arise, it means for each and every input corresponding output is created. Therefore for 1 input, multiple outputs are not possible; this is severely controlled by reversible logic which outcomes testing to be effortless. Conservative logic is also called reversible conservative logic when there is one-toone mapping between input and output vectors in addition with the property that there are equal numbers of 1's in the outputs as in the inputs. If a circuit is designed in an irreversible manner then there will be a bit of information lost and which results in heat dissipation. The line of approach offered by conservative logic avoids a number of dead ends that are found in conventional models and opens up bright views.Based on the landauer principle one bit of information lost would be equal KTln2 joules of energy lost, where K is the Boltzmann constant and T is the temperature. So to reduce this energy lost completely we use reversible logic. And also reversible logic entirely diminishes heat dissipation. Reversible logic has received great awareness in the recent years due to

their ability to diminish the power of dissipation which is the main prerequisite in low power VLSI design. Reversible logic takes care of Fan-out crisis. It supports the process of running the entire system in both ways of forward and backward.The proposed method will take care of the fan-out (FO) at the end of our system i.e., output of the reversible latches and can also interrupts the feedback to make them suitable for testing by only two test vectors i.e., all 0s and all 1s. By this way we can easily test the circuit with ease. In other words when circuit is executed in normal mode, feedback will be present because to compensate for the extra inputs. And similarly when executed in test mode its feedback is disrupted and the circuit is tested for stuck-at-faults. So proposed technique is divided in to two modes normal and test mode. Fan-out leads to increased capacitive load on the driving gate, and therefore longer delay. So the fan-out problem is taken care by the proposed technique. The proposed technique is extended toward the design of two vectors testable master-slave flipflops and double edge triggered (DET) flip-flops. Reversibility in computing implies that no information about the computational states can ever be lost, so we can recover any past stage by computing backwards or will not computing the results. This is termed as logical reversibility. The advantages of logical reversibility can be gained only after employing physical reversibility. It is a process that dissipates no energy to heat. Absolutely perfect physical reversibility is practically not possible. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments, that is not only the outputs can be uniquely determined from the inputs, but also the inputs can be regained from the outputs. In this paper we will be discussing in section-II about the different reversible logic gates and a detailed explanation of Fredkin gate which is common to both conservative and reversible logic.

II.REVERSIBLE LOGIC GATES

[1] The number of Reversible gates (N): The number of reversible gates used in circuit. [2] The number of constant inputs (CI): This refers to the number of inputs that are to be preserved constant at either 0 or1 in order to produce the given logical function. [3] The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. Also the garbage outputs as these are very essential to achieve reversibility. [4] Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. There are different reversible gates and they are: • Not gate • Feynman gate (CNOT) • Fredkin gate (CSWAP) • Toffoli gate • Peres gate • Sayem gate • Double Feynman gate In this Toffoli gate and Fredkin gate are universal gates. Universal gates means using these gates any type of Boolean expression can be obtained (i.e.) any type of circuits can be designed. Not gate is the basic reversible gate. Feynman gate is a 2*2 one through reversible gate. The input vector is I (A, B) and the output vector is O (P, Q). The outputs are defined by P=A, Q = A B. Toffoli gate is a 3*3 gate, the input & output

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vector is I (A, B,C), O(P,Q,R). The outputs are defined by P=A,Q=B, R=AB C. NOT gate is an inverter which inverts the input. Likewise other gates are known. In this we select Fredkin gate mainly because it is compatible with both reversible and conservative logic.Fredkin gate is a 3*3 gate shown in Fig 1. The input vector is I (A, B, C) and the output vector is O(P, Q, R). The output is defined by P=A, Q=A′B AC and R=A′C AB. Quantum cost of a Fredkin gate is5. It is used for designing sequential circuits because it is the only common gate that can be used in conservative, switch, nteraction and reversible logic. Due to its unique characteristics and properties Fredkin gate is used for designing sequential circuit and also it reduces delay and area used for designingcircuit.

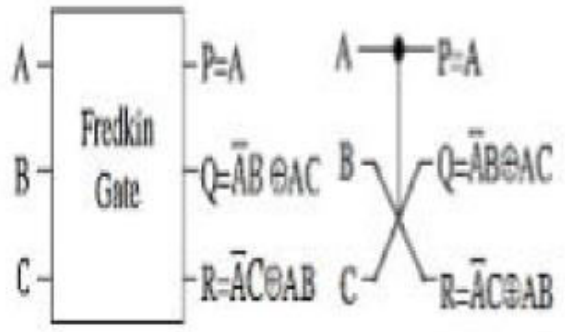

Fig: Fredkin gate

It is reversible and Conservative in nature i.e., it has unique input and output mapping and also has the same number of 1's in the outputs as in the inputs. Fredkin gate has three inputs, depending on the first input which is a control signal outputs are produced. If the first input is 1 means then the other two inputs are regained as outputs. If the input is 0 then the other two inputs are swapped and producedas outputs.

III.PROPOSED DESIGN

1) DESIGN OF TESTABLE REVERSIBLE LATCH:

The characteristic equation of the D latch can be written as Q+ = D · E + .E · Q. In the proposed work, enable (E) refers to the clock and is used conversely in place of clock. When the enable signal (clock) is 1, the value of the input D is reflected at the output that is Q+ = D. While, when E = 0 the latch preserves its previous state, that is Q+ = Q. In Fig. 2(a) reversible D latch is shown and its characteristic equation is reverse of D latch characteristic equation but that design cannot be tested only by two vectors because of feedback. Some other interruptions may occur. So, in our proposed work we will cascade two Fredkin gate and Q output of one gate will follow the other. And it has two control signals C1 and C2 by which the design works. In normal mode which is shown in Fig. 2(b) works when C1 and C2 is given as 0 and 1 and the circuit works as a D latch without any fan-out problem. In test mode which is shown in Fig. 2(c) and (d) works when C1 and C2 is given as 1 and 1 or 0 and 0, the circuit disrupts the feedback and checks for stuck-at-0 or stuck-at-1 fault.

2) DESIGN OF TESTABLE NEGATIVE ENABLE D LATCH

A negative enable reversible D latch will pass the input D to the output Q when E = 0; otherwise preserves the previous state. The characteristic equation of the negative enable D latch is Q+ = D·E +E·Q.This characteristic equation of the negative enable reversible D latch can be mapped on the second output of the Fredkin gate. The

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next Fredkin gate in the design take cares of the FO. This Fredkin gate in the design also helps in making the design testable by two test vectors, all 0's and all 1's, by breaking the feedback based on control signals C1 and C2 as illustrated above for positive enable D latch. The negative enable D latch is helpful in the design of testable reversible master-slave flip flops. This is because as it can work as a slave latch in the testable reversible master-slave flip-flops in which no clock inversion is required.This characteristic equation of the negative enable reversible D latch can be mapped on the second output of the Fredkin gate. The next Fredkin gate in the design take cares of the FO. This Fredkin gate in the design also helps in making the design testable by two test vectors, all 0's and all 1's, by breaking the feedback based on control signals C1 and C2 as illustrated above for positive enable D latch. The negative enable D latch is helpful in the design of testable reversible masterslave flip flops. This is because as it can work as a slave latch in the testable reversible master-slave flip-flops in which no clock inversion is required.

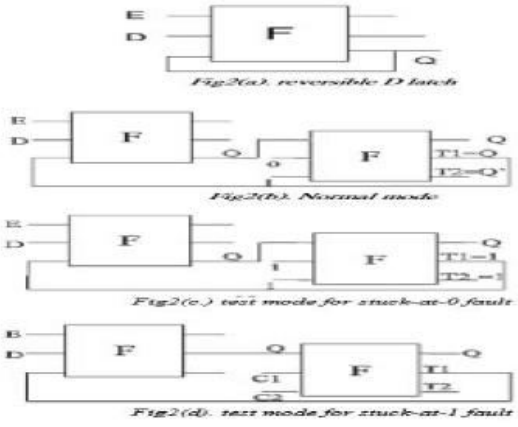
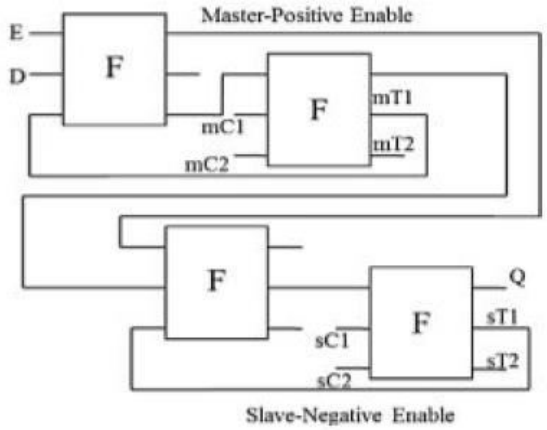


Fig2(a). reversible D latch
Fig2(b). Normal mode
Fig2(c) test mode for stuck-at-0 fault
Fig2(d). test mode for stuck-at-1 fault

3) DESIGN OF TESTABLE MASTER-SLAVE FLIPFLOPS

We have proposed the design of testable flip-flops using the master slave strategy that can be tested for any stuck-at faults using only two test vectors, all 0s and all 1s. Master latch will be positive enabled Fredkin gate based D latch and slave latch will be negative enabled Fredkin gate based D latch.Fig 4 shows the master-slave D flip flop. There are 4 control signals sC1, sc2, mC1 and mc2. mC1 and mC2 control the master latch and similarly sC1 and sC2 control the slave latch. When signals are given as 0 and 1 it will work in normal mode and avoid fan out problem. If the signals are given 0 and 0 it will disrupt the feedback and test the circuit for stuck-at-1 fault. Suppose if the signals are given as 1 and 1 then it will test the circuit for stuck-at-0 fault. Here Master controls the slave latch. If signal is given as 1 master latch works and vice-versa slave latch will work.



4) DESIGN OF TESTABLE REVERSIBLE DETFLIP-FLOPS

In the master-slave flip-flop, it does not sample the data at both clock edges; instead it waits for the next rising edge of the clock

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to work as a master or slave latch. In order to overcome the abovementioned problem, researchers have introduced the concept of DET flip-flops which sample the data at both the edges. Thus, DET flip-flops can sample and receive two data values in a clock period thus frequency of the clock can be reduced to half of the master- slave flip-flop while maintaining the same data rate. The half frequency operations make the DET flip flops very much useful for low power computing as frequency is equal to power consumption in a circuit. It is designed by connecting the two latches, via, the positive enable and the negative enable in parallel rather than in series. The 2:1 Multiplexer at the output transfer the output from one of these latches which is in the storage state (is holding its previousstate).

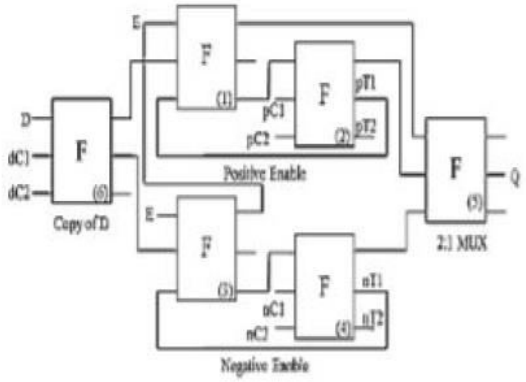

Fig5. DET flip-flop

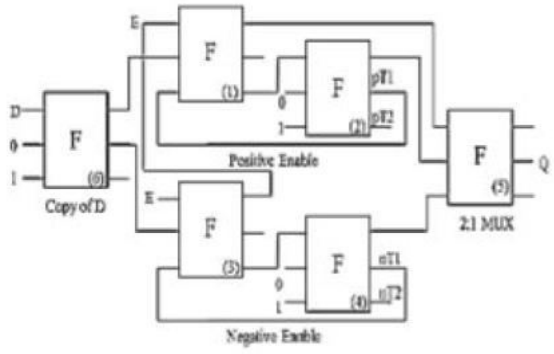

Fig5(b). normal mode

In the proposed design of testable reversible DET flipflop, the positive enable testable reversible D latch and the negative enable testable reversible D latch are set up in parallel. The Fredkin gates labeled as 1 and 2 forms the positive enable, while the Fredkin gates labeled as 3 and 4 forms the negative enable testable D latch. In reversible logic Fan-out is not allowed so the Fredkin gate labeled as 6 is used to copy the input signal D. The Fredkin works as the 2:1 MUX and transfer the output from one of these testable latches (negative enable D latch or the positive enable D latch) that is in the storage state (is holding its previous state) to the output Q.

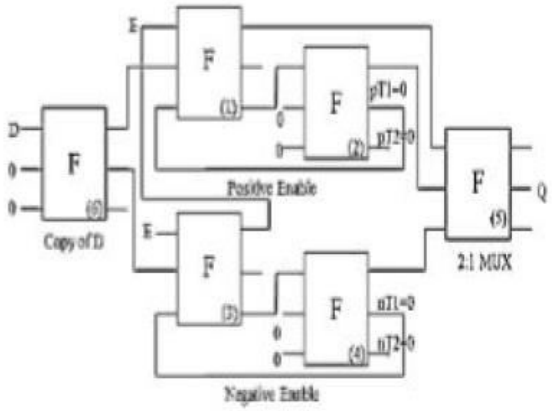

Fig5(c). test mode for stuck-at-1 fault

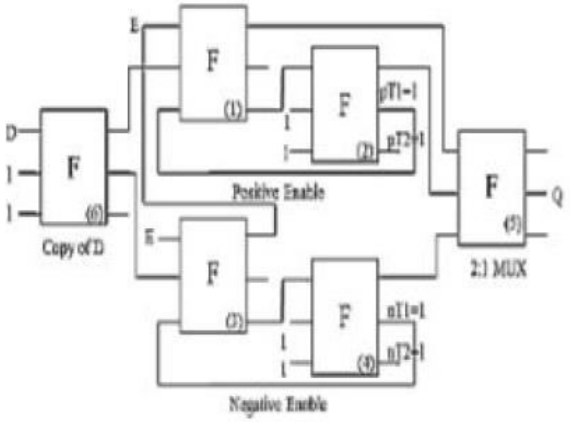

Fig5(d). test mode for stuck-at-0 fault

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In the proposed design of testable reversible DET flip-flop, nC1 and nC2 are the controls signals of the testable negative enable D latch, while pC1 and pC2 are the control signals of the testable positive enable D latch. Depending on the values of the pC1, pC2,nC1, and nC2, the testable DET flip-flops workeither in normal mode or in the testing mode.

RESULTS

Te proposed design results have been illustratedbelow. Those are tested on two faults and waveformsare illustrated.

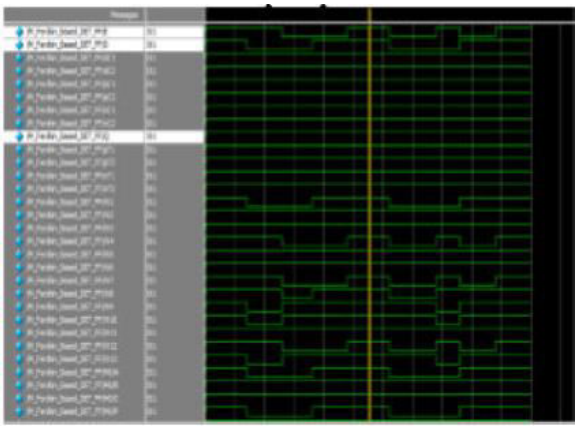

Fig: Test Mode: 1 for DET

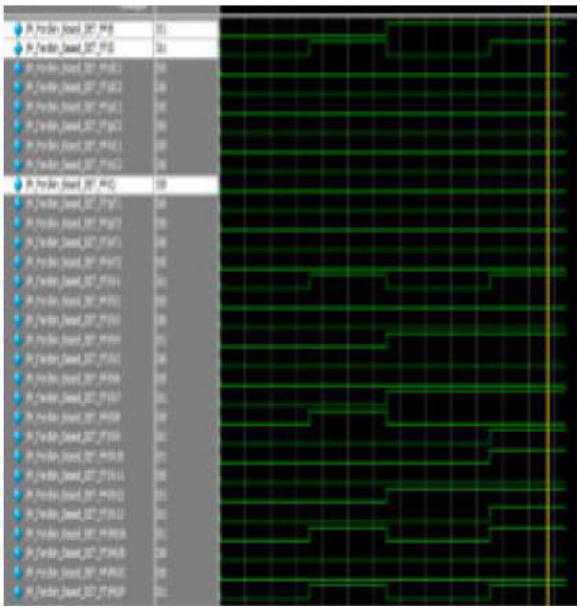

Fig: Test Mode: 2 for DET

CONCLUSION

Thus Reversible sequential circuits are designedusing reversible and conservative logic successfully and tested for stuck-at-faults. A design of Fredkin gate, testable D latch using Fredkin gate, Master slave flip-flop using Fredkin gate, DET flip flop is designed. It is made testable only using two vectors 0 and 1 and so complexity is reduced.

FUTURE SCOPE

In the proposed system we have designed sequential circuits using Fredkin gate. As sequential circuit has feedback it supports reversible logic and hence we designed circuits using reversible logic gate. So in future I would be designing combinational circuits which are irreversible using reversible logic. And also there is an advanced and a complex gate than Fredkin gate which is used in nano technology that is MXQCA gate also will be designed and corresponding circuits using that gate will be designed. From the above output we can see that if control signal or given as 1 means master latch will produce the positive enabled D latch output and similarly 0 means slave latch will produce the negative enabledD latch output.

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