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VHDL IMPLEMENTATION OF OFDM TRANSCIEVER

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ABSTRACT

OFDM is a multi-carrier modulation technique with densely spaced sub-carriers that has gained a lot of popularity among the broadband community in the last few years. Orthogonal frequency division multiplexing (OFDM) is an established technique for wireless communication applications. In this paper, system will be illustrated along with detailed simulation of the OFDM system to study the effect of various design parameters. OFDM transceiver will be implemented using FPGA kit. All modules are designed with VHDL programming language. VHDL be used for RTL description and FPGA synthesis tools will be used for performance analysis of the proposed core. ISIM Xilinx Edition will be used for functional simulation and verification. Xilinx ISE will be used for synthesis.

Keywords: Orthogonal Frequency Division Multiplexing (OFDM), Field Programmable Gate Array (FPGA), Very large scale integrated circuit hardware description language (VHDL).

1.INTRODUCTION

With the rapid growth of digital communication in recent years, the need for high-speed data transmission has increased. The mobile telecommunications industry faces the problem of providing the technology that be able to support a variety of services ranging from voice communication with a bit rate of a few kbps to wireless multimedia in which bit rate up to 2 Mbps. Many systems have been proposed and OFDM system based has gained much attention for different reasons. **Orthogonal frequency-division multiplexing** (**OFDM**) is a method of encoding digital data on multiple carrier frequencies. OFDM has developed into a popular scheme for wideband digital communication, used in applications such as digital television and audio broadcasting, DSL , wireless networks, powerline networks, and 4G mobilecommunications.OFDMisa frequencydivisionmultiplexing (FDM) scheme used as a digital multi-carrier modulation method. A large number of closely spaced orthogonal sub-carrier signals are used to carry data[1] on several parallel data streams or channels. Each sub-carrier is modulated with a conventional modulation scheme (such

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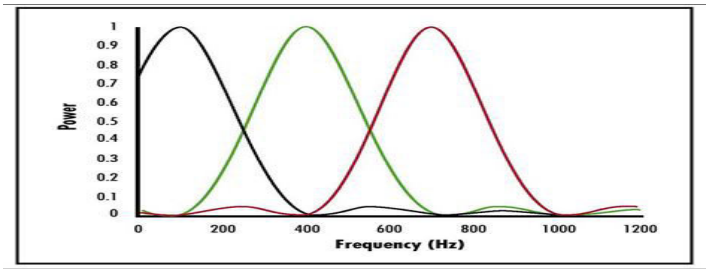
as quadratureamplitudemodulation or phase-shift keying) at a low symbol rate, maintaining total data rates similar to conventional *single-carrier* modulation schemes in the same bandwidth.Although OFDM was first developed in the 1960s, only recently has it been recognized as an outstanding method for high-speed cellular data communication where its implementation relies on very high-speed digital signal processing, and this has only recently become available with reasonable prices of hardware implementation.

1. PRINCIPLES OF OFDM

Orthogonal Frequency Division Multiplexing (OFDM) is a modulation scheme having multicarrier transmission technique [7]. In OFDM, spectrum is divided into abundant carriers each one being modulated at lower data rates. In FDM subcarriers are non-overlapping, hence requires more bandwidth. Saving of bandwidth in OFDM is own FDM is analogous to FDM but much more spectrally effective by positioning the sub-channels much closer together. This is done by selecting the frequencies that are orthogonal and by letting the spectrum of each sub channel to overlay another without interfering with it. OFDM splits the available bandwidth into many narrowband channels (typically 100-8000), each with its own sub-carrier. These sub-carriers are made orthogonal to one another, meaning that each one has an integer number of cycles over a symbol period. Thus the spectrum of each sub-carrier has a "null" at the Centre frequency of each of the other sub-carriers in the system, as demonstrated in Figure 1 below. This results in no interference between the sub-carriers, allowing then to be spaced as close as theoretically possible



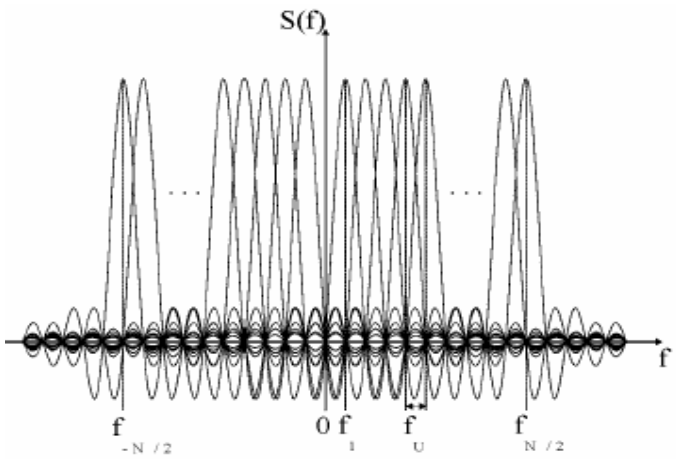


Fig.1 Orthogonality of sub-carriers Fig.2 OFDM sub carriers in the frequency domain

2. METHODOLOGY

The methodology of this paper is basically divided into four main stages. These stages is started with study the relevant topics and followed by the design process, implementation, test and analysis stages.

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All stages are subdivided into several small topics or sub-stages and explanation for each stage will be carried out in this paper.

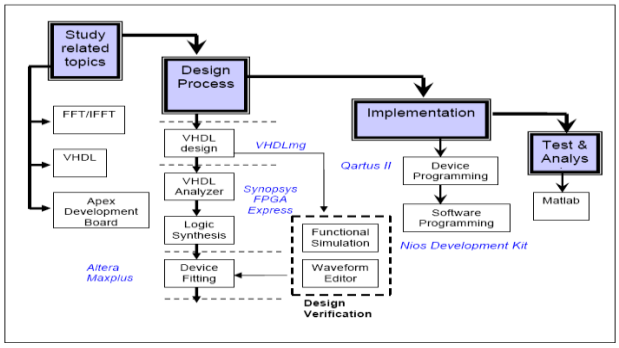

Fig.3 Methodology

2.IMPLEMENTATION

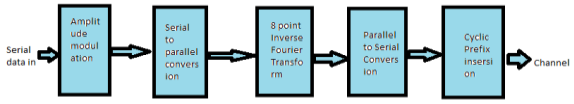

Fig 4: Simplified transmitter block diagram.

The generation of OFDM signal started from amplitude modulation mapping bank. The serial input data is mapped to appropriate symbol to represent the data bits. These symbols are in serial and need to convert into parallel format since IFFT module requires parallel input to process data. The serial to parallel module does the conversion. These parallel symbols are transformed from frequency domain into time domain using IFFT module. These signals are converted into serial format and add a cyclic prefix to data frame before being transmitted.

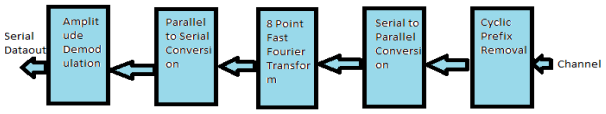

Figure 5: simplified receiver block diagram.

Figure above show the basic block diagram for receiver module. There are five modules in the receiver block and as mention before, cyclic prefix removal will not be included into the design. The received data is in serial format, thus, since FFT input is in parallel, a module which use to converts from serial to parallel is required. Output from FFT is converted back to serial format through parallel to serial converter. The conversion is required since the serial data need to be transmitted. Finally the serial output is demodulated using de-mapping module to get the transmitted data.

4.0 Generation of OFDM signals:

To implement the OFDM transmission scheme, the message signal must first be digitally modulated. The carrier is then split into lower-frequency sub-carriers that are orthogonal to one another. This is achieved by making use of a series of digital signal processing operations.The message signal is first modulated using a scheme such as BPSK, QPSK, or some form of QAM (16QAM or 64QAM for example). In BPSK, each data symbol modulates the phase of a higher frequency carrier. Figure 2.2 shows the time-domain representation of 8 symbols (01011101) modulated within a carrier using BPSK. In the frequency domain, the effect of the phase shifts in the carrier is to expand the bandwidth occupied by the

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BPSK signal to a *sinc* function. The zeros (or "nulls") of the *sinc* frequency occur at intervals of the symbol frequency.

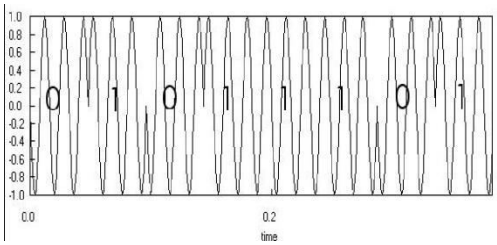

Fig 6: BPSK representation of "01011101"

Fig7: A set of orthogonal signals

Originally, multi-carrier systems were implemented through the use of separate local oscillators to generate each individual sub-carrier. This was both inefficient and costly. With the advent of cheap powerful processors, the sub-carriers can now be generated using Fast Fourier Transforms (FFT). The FFT is used to calculate the spectral content of the signal.It moves a signal from the time domain where it is expressed as a series of time events to the frequency domain where it is expressed as the amplitude and phase of a particular frequency. The inverse FFT (IFFT) performs the reciprocal operation.The underlying principle here is that the FFT can keep tones orthogonal to one another if the tones have an integer number of cycles in a symbol period. In the example figure 2.3 below, we see signals with 1, 2, and 4 cycles respectively that form an orthogonal set.To convert the sub-carriers to a set of orthogonal signals, the data is first combined into frames of a suitable size for an FFT or IFFT. A FFT should be always in the length of 2N (where N is an integer). Next, an N-point IFFT is performed and the data stream is the output of the transmitter. Thus when the signals of the IFFT output are transmitted sequentially, each of the N channel bits appears at a different sub-carrier frequency.By using an IFFT process, the spacing of the sub carriers is chosen in such a way that at the frequency where the received signal is evaluated, all other signals is zero. In order for this orthogonality, the receiver and the transmitter must be perfectly synchronized. This means they both must assume exactly the same modulation frequency and the same time-scale for transmission. At the receiver, the exact inverse operations are performed to recover the data. Since the FFT is perform The main blocks of transmitter and receiver are FFT and IFFT. The fourier transform is given by

$$X(K)=\sum_{n=0}^{N-1} x(n)e^{-j2\pi k/N}$$

X(k) represent the DFT frequency output at the *k*-the spectral point where *k* ranges from 0 to *N-1*. The quantity *N* represents the number of sample points in the DFT data frame. The quantity *x(n)* represents the *n*-th time sample, where *n* also ranges from 0 to *N-1*. In general equation, *x(n)* can be real or complex.

The DFT equation can be rewritten into

$$X(K)=\sum_{n=0}^{N-1} x(n)W_N^{nk}$$

The quantity W_N^{nk} is defined as $W_N^{nk}=e^{-j2\pi nk/N}$ it is defined as twiddle factor

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8point FFT twiddle factor can be defined as follows

Table 4.0: Twiddle Factor value for FFT

	nk=1	nk=2	nk=3	nk=4	nk=5	nk=6	nk=7	nk=8
W	W_8^0	W_8^1	W_8^2	W_8^3	W_8^4	W_8^5	W_8^6	W_8^7
Value	1	0.7071-j0.7071	-j1	-0.7071-j0.7071	-1	-0.7071+j0.7071	J1	0.7071+j0.7071

For decimation in frequency radix-2, the input is separated into two halves which is:

x(0),x(1),……x(N/2-1) and x(N/2), x(N/2+1),……..x(N-1)

Thus the DFT also can be separated into two summations:

$$X(k)=\sum_{n=0}^{(N/2-1)} x(n)W^{nk} + W^{kN/2} \sum_{n=N/2}^{N-1} x(n)W^{nk}$$

Thermore, let:

$$a(n)=x(n)+x(n+N/2)$$

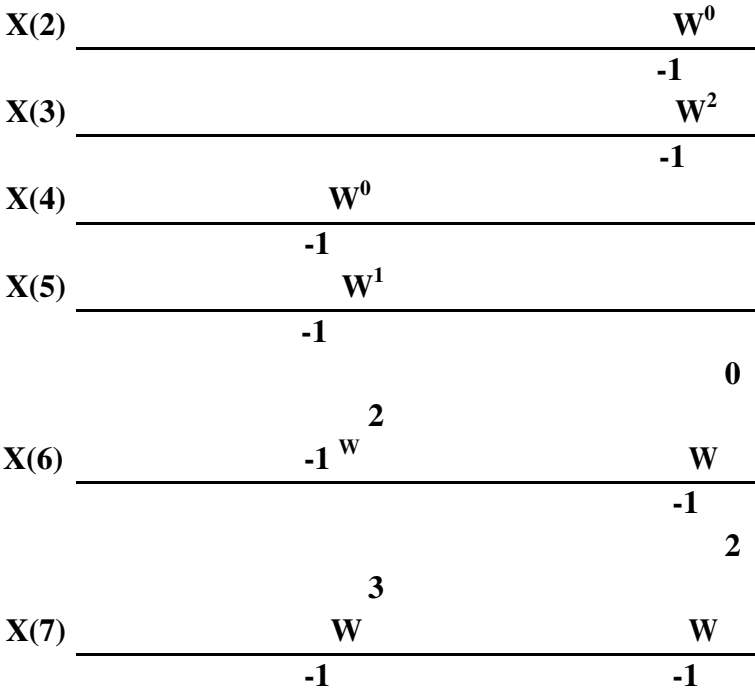
$$b(n)=x(n)-x(n+N/2)$$

To equation ….:

$$X(2k)= \sum_{n=0}^{(N/2)-1} a(n)\, W_{N/2}^{nk}$$

as

$$X(2k+1)= \sum_{n=0}^{(N/2)-1} b(n)\, W_{N/2}^{nk}$$

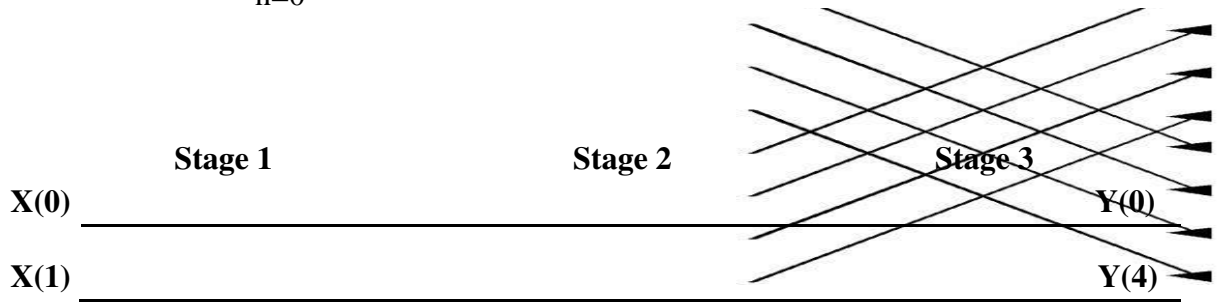


The equation above shows that for FFT decimation in frequency radix 2, the input can be grouped into odd and even number. Thus, graphically the operation can be view using FFT flow graph shown in figure. →

From this figure, the FFT computation is accomplished in three stages.

4.7.1 FFT Signal Flow Graph.

The X(0) until X(7) variable is denoted the input value for FFT computation and Y(0) until Y(7) is denoted as the output.



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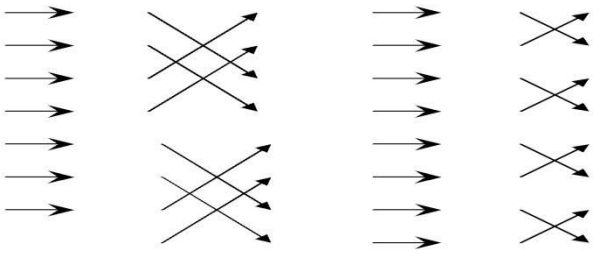


Figure 4.8: 8-point FFT flow graph using decimation-in-frequency

FFT stage 1

FFT stage2

FFT stage3

X(0)+X(4)=>X'(0)

X'(0)+X'(2)=>X''(0)

X''(0)+X''(1)=>Y(0)

X(1) + X(5)=>X'(1) X'(1) + X(3) => X"(1) X"(1) – X"(5) => Y(1),

X(2) +X(6) => X'(2) [X'(0) – X'(2)]W0 => X"(2) X"(2) + X"(3) => Y(2),

X(3) + X(7) =>X'(3) [X'(1) – X'(3)]W0=>X"(3) X"(2) – X"(3) => Y(3),

[X(0) – X(4)]W0 => X'(4) X'(4) + X'(2) => X"(4) X"(4) + X"(5) => Y(4)

[X(1) – X(5)]W1 => X'(5) X'(5) + X(3) => X"(5) X"(4) – X"(5) => Y(5),

[X(2) – X(6)]W2 => X'(6) [X'(4) – X'(6)]W0 => X"(6) X"(6) + X"(7) => Y(6),

[X(3) – X(7)]W3 => X'(7) [X'(5) – X'(7)]W0 => X"(7) X"(6) – X"(7) => Y(7)

	nk=1	nk=2	nk=3	nk=4	nk=5	nk=6	nk=7	nk=8
W	W_8^0	W_8^1	W_8^2	W_8^3	W_8^4	W_8^5	W_8^6	W_8^7
Value	1	0.7071-j0.7071	-j1	-0.7071-j0.7071	-1	-0.7071+j0.7071	J1	0.7071+j0.7071

Inverse Fast Fourier Transform

Inverse Fast Fourier Transform (IFFT) is used to generate OFDM symbols. The data bits is represent as the frequency domain and since IFFT convert signal from frequency domain to time domain, it is used in transmitter to handle the process. IFFT is defined as the equation below:

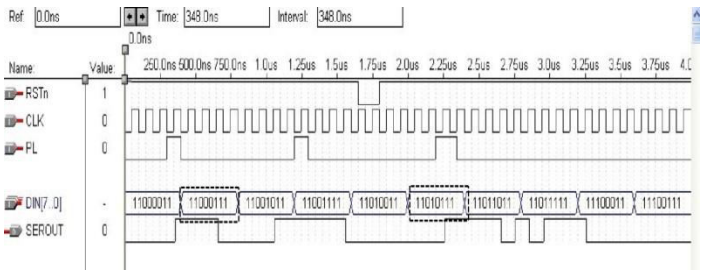
$$X(n)=\frac{1}{N}\sum_{k=0}^{N-1} x(k)W^{-nk}, k=0,1,2\ldots\ldots.$$

Below is the table show the value of twiddle factor for IFFT.

Table 4.1: Twiddle factor for 8 point Inverse Fast Fourier Transform

2.SIMULATION RESULTS

2.1Simulation Result of Serial to Parallel Conversion and Parallel to serial conversion:



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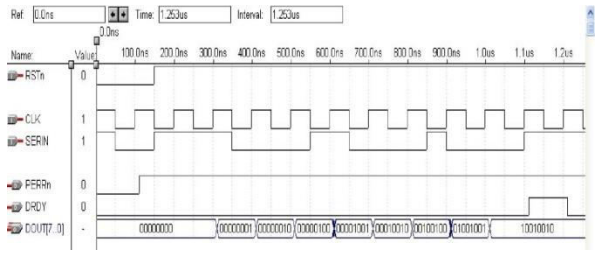

Fig 8: Simulation waveform of the serial to parallel.

Fig 9: Simulation waveform for parallel to serialThe Fig6 shows a simulation waveform for an input data '11001001'. The input data is in serial format and the conversion is started with the start bit is being asserted '1' in the SERIN input. Then, the SERIN input receives serial data '1','1','0','0','1','0','0','1' followed by the even parity bit of value '0'. After the parity bit is received, the output signal DRDY is asserted '1' in the next clock cycle. The DRDY signal is used to tell another circuit block to get the parallel data from DOUT right away. Otherwise the data may be lost when the next word comes. The DRDY and the start bit are allows to be asserted simultaneously and DOUT's value is changed right after DRDY is disserted. The old data is shifted out bit by bit. Output PERRn is not asserted since the parity error is not detected..Fig7above show three example of data conversion from parallel to serial. When input signal PL is asserted '1', the data DIN "11000111" is parallel loaded into the parallel to serial circuit. In the next clock cycle, a start bit of '1' is outputted, followed by the data "11000111", then completed with an even parity bit of value '1'. After that, the output stays at low until the PL input is asserted again. The second data is "11001111" and start bit value is '1'. But during data conversion RSTn signal is asserted to '0' result that the output of SEROUT is '0'. The third data is "11010111". The start bit is same followed by data and parity bit value is '1'.

2.2Simulation Result of OFDM transmitter and Reciever

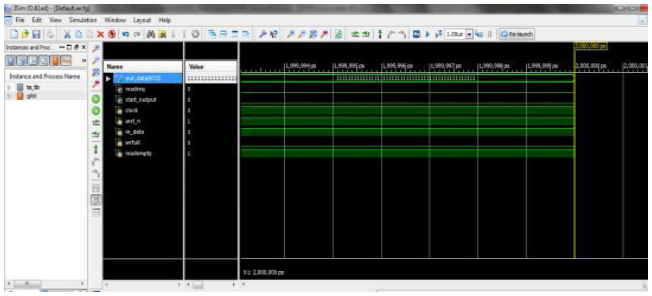

Fig.10simulation result of OFDM Transmitter

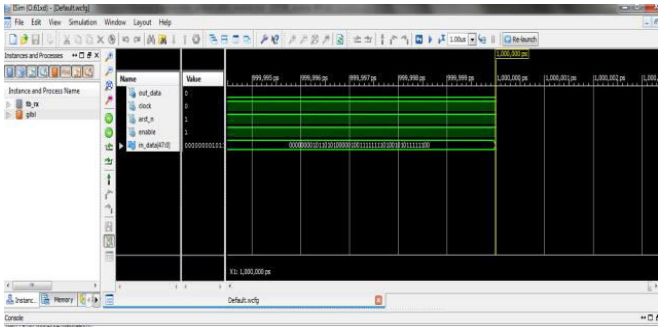

Fig.11 simulation result of OFDM Receiver

CONCLUSION

A baseband OFDM transmitter and receiver were successfully designed on FPGA. Each block was tested using Xilinx ISE. The complete resource utilization is 4% f the number of slice FLIP FLOPS and 72% of 4 input LUT's.

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