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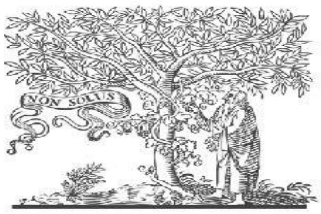

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Paper Authors
GANGOLU RAJESH, RAJU THOMMANDRU

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DESIGN AND IMPLEMENTATION OF HIGH EFFICIENT HYBRID TREE ADDER ARCHITECTURE

[1]GANGOLU RAJESH, [2]RAJU THOMMANDRU

[1]M.Tech Scholar, Dept of ECE, Chalapathi Institute of Technology, AR Nagar, Mothadaka, Guntur, Andhra Pradesh, India

[2]Associate Professor, Dept of ECE, Chalapathi Institute of Technology, AR Nagar, Mothadaka, Guntur, Andhra Pradesh, India

ABSTRACT: Adders are an almost requisite element of every modern integrated circuit. Since adders are used in many complex digital circuits as a basic component, enhancing digital adder performance would greatly accelerate binary operations within such complex circuits. On the most efficient and fastest adders developed are the parallel prefix adders. The popularity of the parallel prefix adders is that its ability to compute addition operation with a significantly high speed, reliability and efficiency, in the category of Very Large Scale Integration (VLSI). There are many types of parallel prefix adders that perform addition operation with various different logics and every type uses the prefix operation. The prefix operation is the logic of computing the output depending on the previous input. Therefore design and implementation of high efficient hybrid tree adder architecture is proposed in this project. The Brent kung tree adder architecture is used in this design through black cell and gray cell to achieve the area optimized and high speed of implementation. This parallel adder will improve the performance and operation speed in effective way compared to existed one.

KEYWORDS: Very Large Scale Integration (VLSI), Adders, parallel prefix adders, modified Brent kung tree adder.

I. INTRODUCTION

Nowadays very large scale integration (VLSI) chips have led to rapid and innovative development in low power design. In recent years, the growth of personal computing devices such as portable computers and real time audio and video based multimedia applications, and wireless communication systems had made power dissipation a most critical design parameter. The need for low power design is also becoming a major issue in high performance digital systems such as microprocessor, digital signal processor and other applications. For these applications, multiplier is the major core block [1]. It functions as a fundamental operation in most signal processing.

Adders and Multiplier designs are the important elements of VLSI Design. With advanced growing chip designing, many researchers and developers have taken much effort to design multipliers which initiates high speed, reduced power consumption and reduced area of multipliers, thus making them compatible for various high speed, low power, and compact VLSI implementations. Area, speed and power are the important parameters; the power is affected due to increasing speed and area. Here the two multipliers such as Array and Wallace tree multipliers designed to obtain an efficient

multiplier. Due to its high degree of regularity, array multiplier structure is suitable for VLSI implementation. Addition is a fundamental arithmetic operation for which a wide variety of algorithms and methods exist. Many alternatives for adder architectures have been invented with emphasis on their VLSI circuit implementation [2]. Carry look ahead (CLA), carry-skip, and carry-select adder architectures, among many others, present different area-delay power tradeoffs. Several works studied energy-efficient adders. It was noted that faster arithmetic circuits can be more energy efficient, a direction taken by our work.

In very large scale integration digital systems the addition operation is calculated by using parallel prefix adders. The quite faster adders are giving support to VLSI chips and parallel prefix adders are inside the chip to calculate the mathematical operations. For the VLSI calculations the basic or standard adders are more than enough, but the delay path is going to overpower the adder when the width of the adder increases. So the parallel prefix adders take into action to achieve this problem [3]. Now a day the parallel prefix adders are widely used in order to calculate efficiency, power and delay of every adder individually and it makes differentiation with another adders. This type of adders are more convenient, accurate and having the high speed while execution. This paper proposes a hybrid tree adder where addition takes place by considering the hybrid carry propagation.

II. LITERATURE SURVEY

Pallavi Saxena et al [4] proposed a paper on "Design of Low Power and High Speed Carry Select Adder Using Brent Kung Adder". In this paper constraint carry select adder architectures are proposed using parallel prefix adders (Brent Kung Adder) is used to design linear Carry Select Adder. By using Carry look ahead adder to derive fast results but they leads to increase in area. Sandeep Kakde et al (2015) [5] proposed a paper on "Design of Area and Power Aware Reduced Complexity Wallace Tree Multiplier". In this paper, the work has been done to reduce the area by using energy efficient CMOS full adder. By using the multiplier, the system complexity is increased. Ko, Seok-Bum, *et.al.*, [6], have proposed that the large cost of parallel multiplication units can be easily overcome by use of sequential architectures. They have also mentioned that besides the low area cost of sequential multipliers, the delay incurred by them is quite large. The prime concern of this reported data is to lower down the high amount of latency incurred by the sequential multiplication units but to maintain the lowest possible area cost. In this work the cycle time of the multiplication unit is maintained to be equal to the sum of delay caused due to binary half-adder and the delay caused due to decimal multiply-by-2 function. This delay is lower than the delay caused due to decimal CSA. In this work, encoding scheme of 4-2-2-1 is used for the generation and creation of the partial products.

Tso-Bing Juang, *et.al.*, [7], have proposed digit-serial and parallel implementations of decimal adders with three operands which are efficient in terms of area. The proposed decimal adders can do calculations easily with three operands by making use of designed analyzer circuits. The obtained results clearly mention the area-efficient behavior of the proposed decimal adders. The results also show that the power requirements are less. Besides its parallel implementation, they simply improve the throughput, efficiency and frequency of

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operation. It offers easy computations for additions, multiplications and divisions with multiple operands. Rajaram S et al [8] proposed a paper on "Improvement of Wallace Multipliers using Parallel Prefix Adders". In this paper, employing parallel prefix adders (fast adders) at the final stage of Wallace multipliers to reduce the delay.

Hybrid adder architecture was also proposed in [9]. It improved the area-delay curve by offering a wider range of power-delay optimization, obtained by concatenating several subgroups of various, independent, adder architectures. Sub-groups optimal size was set by solving an appropriate ILP optimization. Our approach is different. The LSB and MSB parts are working in parallel, where the sums and MSC of the MSB part consider the LSB part. Another advantage is the scalability, allowing repetition of the hybrid LSB-MSB mix in wide adders, where the mix is fixed, determined by the adder size, and non-repetitive. In [10] a method for sign detection in a Binary Signed-Digit (BSD) number system based on optimized reverse tree structure was proposed. It focused on time-area (and hence energy) efficient generation of the carry-out and was shown to be advantageous compared to BSD CLA implementation. Computation of MSC was also proposed for address generation of FFT circuits.

III. HYBRID TREE ADDER

Parallel prefix adders can be utilized to improve the performance and for reducing the delay. For determining the large group prefixes and calculating the small group intermediate prefixes the concept of parallel prefix adders are used until the completion of all carry bits computation. Parallel prefix addition of the operands A & B of width n is done in five steps using Brent Kung (B.K) adder architecture is represented in Figure (4.1). Initially it takes inputs A ad B and assigns to the propagator and generator block through registers. In this block each bit in two inputs are multiplied bit by bit and produces partial products and these partial products are applied used to compute the Propagate (P_i) and Generate (G_i) signals. Then these signals are applied to the black and grey cells that plays key role in the generation and propagation of carry to a particular adder stage. Black cells consists one OR gate and two AND gates, whereas grey cell consists one AND gate and one OR gate. Here hybrid adder tree architecture is implemented for the partial product addition through black and gray cells. Hybrid adder architecture used in this project is Brent – Kung parallel prefix structure which does not wait for preceding bit addition operation and modification is done at gate level to improve the speed and decreases the area. Finally XOR-based sum logic is used to find the final sum and carry of addition operation.

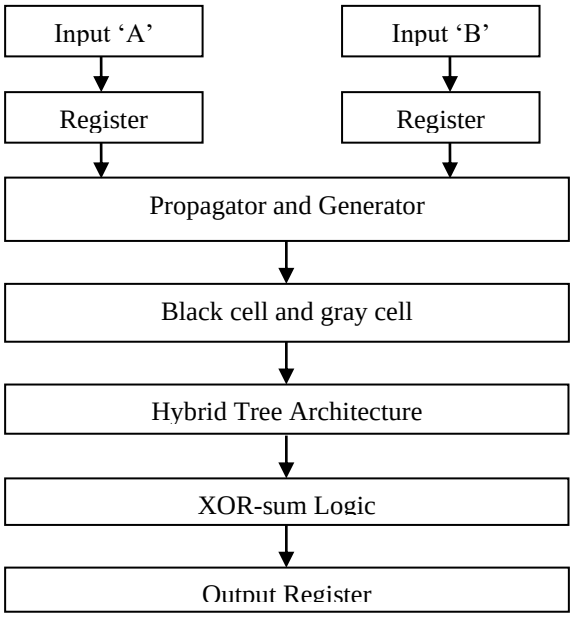

Fig. 1: ARCHITECTURE OF HYBRID TREE ADDER

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3.1 Propagator and Generator

In this stage, generate and propagate produced are from each pair of the inputs. The propagate gives "XOR" operation of input bits and generates gives "AND" operation of input bits. In this stage, half sum (d_i), Propagate (p_i) & Generate (g_i), signals for all the adder bits are calculated using the following equations.

$$g_i = A_i \quad \text{---------- (1)}$$
$$p_i = A_i \quad \text{---------- (2)}$$
$$d_i = A_i \oplus B_i \quad \text{---------- (3)}$$

Here $0 \leq i \leq n-1$, where n is the word length.

The current full adder output signal "sum (S_i)" & the right-adjacent full adder output signal "carry" bit are used together to calculate propagate (P_i) & generate (G_i) signals in the 2nd stage (base logic). The "squared saltire - cell" represents the computation of Gi & Pi signals and in base logic stage n +1 number of saltire - cells are there. The saltire - cell realized by given logical expression,

$$G_{i:i} = g_i = S_i' \cdot cy_{i-1} \text{ ---------(4)}$$
$$P_{i:i} = p_i = S_i' \oplus cy_{i-1} \quad \text{---------- (5)}$$

3.2 Black and Gray Cells

The logical diagram of grey & black cell is represented in Figure 4.3 which can computes the carry propagate $P_{i:j}$ & generate $G_{i:j}$signals logical expressions are given below:

$$G_{i:j} = G_{i:k} + P_{i:k} \cdot G_{K-1:j} \quad \text{--------- (6)}$$
$$P_{i:j} = P_{i:k} \cdot P_{K-1:j} \quad \text{---------- (7)}$$

(log2 n+1) is the number of prefix computation stages of suggested adder . Hence of the proposed adder critical path delay is majorly effected by the carry propagate chain.

3.3 Hybrid Adder Tree Architecture

The proposed Brent-kung adder is flexible to speed up the binary addition and the arrangement looks like tree structure for the high performance of arithmetic operations. Field programmable gate arrays [FPGA's] are mostly used in recent years because they improve the speed of microprocessor based applications like mobile communication, DSP and telecommunication. Research on binary operation fundamentals and motivation gives development of devices. The construction of efficient Brent-kung adder consists of two stages. They are pre-processing stage and generation stage. Brent Kung adder is used for high performance addition operation. The Brent-kung is the parallel prefix adder used to perform the addition operation. It is looking like tree structure to perform the arithmetic operation. The Brent-kung adder consists of black cells and gray cells.

The efficient Brent-kungadder arrangement is looking like tree structure for the high performance of arithmetic operations and it is the high speed adder which focuses on gate level logic. It designs with a reduction of number of gates. So, it decreases the delay and memory used in this architecture. The modified Brent-kung adder tree architecture of 32-bt length is implemented which improves the speed and decrease the area for the operation of addition. The input bits Ai and Bi concentrates on generate and propagate by XOR and AND operations respectively. The propagate and generate signals undergoes the operations of black cell and gray cell and gives the carry Ci. That carry is XORed with the propagate of next bit, that gives sum.

3.4 XOR-Sum Logic

Sum bits are produced by simple XOR gates or using conditional sum adders. For every

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bit position in conditional sum adder 2 tentative sums can be produced and selects the correct one whenever relative carry bit arrives. The last stage is represented as sum logic in that the "sum (S_i)" bits are computed from the carry propagate Pi & carry generate $G_{i:j}$ bits by the logical expression,

$$S_i = (P_i \oplus G_{i-1:0}) \quad \text{---------- (8)}$$

This stage is where the overall adder operation is completed, the carry signals of the second stage will pass through to the final stage (i.e.,) Post-Processing Stage. The final result of the entire adder operation is obtained from the equation of sum and carry. From the carry generate bit $G_{n:0}$ the carryout signal (C_{out}) is directly obtained.

$$C_{out} = G_{n:0} \quad \text{---------- (9)}$$

IV. RESULTS

The Xilinx design environment was used to implement and examine the developed algorithm. The FPGA architecture of the proposed high efficient hybrid tree adder architecture is shown in Fig. 2 and Fig. 3. The below Fig. 2 and Fig. 3 show the RTL schematic and technology schematic of the proposed hybrid tree adder architecture. The RTL schematic is a combination of inputs and outputs. From here, register-transfer logic deliberation is utilized in equipment portrayal dialects (HDLs) like Verilog and VHDL to make elevated-level portrayals of a circuit, from which lower-level portrayals and, at last, genuine wiring can be determined. Structure at the RTL level is standard in today's advanced plan.

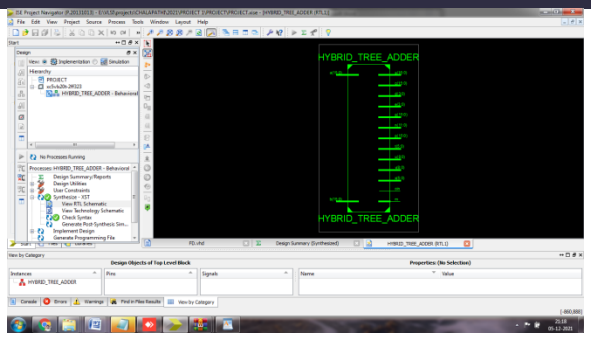

Fig. 2: : RTL SCHEMATIC OF PROPOSED HYBRID TREE ADDER

The technology schematic is a combination of look-up tables, Truth Tables, K-Maps, and equations. It shows the technology schematic of the hybrid tree adder architecture in the below figure (3). This schematic is generated after the optimization and technology targeting phase of the synthesis process. It shows a representation of the design in terms of logic elements optimized for the target Xilinx device, for example, in terms of LUTs, carry logic, I/O buffers, and other technology-specific components.

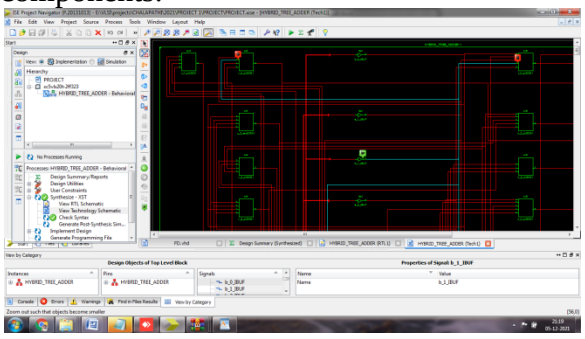

Fig. 3: TECHNOLOGY SCHEMATIC OF PROPOSED ADDER

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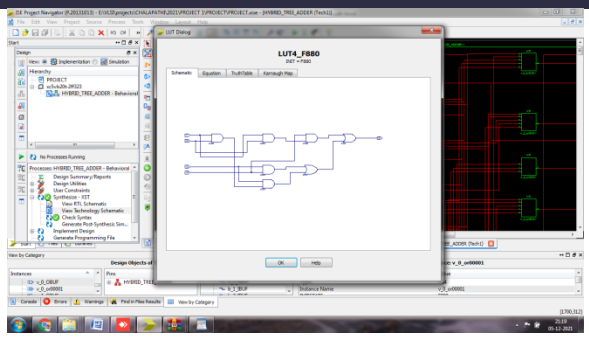

Fig. 4: LOOK UP TABLE (LUT)

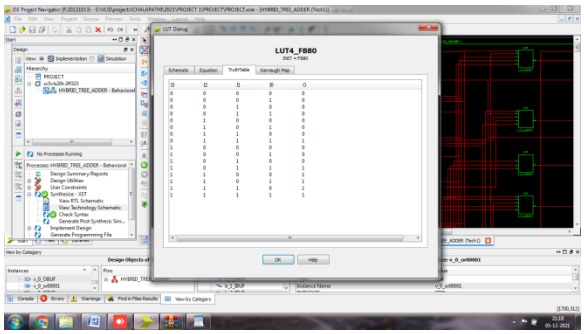

Fig. 4: TRUTH TABLE

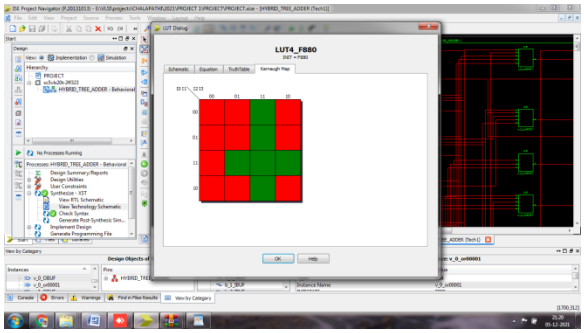

Fig. 6: K-MAP

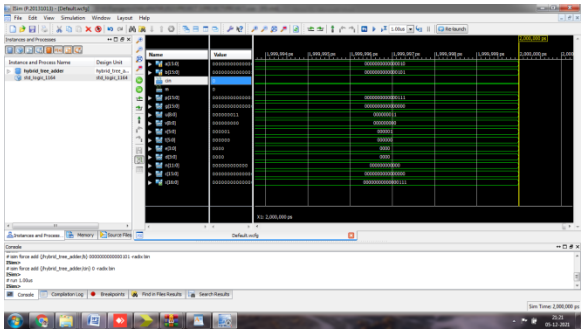

Fig. 7: OUTPUT WAVEFORMS

V. CONCLUSION

In this project design and implementation of high efficient hybrid tree adder architecture was proposed. The proposed adder architecture is a hybrid parallel prefix adder for computing the input operands addition using four stage structures. The propagator and generator stage is used to generated partial products which are used to produce propagate and generate signals. Then Black cell and gray cells were used for carry generation and propagation in each bit addition. After that brent kung tree adder structure stage is used in hybrid tree adder structure to perform parallel prefix addition and then generate carry. Finally XOR-based sum logic stage finds the sum and final carry of the addition. The reduction of area & delay in prefix computation stage in Brent kung tree adder structure and black cells & gray cell stages is the newness of the proposed adder system. This proposed system can reduce the number of cells in parallel adder to achieve the high speed. This parallel adder will improve the performance and operation speed in effective way compared to existed one.

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