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RENEWABLE ENERGY SOURCES FED ASYMMETRIC PWM FULL BRIDGE CONVERTER FOR GRID CONNECTED APPLICATIONS

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ABSTRACt: This paper presented Asymmetrical PWM controlled grid connected system, the asymmetrical PWM control develops high efficient controllable system. The proposed converter achieves ZVS and ZCS switching, can be implemented with asymmetrical full bridge high gain converter, power management system is designed for the proposed system to manage power flow among different sources. For AC grid connected applications to convert the dc to an ac source by using an inverter. A grid-tie control system is proposed for asymmetrical PWM converter with both active and reactive power flow capability in a wide range under two types of renewable energy and distributed generation sources. Power conditioning system (PCS) is Reactive power command is generated by distributed generation (DG) control site for both systems. Asymmetrical full bridge PWM leads to better performance in terms of less output current ripple and harmonics, no zero-crossing distortion. Generally, the renewable energy sources generate low-voltage energy. The renewable energy sources that depend on environment conditions especially generate fluctuating low-voltage energy. Thus, a frontend converter for fluctuating low-voltage energy is required between the low-voltage source and load requiring high voltage.

Keywords-Asymmetrical pulse-width modulated (PWM), full-bridge converter, soft switching, Inverter.

I. INTRODUCTION

With the exhaustion of the worldwide resources and the environmental pollutants, the research at the renewable power sources including gas cells and photovoltaic cells has been regularly extended in business fields [1-4]. Generally, the renewable power sources generate low-voltage strength. The photovoltaic cells which rely upon environment conditions particularly generate fluctuating low-voltage electricity. Hence, a front-cease converter for fluctuating low voltage electricity is required between the low voltage supply and cargo requiring excessive voltage.Forward/fly back converters that use an active-clamp with voltage double, LLC converters, and segment-shift full-bridge (PSFB) converters are usually not unusual topologies considered for growing electricity capability [5-6]. An energetic-clamp circuit correctly realizes the zero-voltage switching (ZVS) for the switches through using the leakage inductance, the magnetizing inductance, and the parasitic capacitance. Especially, forward/fly back converters that use the lively-clamp with voltage double offer the zero-

modern-day switching (ZCS) of the diodes of the transformer secondary side because of the resonant-cutting-edge formed with the leakage inductance and the resonant capacitor. But, ahead/ fly back converters have a far better voltage strain across the number one switches of the transformer than the input voltage. Therefore, the MOSFET with low on resistance RDS (on) cannot be hired [7]. With variable frequency manipulate, LLC resonant converter can be hired in all packages with variable enter and output voltages, call for of high performance and power density. But, due to very wide bandwidth, the frequency must be accelerated very excessive to acquire enough voltage advantage controllability. Particularly, traditional LLC resonant topology as the front quit converter of the micro-inverter is hardly implemented because it is tough to keep excessive performance over fluctuating input voltage with different load situations [8]. The section-shift full-bridge (PSFB) converters are widely used for high efficiency in the medium strength packages. The traditional phase-shifted full-bridge (PSFB) converter benefits from zero-voltage switching (ZVS) for all switches without the help of any auxiliary circuits [9-10]. However, this PSFB converter suffers from a narrow ZVS range of lagging-leg switches under wide load variation, which severely affects its light load efficiency [11]. Given the resonance between transformer leakage inductance and parasitic junction capacitance of a rectifier diode, serious voltage spikes across the diode rectifier are generated [12], which increases the diode voltage rating and causes electromagnetic interference problems. Excessive circulating current in the primary side during the freewheeling interval also increases the primary side conduction and turn-off switching losses of the lagging-leg switches [13]. From the corresponding waveforms of a traditional PSFB duty losses exist in the traditional PSFB converter, which increase the turns ratio of the transformer and current stress in the diodes. Many studies have attempted to overcome the said problems in a traditional PSFB converter. In order to extend the ZVS range and eliminate voltage spike of diode rectifier, additional auxiliary circuits are required, which increase complexity of the converter and cause additional conduction losses. A new PSFB converter proposed in [4] always operates at a maximum duty ratio of 50% by varying the primary turns of the transformer, thus eliminating the circulating current and decreasing primary-side conduction losses. The power rating for switches decreased and the efficiency improved in the input-series-connected FB converter proposed in [14]. However, this technique increases the controller complexity. The transformer secondary side resonance technique is proposed to achieve zero current switching (ZCS) for the diode. The ZCS for the output diode is achieved with the resonant tank in the secondary side, whereas the ZVS for switches is realized through the active clamp technique. However, such resonant technique results in an increased current stress of power switches. A hybrid switching mode step-down resonant-PWM converter is proposed to decrease the current stress of the power switch. It operates in PWM mode when the switch is turned on, whereas it operates in resonant mode when the switch is turned off.

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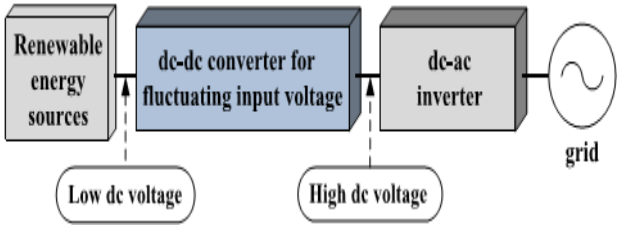

Fig.1.Renewable energy conversion system

II. ANALYSIS OF APWM FULL-BRIDGE CONVERTER

a)Circuit Configuration and Operation Principle

A circuit configuration of the highly efficient APWM full bridge converter for low input voltage range is shown in Fig.2. The configuration of the proposed converter is basically similar to that of the conventional full-bridge converter except for the dc blocking capacitor and the secondary side of the transformer. The primary side of the transformer consists of the primary winding turns N_p, the four switches, and the dc blocking capacitor C_b. The secondary side has the secondary winding N_s, the output diode D_o, and the output capacitor C_o.

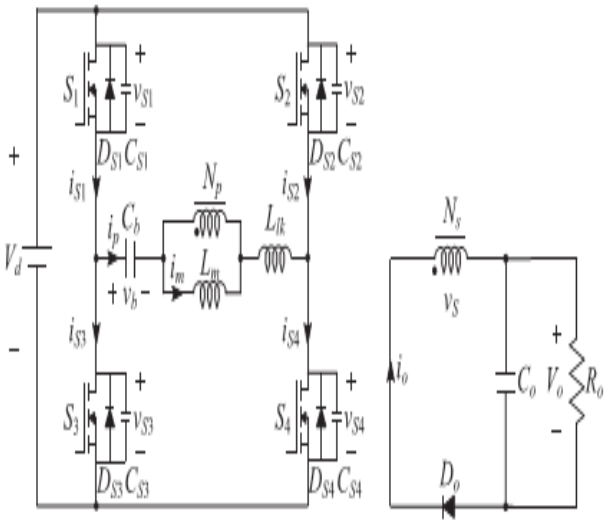

Fig.2.Circuit diagram of the proposed APWM full-bridge converter

To analyze the steady-state operation of the proposed APWM full-bridge converter, the following assumptions are made.

1) The transformer is modeled as an ideal transformer with the primary winding
2) turns N_p, the secondary winding turns N_s, the magnetizing inductance L_m, and the leakage inductance L_{lk}
3) All switches S_1–S_4 are considered as ideal switches except for their body diodes and output capacitors (C_{S1}=C_{S2}=C_{S3}=C_{S4}= C_{oss}).
4) The dc blocking capacitor C_b and the output capacitor C_o are large enough to neglect the voltage ripple on it, so the voltages across C_b and C_o are constant.

While the switch S_1 (S_4) operates with a duty ratio D, depending on the input voltage and load condition, the switch S_2 (S_3) operates with a duty ratio 1−D. In other words, the switches S_1 (S_4) and S_2 (S_3) are operated asymmetrically. Therefore, the circulating current loss of the primary side can be eliminated because the proposed converter has no freewheeling period. Fig.3 represents the operating modes, and Fig.4 represents the theoretical waveforms of the proposed converter under a steady-state condition. The operation of the proposed converter can be divided into six modes during a switching period T_s.

Mode 1[t_0, t1]: At t_0, the switches S_2 andS_3 are turned off. The primary current i_p discharges the output capacitances C_{S1} and C_{S4} of the switchesS_1 and S_4 and charges the output capacitancesC_{S2}andC_{S3} of switches S_2 and S_3. The interval of this mode is very short and negligible because the output capacitances C_{oss} of the switches are very small. Thus, the

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primary current i_p and the magnetizing current i_m are regarded as constant value.

Mode 2[t_1, t2]: Att_1, when the voltages v_{S1}andv_{S4}acrossthe switchesS_1 and S_4become zero, the negative current flows through their body diodesD_{S1}andD_{S4}before theswitchesS_1 and $S_4$are turned on. Then, ZVS operation is achieved with the turn-on of the switchesS_1 and S_4, and the resonance occurs between the dc blocking capacitor C_b and the primary inductor L_m+L_{lk} of the transformer, but resonance effect does not appear because the resonant period is much longer than one switching period T_s. Thus, by the difference between the voltages of the input and the dc blocking capacitor C_b, the direction of the primary current i_p is changed and kept almost linearly as follows:

$$i_p(t) = i_p(t_1) + \frac{V_d - V_b}{L_m + L_{lk}}(t - t_1) \quad (1)$$

Where V_d is the input voltage and V_b is the average voltage across the dc blocking capacitor C_b.

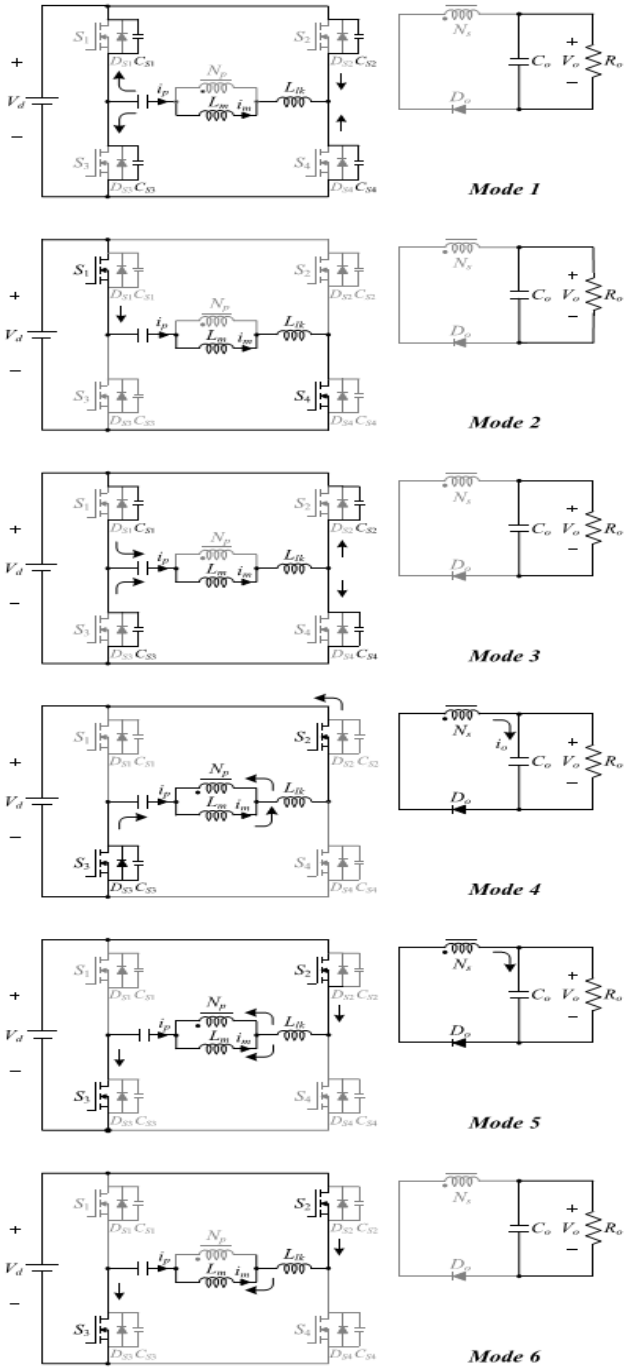

Fig.3. Operating modes of the proposed converter

Mode 3 [t_2, t_3]: At t_2, the switches S_1andS_4 are turned off. The primary current ip charges the output capacitances C_{S1}, C_{S4} of S_1, S_4 and discharges the output capacitancesC_{S2}, *CS3* ofS_2, *S4*. Similar to Mode 1, the primary current i_p

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and the magnetizing current i_m are regarded as constant value.

Mode 4 [t_3, t_4]: At t_3, similar to Mode 2, ZVS turn-on of the switches S_2 and S_3 is achieved. The energy stored in the magnetizing inductance is delivered to the secondary side of transformer, and the voltage across the magnetizing inductance L_m is clamped by the reflected output voltage as

$$L_m \frac{di_m(t)}{dt} = -\frac{V_o}{n} \tag{2}$$

Where $n=N_s/N_p$. Because the difference between the primary current i_p and the magnetizing current i_m is reflected in the output current i_o, the magnetizing current i_m is decreased as

$$i_m(t) = i_p(t_3) - \frac{V_o}{nL_m}(t - t_3) \tag{3}$$

The resonance occurs between the dc blocking capacitor C_b and the leakage inductance L_{lk} of the transformer. The voltage across the leakage inductance L_{lk} of primary side is the difference between $V_d + V_b$ and the reflected output voltage V_o/n from the secondary side. Thus, the state equations can be written as follows:

$$L_{lk} \frac{di_p(t)}{dt} = -V_d - V_b + \frac{V_o}{n} \tag{4}$$

$$C_b \frac{dv_b(t)}{dt} = i_p(t) \tag{5}$$

Solving (4) and (5), the primary current i_p is

$$i_p(t) = i_p(t_3)\cos\omega_r(t - t_3) + \frac{V_o/n - V_d - V_b}{Z_r}\sin\omega_r(t - t_3) \tag{6}$$

Where the resonant angular frequency ω_r and the impedance Z_r of the resonant circuit are

$$Z_r = \sqrt{\frac{L_{lk}}{C_b}} \quad \omega_r = \frac{1}{\sqrt{L_{lk}C_b}}. \tag{7}$$

Mode 5 [t_4, t_5]: At t_4, the primary current i_p becomes zero and changes its direction. Also, the magnetizing current im changes its direction during this interval. The output current i_o approaches zero at the end of this mode with resonant characteristics. When the output current i_o becomes zero, this mode ends.

Mode 6[t_5, t6]: At t_5, because the resonance launched in Mode 4is ended, the output current i_o becomes zero. However, the output diode D_o is maintained to on-state until the switches$S_2$and$S_3$are turned off. During this mode, the primary current i_p is equal to the magnetizing current i_m. Thus, ZCS turn-off of the output diode D_o is achieved.

b) Steady-State Analysis

While the switchesS_1andS_4operate with a duty ratio D, the difference between the input voltage V_d and the average voltage V_b of the dc blocking capacitor C_b is applied on the inductor of the transformer primary side. While the switchesS_2 and S_3 operate with a duty ratio $1-D$, the reflected output voltage V_o/n is applied on the inductor of the transformer primary side and the output diode D_o is turned-on. Since the resonant period of the resonant network is much longer than the dead-time duration, equations of the primary current i_p from (1) and (2) are derived as follows:

$$i_p(t_3) = i_p(t_1) + \frac{V_d - V_b}{L_m + L_{lk}} DT_s \tag{8}$$

$$i_p(t_1) = i_p(t_3) - \frac{V_o}{nL_m}(1 - D)T_s. \tag{9}$$

From the resonance of the primary side in Modes 4 and 5, since the leakage inductance L_{lk} is much smaller than the magnetizing

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inductance L_m, the leakage inductance L_{lk} is negligible. Therefore, the following equation can be obtained:

$$V_d + V_b \simeq \frac{V_o}{n} \tag{10}$$

From (8) to (10), the voltage gain between the input voltage V_d and output voltage V_o is expressed as follows:

$$\frac{V_o}{V_d} \simeq \frac{L_m}{L_m + L_{lk}} 2nD \simeq 2nD \tag{11}$$

Because the leakage inductance L_{lk} is negligible, the average voltage V_b of the dc blocking capacitor C_b is expressed from (10) and (11) as shown in

$$V_b = V_d(2D - 1) \tag{12}$$

Due to the charge balance of the dc blocking capacitor C_b, the average value of the primary current I_p is zero in the steady state. Thus, the relation between the average values of the magnetizing current I_m and average output current I_o can be determined as follows:

$$I_m - I_p = I_m - \frac{1}{T_s}\int_0^{T_s} i_p(t)dt = nI_o. \tag{13}$$

From Fig.4, the average magnetizing current I_m can also be obtained by

$$I_m = \frac{i_p(t_1) + i_p(t_3)}{2}. \tag{14}$$

$$i_p(t_1) = nI_o - \frac{(1-D)T_s}{nL_m}V_o \tag{15}$$

$$i_p(t_3) = nI_o + \frac{(1-D)T_s}{nL_m}V_o \tag{16}$$

$$i_p(t) = \left(nI_o + \frac{(1-D)T_s}{nL_m}V_o\right)\cos\omega_r(t-t_3) - \frac{V_o}{nL_m\omega_r}\sin\omega_r(t-t_3). \tag{17}$$

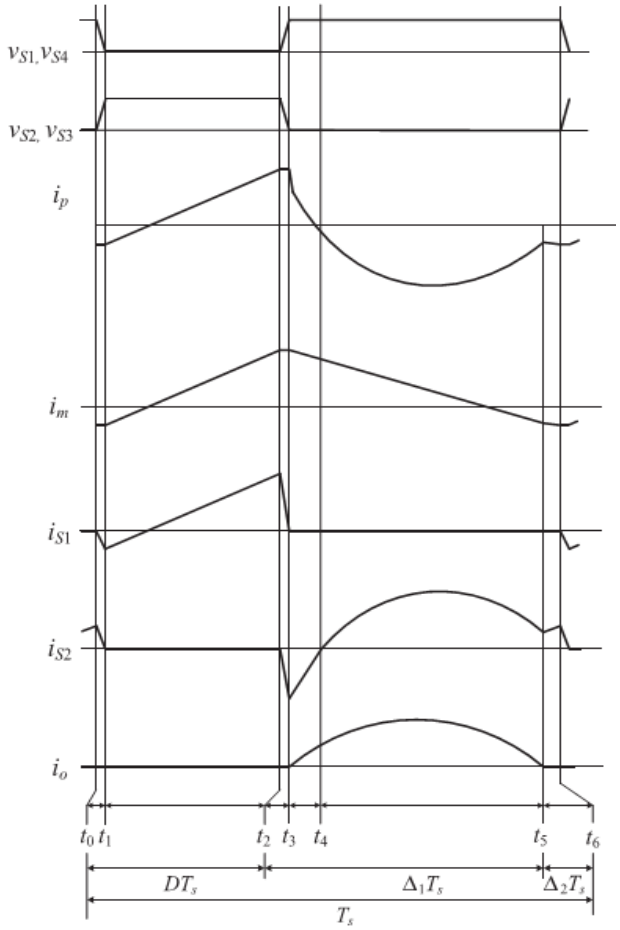

Fig.4.Theoretical waveforms of the proposed converter

From (1), (13), and (14), the currents i_p (t_1) and ip (t_3) are given by

Using (13)–(16), the resonant current (6) can be represented by

III. SOFT-SWITCHING CONDITIONS

a) ZVS Condition of the Power Switches

For ZVS turn-on of S_1 and S_4, the primary current i_p (t_1) should be negative before S_1 and S_4 are turned on. Thus, from (15), ZVS condition can be expressed as follows:

$$nI_o - \frac{(1-D)T_s}{nL_m}V_o < 0. \tag{18}$$

Equation (18) is arranged by the min–max theorem as

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$$\frac{n^2 L_m I_{o,\max}}{V_o} = \frac{n^2 L_m}{R_{o,\min}} < (1 - D_{\max}) T_s \tag{19}$$

Where $I_{o,max}$ is the maximum output current, $R_{o,min} = V_o/I_{o,\,max}$ is the minimum output resistance, and $D_{max}$is the maximum duty ratio of the switches S_1 and S_4under the minimum input voltage $V_{d,min}$. From (11), D_{max} can be described as

$$D_{\max} \simeq \frac{V_o}{2nV_{d,\min}}. \tag{20}$$

According to the variations of the input voltage V_d and turn ratio, the duty ratio of the switches S_1 and S_4. Thus, from (19) and (20), the magnetizing inductance L_m should be designed to satisfy ZVS condition as follows:

$$L_m < \left(1 - \frac{V_o}{2nV_{d,\min}}\right) T_s \cdot \frac{R_{o,\min}}{n^2} \tag{21}$$

Where T_s is a switching period. According to the variation of the duty ratio D, the critical magnetizing inductance value L_m to satisfy the ZVS turn-on condition of the switches The ZVS turn-on condition of the switches $S_2$and S_3 can be expressed with the same manner of ZVS condition of the switches $S_1$and S_4. Thus, ZVS operation of S_2 and S_3 can be achieved when the primary current i_p (t_3) is positive. From (16), ZVS condition of S_2 and S_3 is expressed as follows:

$$nI_o + \frac{(1 - D)T_s}{nL_m} V_o > 0. \tag{22}$$

The left side terms of (22) are always positive regardless of load variations. Therefore, ZVS operation of the switches S_2 and S_3can always is satisfied.

Another ZVS turn-on operation requires a sufficient dead time between two switch pairs to absolutely discharge the voltage across the output capacitance C_{oss} of the switches. Because i_p (t_1) = i_m (t_1) is regarded as constant value during the dead time, the minimum dead time Δt_{dead} can be calculated as

$$\min\{|i_p(t_1)|, |i_p(t_3)|\} \geq 4C_{oss} \frac{dV_d}{dt} \tag{23}$$

From (15) and (16), the primary current i_p (t_3) is always larger than the absolute value of the primary current i_p (t_1). Therefore, (23) can be simplified as

$$\Delta t_{dead} \geq \frac{C_{oss} V_d}{|i_p(t_1)|/4}. \tag{24}$$

The primary current i_p (t_1) should be negative for ZVS operation. Thus, (24) can be expressed as shown in

$$\Delta t_{dead} \geq \frac{4C_{oss} V_d}{\frac{(1-D)T_s}{nL_m} V_o - nI_o} \tag{25}$$

The minimum dead time Δt_{dead} should be considered in the practical design of the magnetizing inductance because Δt_{dead} is always smaller than $(1-D_{max})\,T_s$.

c) ZCS Condition of the Output Diode

To achieve the ZCS turn-off condition of the output diode Do, the resonant angular frequency ωr should be larger than the critical angular frequency ω_{rc}. Because the critical condition is ip (Ts) = $i_m(T_s)$ at $\Delta_2 T_s = 0$ and $D = D_{max}$, the critical angular frequency ω_{rc} can be described considering the negligible dead-time duration of the power switches as follows:

$$\left(\frac{n^2 L_m}{R_{o,\min}} + t_{S2,\min}\right) \cos\omega_{rc} t_{S2,\min} - \frac{1}{\omega_{rc}} \sin\omega_{rc} t_{S2,\min} - \frac{n^2 L_m}{R_{o,\min}} + t_{S2,\min} = 0 \tag{26}$$

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Where$t_{S2,min}$is the minimum turn-on duration of the switches S_2 and S_3. The magnetizing inductance $L_m$is generally designed for the magnetizing current $i_m(t_1)$to be a small negative value to minimize the conduction loss of the converter. By this assumption, (3.26) can be obtained as follows:

$$\tan \omega_{rc} t_{S2,\min} \simeq \omega_{rc} \frac{n^2 L_m}{R_{o,\min}} + \omega_{rc} t_{S2,\min} \quad (27)$$

From (21), (27) is expressed as shown in

$$\tan \omega_{rc} t_{S2,\min} < 2\omega_{rc} t_{S2,\min} \quad (28)$$

Thus, the critical angular frequency ω_{rc} can be calculated using a numerical method as shown in

$$\omega_{rc} \approx \frac{\pi + 1.462}{t_{S2,\min}} = \frac{\pi + 1.462}{(1 - D_{\max})T_s} \quad (29)$$

From (29), the dc blocking capacitance C_b must satisfy the following relation:

$$C_b \leq \frac{1}{\omega^2_{rc} L_{lk}} \quad (30)$$

According to the variation of the duty ratio D, the critical resonant capacitance C_b to satisfy the ZCS turn-off condition of the output diode D_o.

IV. PHOTOVOLTAIC SYSTEM

A Photovoltaic (PV) system directly converts solar energy into electrical energy. The basic device of a PV system is the PV cell. Cells may be grouped to form arrays. The voltage and current available at the terminals of a PV device may directly feed small loads such as lighting systems and DC motors or connect to a grid by using proper energy conversion devices this photovoltaic system consists of three main parts which are PV module, balance of system and load. The major balance of system components in this systems are charger, battery and inverter.

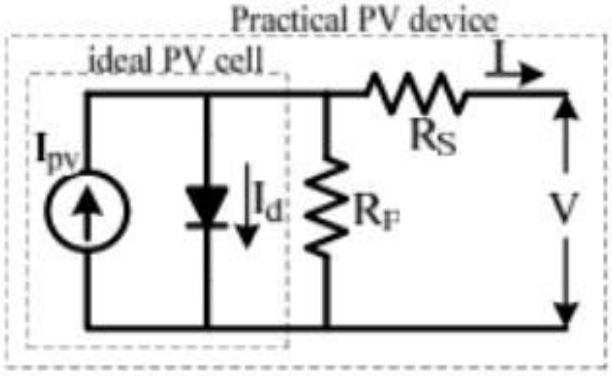

Fig.5 Practical PV device

A photovoltaic cell is basically a semiconductor diode whose p–n junction is exposed to light. Photovoltaic cells are made of several types of semiconductors using different manufacturing processes. The incidence of light on the cell generates charge carriers that originate an electric current if the cell is short circuit ed1

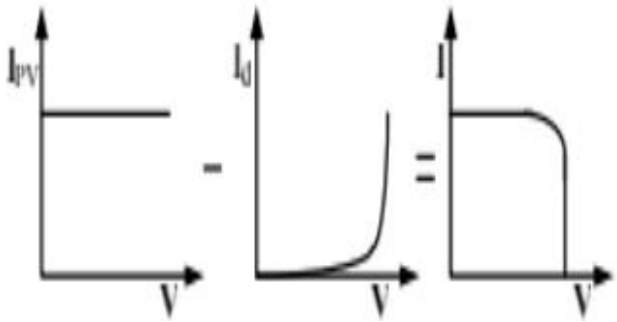

Fig.6. Characteristics I-V curve of the PV cell.

The equivalent circuit of PV cell is shown in the fig.5. In the above figure the PV cell is represented by a current source in parallel with diode. Rs and Rp represent series and parallel resistance respectively. The output current and voltage form PV cell are represented by I and V. The I-V characteristics of PV cell are shown in fig.6. The net cell current I is composed of the light generated current IPV and the diode current ID.

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V. MATLAB/SIMULINK RESULTS

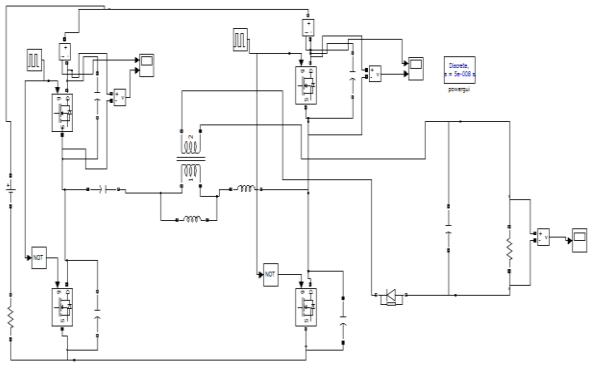
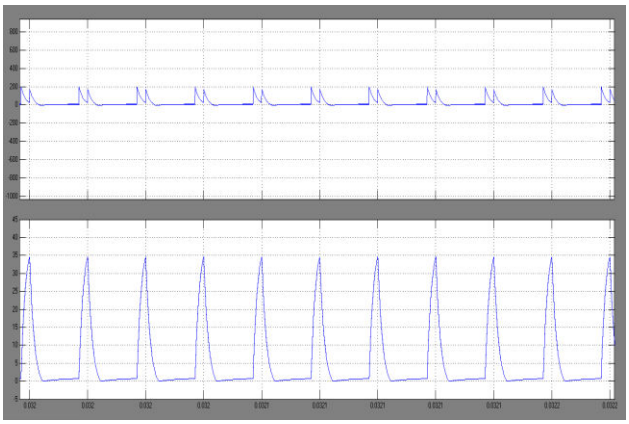
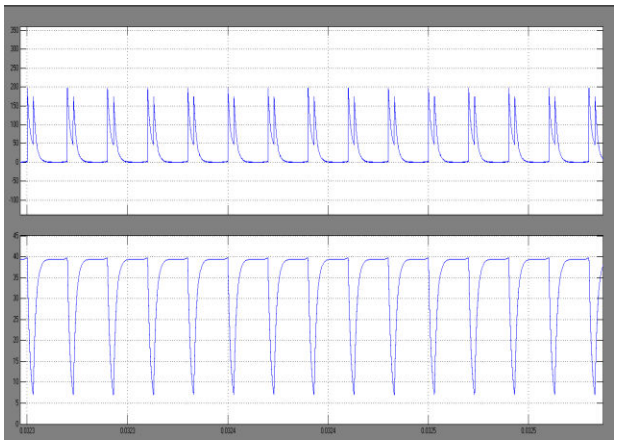


Fig.7 MATLAB/SIMULINK circuit of the proposed APWM full-bridge converter



(a)



(b)

Fig. 8.Experimental waveforms for ZVS turn-on of the switchesS1and S2 at V_d=40V and Po= 400W. (a) $V_{S1}$and i_{S1}. (b) V_{S2} and is2

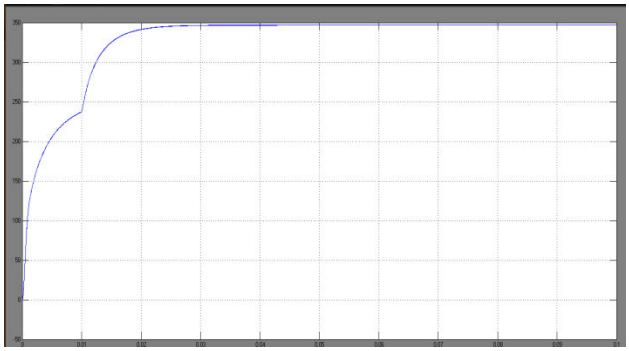
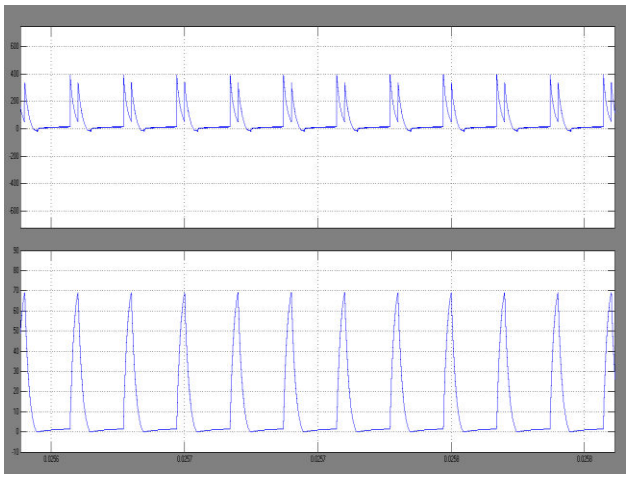
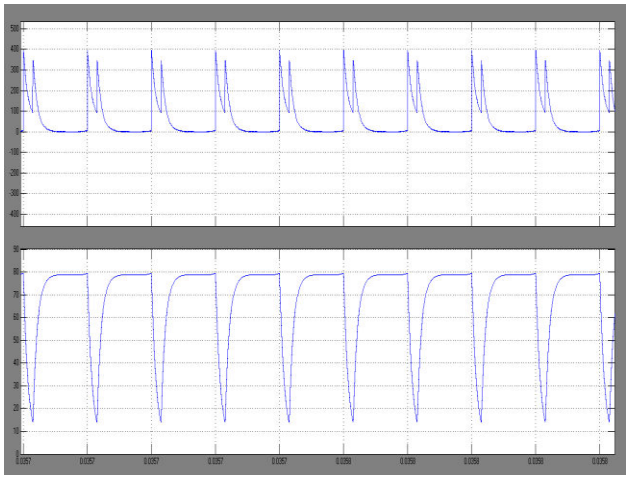


Fig.9 Output voltage waveform



(a)



(b)

Fig.10. Simulation waveforms for ZVS turn-on of the switches S1 and S2 at Vd = 80 V and Po = 400 W. (a) vS1 and iS1. (b) vS2 and iS2.

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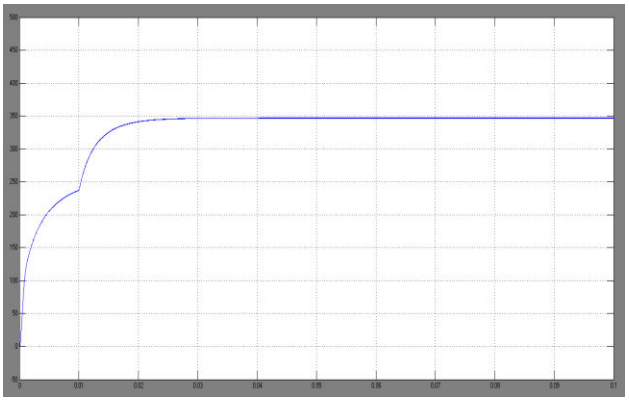

Fig.11.Simulation results for proposed converter output Voltage

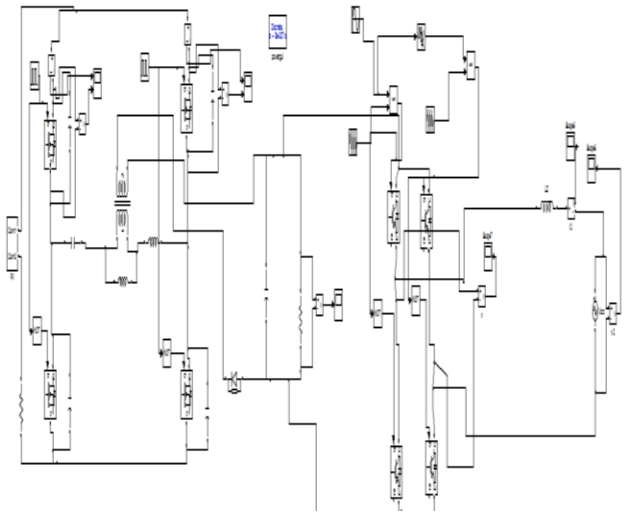

Fig.12 MATLAB/SIMULINK circuit of the proposed PV fed APWM full-bridge converter with AC grid connected system

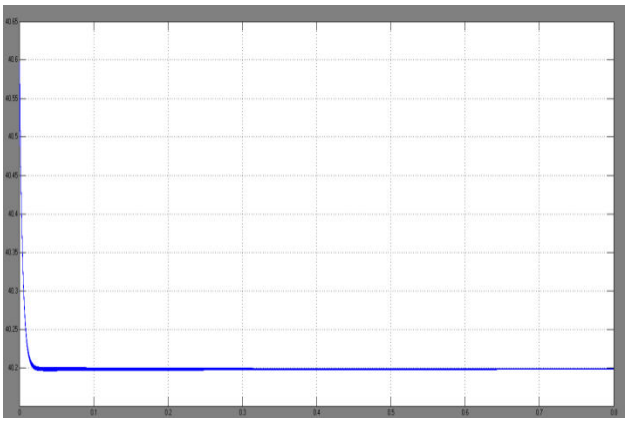

Fig.13 Simulation waveform of PV output voltage

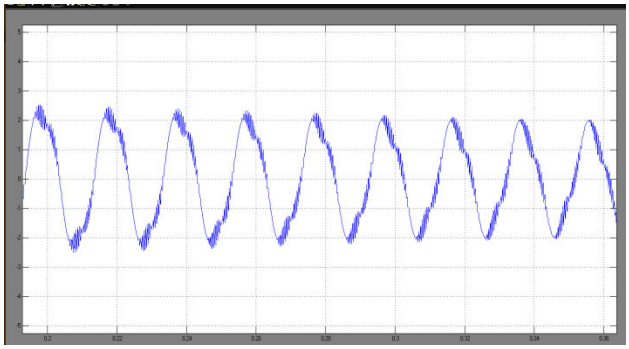

Fig.14 Output waveform of Grid current

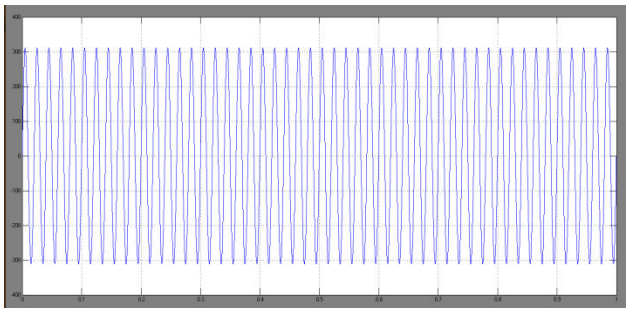

Fig.15 Output waveform of Grid voltage

VI. CONCLUSION

In this paper, the zvzcs asymmetrical full bridge converter with high voltage gain is interfaced with a PV module. The converter is able to provide a high efficiency and high-voltage gain with relatively low transformer turns ratio. The ZVS of all power switches and ZCS of the output diodes are achieved. Therefore, the converter is suitable for high-voltage applications. In this paper, both dc and solar energy sources are used as input source. And from both the result high voltage gain and high efficiency is obtained. So in this highly energy concerned world effective utilization of solar energy with this concept of converter can be used for many applications. This paper proposes a solar power generation system to convert the DC energy generated by a solar cell array into AC energy that is fed into the utility. The MLIs are very beneficial as the number of switches in

inverter increases this increases the level of inverter the harmonics distortion in AC output voltage and current decreases, it also provide reactive power compensation to the AC grid and reduction in electromagnetic emissions because they operate on lower switching frequency. The proposed solar power generation system is composed of a DC/DC power converter and an inverter. Inverters an attractive solution for grid-connected PV inverters.

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