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# DESIGN AN EFFICIENT REVERSIBLE MULTIPLIER ARCHITECTURE BASED ON NS GATE

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**ABSTRACT:** Multiplier forms a significant unit in several arithmetic logical functions. Modular multiplier has been developed as the highly crucial and well-organized circuit for binary addition. Their specific configuration and execution performance is highly feasible for fabricating a VLSI chip. In this project design an efficient reversible multiplier architecture based on NS gate is implemented. The performance of modular multiplier is estimated by calculating some parameters are known as delay, number of gate count/Transistor Count (area). To generate a useful function of gate, the reversible gates need some sustained auxiliary inputs. Also for maintaining the reversibility of the circuits some additional unutilized outputs are necessitate that are mentioned to as the garbage outputs. In this NS gate is used to determine the logic function. The multiplier speed in digital signal processing applications should be very high. Here in this project we analyzed the performance of reversible multiplier architecture based on NS gate by computing test parameters several times.

**KEY WORDS:** **NS Gate, Reversible gate, Reversible multiplier, Register.**

## I.INTRODUCTION

Multiplication is the major function in the four elementary functions such as multiplication, subtraction and so on. In any digital system, addition is very important operation [4]. It is primary operation which is useful to implement all the other arithmetic functions. For designing a fast, accurate and low power consumed adder [2] directly increases the device speed. This adder can also be used for faster computational applications as well as to improve overall the system life. The Arithmetic and Logic unit is the main block of digital systems like Digital Signal Processors (DSP), microprocessors, microcontrollers, and other data processing units [6]. In many arithmetic functions, an multiplication is an important element as hardware Unit for all the other applications.

The addition function is also used in various other functions like decoding, encoding and so on. Generally, addition is a function of adding two numbers which produces the output known as the sum and the carry. All the complex adder structures are developed using Half Adder (HA) and Full Adder (FA) only.

The reversible computing process is isolated to the unknown external environments. Hence the laws of physics will be describe in the interaction of the systems to evaluate the process. The main motivation to implement the reversible computing process is to improve the energy efficiency. And to predict the computing process in potential way. Generally, this concept was taken from the fundamentals of reversible computing is introduced by von Neumann-Landauer. It

consists of certain limit to dissipate the energy and he proposed the physically reversible computing process. Coming to Rolf Landauer of IBM, he proposed the logically reversible computing process. In the physically reversible computing process, the system will eliminate the n bits of information by using thermodynamic entropy. Next in logical reversible process the transition function will map the old computational states. This process will use the one to one mapping functions. This is unique distributed in an economic way. This mainly defines the input logic states in effective way.

The complete basic function of adder is constructed using a Half Adder and it can be improved by a Full Adder. The carry bit which is obtained in the addition process is very important in the design of an adder and also decides the speed of the adder. To reduce the time delay of the propagated Carry, multiple adders are designed. Binary adder is one of the significant modules of microprocessors. It is not only used to complete addition and subtract functions, but also can be used to achieve multiplication functions and so on. Some of the mostly used adders are CLA [1], Manchester Chain Adder, Carry Select Adder and Parallel Prefix Adder.

Designing of an adder consists lot of constraints. The trade-off between the delay and the area is the important factor. Usually adder requires very less area that is why it is easy to implement, but the time taken to give the result is high. To overcome this, advanced techniques are coming in to picture. Now a day's including the speed, the power consumption is also a considerable parameter. So the design of an adder is useful to satisfy all the specifications [5].

Binary addition is the basic function that continuously plays a considerable effect on the modern-day digital system design like control systems and DSP circuits. Various types of adders are available in which each one has its own importance and performance. Selection of an adder is based on the specific use of that. Therefore, binary adders are needed to have fast computation time, high efficiency, less area and low power consumption.

Binary adder [3] is the most important element in any digital system and it determines the performance of that digital system. It is used in many applications like arithmetic and logic units, multipliers, memory addressing units and dividers. Implementation of binary adder with advanced technology improves the overall performance of the device as well as entire system. The main disadvantage of this adder is the carry chain. The number of input bits available at the input of the adder increases the length of the carry chain. To increase the efficiency of the carry propagate adder, it is need to extent the carry chain without eliminating it. So, most of the digital designers now a day's came with high speed adder by advancing the architecture of computer which tends to keep the critical path in many calculations. In this paper we mostly concentrated on the designing of an adder with high speed, device utilization and usage of cell.

## II. EXISTED SYSTEM

The below figure (1) shows the architecture of existed system. The existed system designed an accuracy-configurable adder by masking the carry propagation at runtime. This adder accomplishes the actual function of delivering an unbiased trade-off amid

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power and delay with no loss of reliability. In general, a CSA has of three parts:

(1) half adders for carry production (G) and ropagation (P) signals preparation,

(2) carry save adder units for carry generation, and

(3) XOR gates for producing final sum

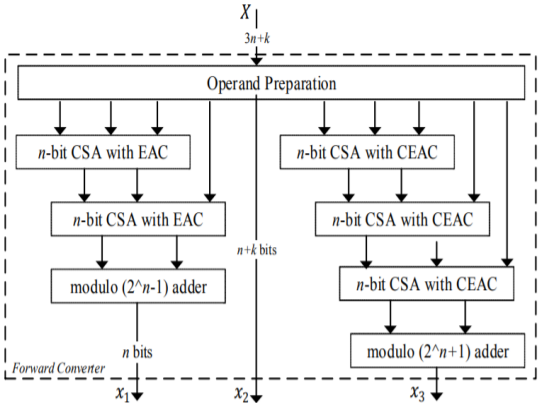


**Fig. 1: EXISTED SYSTEM**

We concentrate on the half adders for G and P signals groundwork in part 1 Note that owing to exploit the circuit of Ai XOR Bi for Si production, here Pi is indicated as Ai XOR Bi in its place of Ai OR Bi. As C0 is same as G0 , if G0 is 0, C0 will be 0. From (2), we find that C1 is equal to G1 when C0 is 0. In other words, if G0 and G1 are equal to 0, C0 and C1 will be 0. By expanding the above to i , Ci will be 0 when G0, G1, … , Gi are all 0. This means that the carry propagation from C0 to Ci is masked. From (3.1 hen M_Xi = 1, the exact sum Si and carry Ci will be 0 and 1 ({Ci , Si} = {1,0}); when M_X0 , M_X1 , … , M_Xi are all 0, Si is equal to Pi (= Ai XOR Bi = 0) as an approximate sum and Ci is equivalent to 0 ({Ci , Si} = {0, 0}) as conferred above. Here {,} denotes concatenation.

This denotes that the variation amid the exact and estimated sum is 2. Headed for improved reliability results for the estimated sum, we use an OR operation as an alternative to an XOR operation for P production when M_X = 0. hence, the disparity will be decreased to 1. A 2-input XOR gate can be developed by using a 2-input NAND gate, a 2-input OR gate, and a 2-input AND gate.), we can obtain that Si is similar to Pi when Ci-1 is 0. From the standpoint of near computing, if G is controllable and can be controlled to be 0, the carry propagation will be masked and S (=P) can be taken as an fairly accurate sum. The other way of perception, we can get hold of the selectivity of S amid the accurate and approximate sum if we can control G to be A AND B or 0. But this system doesn't gives effective results in terms of area, delay and speed. Hence a new system is proposed which is discussed in below section in detail manner.

## III. PROPOSED SYSTEM

The below figure (2) shows the architecture of proposed system. Input 'A' and input 'B' are saved in the register. n/2 multiplier will take the data from register. Multiplied data will given to NS gate adder and transferred to the CSA tree. The obtained data will save in the register.

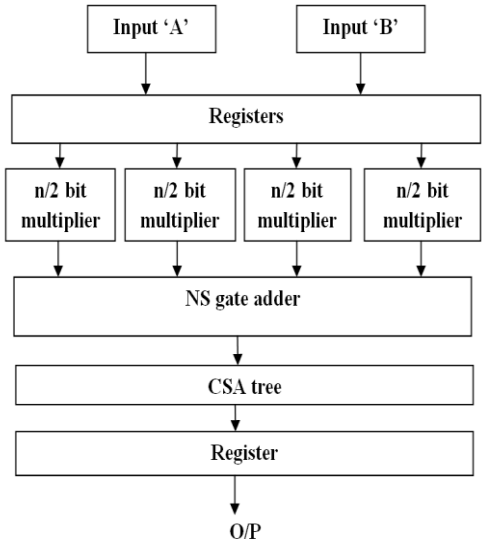


**Fig. 2: BLOCK DIAGRAM OF PROPOSED ADDER**

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The input are termed as input terminal respectively and the output are termed garbage outputs It can be established from the Truth Table that the input pattern analogous to a particular output pattern can be exclusively determined. The proposed NSG gate can perceive all Boolean logical operators. Here the inputs are obtained from memory location and given to NS gate. Since the bits are vast and also ripple carry adder produces all the output values in parallel. The both input and output bits are taken in parallel. The register is taken out or fed back as one of the input to the ripple carry adder. Reversible adder circuit is intended for addition binary logics. Sum signal (SUM) and garbage outputs are the outputs of the proposed system. Most important arithmetic operation performed almost in all digital signal processors and systems is addition operation. Addition is involved in all digital signal and data processing. Thus performance of a system completely depends upon the performance of its reversible adder unit. The speed, power consumption and area of a proposed system define performance of a system. adders are utilized to implement any operation because these are fast, reliable and efficient components. These are of number of types and depending upon the application a specific type of adder is chosen. In a simple way addition is a process of adding an integer.

The most important and the purpose of the prominent in the proposed gate is the work singly as the reverse for the reversible adder, we proposed the reverse adder in a number. NS gates are better than the previous gates for the full adders in the design, the reverse adder circuits of all are proposed till now. The only reversible gate is required for the proposed reversible adder by using the NS gate and it produces only garbage outputs while performing operations like full adder, full subtractor, and half adder. A part from these they are the other reversible gates proposed till now the NS gate can also be singly performs the functions from the full subtractor, half adder, and half subtractor with only the garbage outputs. Hence compared to other gates this proposed system provides effective results.

## IV. REULTS

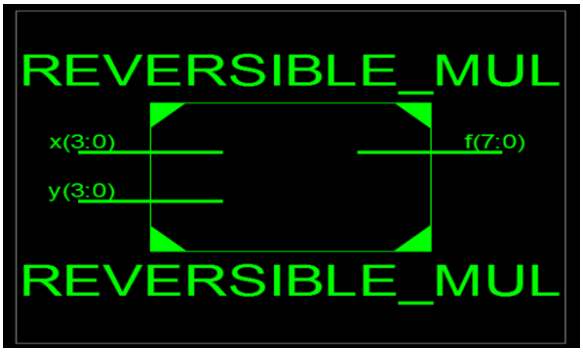


**Fig. 3: RTL SCHEMATIC**

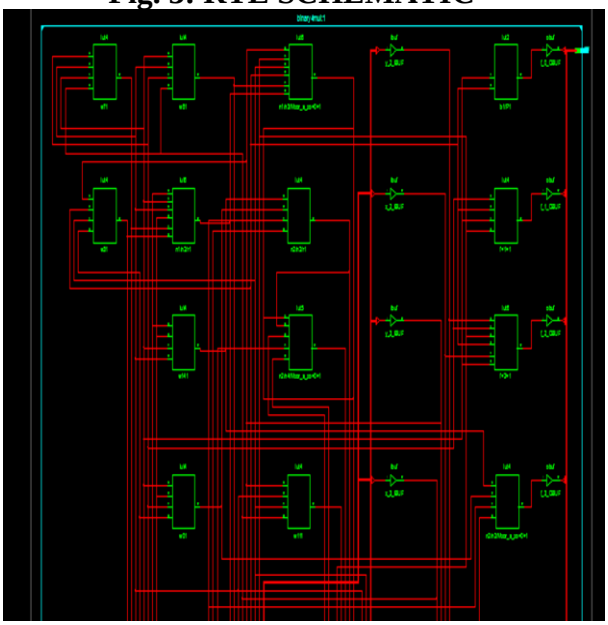

**Fig. 4: TECHNOLOGY SCHEMATIC**

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**Fig. 5: OUTPUT WAVEFORM**

## V. CONCLUSION

Design an efficient reversible multiplier architecture based on NS gate was implemented. Modular multiplier is constructed using various design méthodologies. Variable latency adder performance basically relies on prefix-processing stage. The digital signal processing for the most frequently used a computational unit and multimedia applications is a adder. NS gate is used to determine the logic in the system. In terms of hardware complexity, number of gates, garbage outputs and constant inputs and for the proposed adder. Hence the proposed system gives effective output.

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