Implementation of Dual Modulus Prescaler in True Single Phase Clock (TSPC)

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Abstract – A high speed CMOS divide-by-16/17 dual modulus prescaler has been designed using 250 nm CMOS technology. It consists of the pseudo divide-by- 2/3 prescaler and an asynchronous divide-by-8 prescaler, which are all implemented in TSPC structure. The speed of the divide-by-16/17 dual modulus prescaler is enhanced by decreasing its delay. It is achieved by means of adapting a pseudo divide-by- 2/3 prescaler and by changing the connections between the TSPC D flip-flops. By adapting a pseudo divide-by- 2/3 prescaler and by changing the connection between TSPC D flip-flops, the minimum working period is reduced by about half a NOR gate's delay and by an inverter's delay respectively. The operating frequency is simulated to be up to 5.8 GHz.

I. INTRODUCTION

A prescaler is a counting circuit which is used to reduce a high frequency signal to a lower frequency signal by doing some integer division. The prescaler takes the values in powers of 2 or

some fixed values or some integer value from 1 to 2^P, where P is the number of prescaler bits.Prescalers are widely used at very high frequency to extend the upper frequency range of frequency counters, phase locked loop (PLL) synthesizers, and other counting circuits. When prescaler is used in conjunction with a PLL, it introduces a undesired change between the frequency step size and phase detector

frequency. Therefore, it is necessary to either restrict the integer to a small value or to utilize a dual modulus prescaler.A dual-modulus prescaler is a prescaler that selectively divides the input frequency by one of two integers, such as 16 and 17. When the dual modulus prescaler is implemented in TSPC structure, single clock phase, low power and small area can be obtained. A structure of True Single Phase Clock (TSPC) Dflip- flop is shown in fig.1. The setup time of Fig.1.can be written as

$$T_{setup} = t_{D\_A}$$

Here tD_A represents the propagation time from node D to A, which is a clocked inver ters

delay.The propagation delay of the TSPC DFF can be written as

$$T_{D\_QN} = t_{A\_B} + t_{B\_QN} \quad T_{D\_Q} = t_{A\_B} + t_{B\_QN} + t_{QN\_Q}$$

Where TD_QN and TD_Q are the propagation delay from clk to QN and Q respectively. tA_B, tB_QN , tQN_ Q represents the propagation delay from node A to B, B to QN, QN to Q respectively. An advantage of TSPC circuit is single clock

phase, low power, small area, large output swing, high robustness and reduction of logic depth. The optimized design is to employ only one AND/OR logic gate before one TSPC DFF. The design rules of TSPC circuits are as

follows:

1. The AND/OR logic should be embedded in the first stage but not other stages.
2. No two paths should control one node to avoid glitches and conflictions.

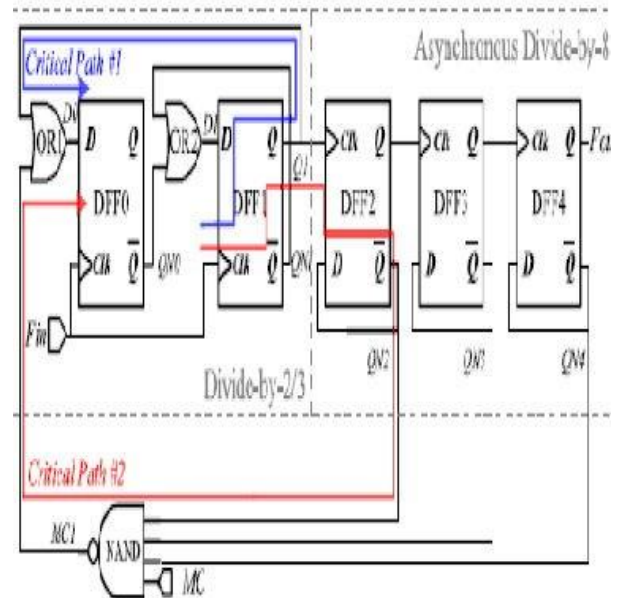## II. CONVENTIONAL DIVIDEBY- 16/17 DUAL MODULUS PRESCALER

Fig.2. Schematic of conventional divide-by-16/17 prescaler

Fig.2.shows the schematic of a conventional divide-by-16/17 dual modulus prescaler based on divide-by-2/3 divider. Divide-by-2/3 prescaler is followed by an asynchronous divide-by-8 prescaler which produces the output unction of divide-by-16/17 prescaler. It has two critical paths.

1. Critical path #1 comes through DFF1 and OR1.

2. Critical path #2 comes through DFF1, DFF2, NAND , OR1 Signals must pass through path #1 within a period of Fin and the signals must pass through path #2 within two periods of Fin. Since OR1 and OR2 gates can be absorbed into the TSPC DFFs, the minimum working period can be written as

$$T_{min,con} = \max \left\{ \begin{array}{l} t_{d\_Q,DFF1} + t'_{setup,DFF0} \\ \dfrac{t_{d\_Q,DFF1} + t_{d\_QN,DFF2} + t_{d,NAND} + t'_{setup,DFF0}}{2} \end{array} \right\}$$

Where td_ Q, DFF1 represents the propagation delay from clk to Q1 of DFF1. td_ QN, DFF2 represents the propagation delay from clk to QN2 of DFF2. t'setup,DFF0 represents the setup time of the DFF0 with absorbed OR1 and tD _NAND is the NAND gate delay.

1. A new pseudo divide-by-2/3 prescaler is used which accomplish a single but not continuous divide-by-3 operation in a cycle.

2. The connections are interchanged between the TSPC D flip flops (i.e., the clk input to the asynchronous divide-by-8 prescaler is given from the QN instead of Q of pseudo divide-by-2/3 prescaler) so that the delay decreases from tD_Q to tD_QN. The operation mode of the proposed circuit is as follows:

1. When modulus control MC=1, the pseudo divide-by-2/3 prescaler accomplishes seven times of divide-by-2 operation and one time of divide-by-3 operation in a cycle. Therefore the circuit operates in divide-by-17 mode.

2. When MC=0, the pseudo divide-by-2/3 prescaler accomplishes only divide-by-2 operations in a cycle. Therefore the whole circuit operates in divide-by-16 mode. In theory, it is difficult to estimate which path decides the minimum working period. The optimized design is to make the critical path #1 approximately equal to half length of critical path #2.

Therefore the minimum working period of conventional divide-by-16/17 prescaler can

be written as Tmin,con = (1/2) tD_Q,DFF1 + tD_QN,DFF2 + tD ,NAND +t'setup, DFF0 (1) These two critical paths should be optimized to achieve high speed which is a great challenge for designers.

The critical path is optimized by replacing the OR and NAND gate by AND gate in the proposed

system. This reduces the propagation delay which in turn decreases the minimum working period of the prescaler. The reduction of working period in proposed system is achieved by decreasing its delay. The delay is decreased by adopting a pseudo divide-by-2/3 prescaler and changing the interconnection between the TSPC D flip-flops.

III. PROPOSED DIVIDE-BY-16/17 DUAL MODULUS PRESCALER
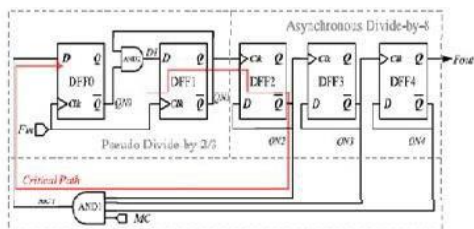

Fig.

The main changes from the conventional prescaler.

The maximum working frequency of the proposed system is decided by its divide-by-17 operation mode. The key operation in

divide-by 17 mode is the divide-by-3 operation of pseudo
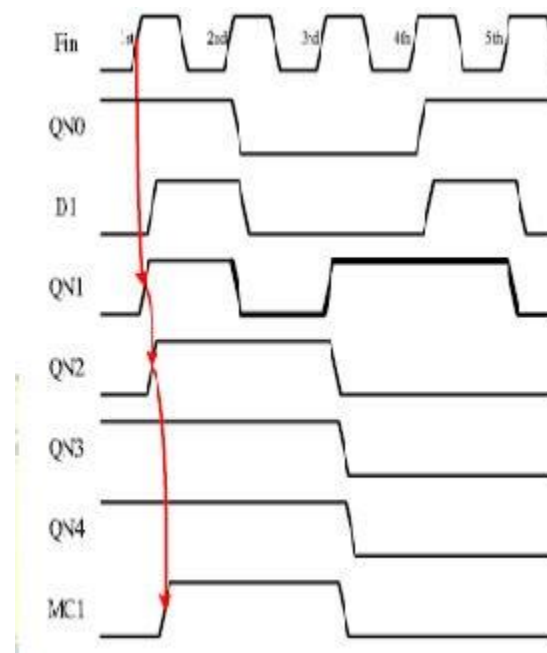
divide-by-2/3 prescaler.

Fig.4. Timing diagram of proposed divide-by- 16/17 prescaler

Fig.4. shows the timing diagram of divideby- 3 operation of the proposed circuit. The operation of the timing diagram is as follows:

i. In the first rising edge of Fin, QN1 and QN2 switch to high. So MC1 switches to high and holds for two periods.

ii. In the second rising edge of Fin, QN0 and D1 switch to low and hold for two periods.

iii. In the third rising edge, QN1 switches to high and holds for two periods. From the second to fifth rising edge of Fin, DFF1 outputs a divide-by-3 signal in node QN1 and pseudo divide-by-2/3 prescaler accomplishes a divide-by-3 operation. After this, the pseudo divide-by- 2/3 prescaler will carry out seven times divide-by-2 operation. A divide-by-17 signal is obtained in node Fout. The minimum working period of the proposed prescaler can be written as Tmin,pro = (1/2) tD_QN,DFF1 + tD_QN,DFF2 + t"setup, DFF0 operation of dual modulus prescaler. When MC=1, dual modulus prescaler divides the clock frequency by 17. When MC=0, it operates in divide-by-16 Here the delay is calculated in simulation which is in the range of μs. (2) Where tD_QN,DFF1 is the propagation

delay from clk to QN1 of DFF1. tD_QN,DFF2 is the propagation delay from clk to QN2 of DFF2. t"setup, DFF0 is the setup time with absorbed AND1 gate. From equations (1) and (2) , it is clear that the minimum working period of the proposed divideby- 16/17 prescaler is reduced by half an inverter's delay and half a NOR gates delay. Therefore the difference in delay between conventional and proposed divide-by-16/17 prescaler circuit can be written as

$$Tmin,con - Tmin,pro \approx T_{D\_NOR} + \frac{T_{D\_INV}}{2}$$

By adopting a Pseudo divide-by-2/3 prescaler, the minimum working period is reduced by half a NOR gate's delay. By changing the connection of TSPC DFF's, the minimum working period is further reduced by half an inverter's delay. and half an inverter's delay is decreased by adopting pseudo divide-by-2/3 prescaler and by changing the connections between TSPC D flip flops.

RELATED WORK

As far as, the proposed system was only concerned with the delay and speed. My future work is to design the prescaler with low power consumption and to increase the frequency range up to 12 GHz and to further implement it in the fractional N-PLL frequency synthesizer to achieve accurate phase and frequency comparisons.

IV. SIMULATION RESULTS
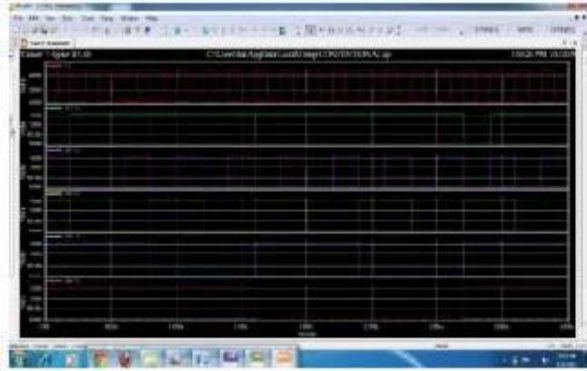
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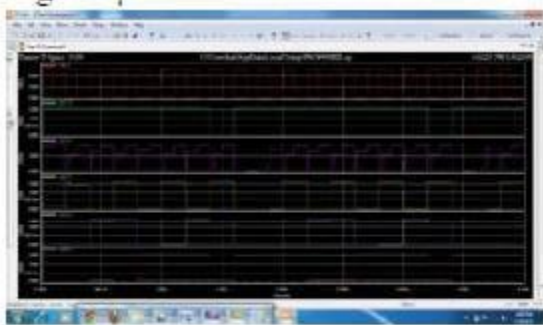

Fig.5. Output of existing system

The dual modulus prescaler was simulated using 250 nm CMOS technology.Fig.5 shows the

output of existing system. It also reveals the

Fig.6. Output of proposed system

Fig.6 shows the output of proposed system. The operating frequency range can be simulated up to 5.8 GHz. The delay calculated in the simulation is found to be in the range of ns which is smaller compared to the existing system. The minimum working period is reduced in the proposed system is 3.48 secs. Therefore, this guarantees that the working period of the proposed prescaler is reduced than the existing conventional system.

V. CONCLUSION

A high speed dual modulus prescaler has been designed using 250 nm CMOS technology. Pseudo divide-by-2/3 prescaler reduces the minimum working period by half a NOR gate's delay. By changing the connection between TSPC D Flip flops, its minimum working period is reduced by about half an inverter's delay. Therefore the speed of the proposed system is enhanced by adopting pseudo divide-by-2/3 prescaler and by changing its interconnection between the flip flops. The operating frequency is also simulated to be up to 5.8 GHz with low delay.

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