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A MODIFIED SWITCHING PATTERN FOR THREE PHASE SEVEN LEVEL CHB INVERTER FED INDUCTION MOTOR DRIVE

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ABSTRACT-In this paper a modified Switching pattern for 7 level Cascaded H Bridge Inverter is presented. Basically Inverter is a device that converts DC power to AC power at desired output voltage and frequency. Demerits of inverter are less efficiency, high cost, and high switching losses. To overcome these demerits, we are going to multilevel inverter. Though the multilevel inverters hold attractive features, usage of more switches in the conventional configuration poses a limitation to its wide range application. Cascaded multilevel inverter has the advantage of most reliable and to achieve the best fault tolerance owing to its modularity; a feature that enables the inverter to continue operating at lower power levels after cell failure. Modularity also permits the cascaded multilevel inverter to be stacked easily for high power and high voltage applications. Therefore, a renewed 7-level multilevel inverter topology is introduced switching pattern of cascaded H bridge inverter topology is analyzed through thermal module of power electronic switches thereby ensuring the minimum switching losses, reducing size and installation cost. The proposed inverter provides higher output quality with relatively lower power loss with the induction motor drive. The performance and results are evaluated by using Matlab/Simulink software.

Keywords: Cascaded H bridge multilevel inverter, switching and conduction losses,Induction motor.

I. INTRODUCTION

In recent years, power electronics engineershave paid great attention to multilevel inverters as a new kind of power converter. Most multilevel inverters have an arrangement of switches and capacitor voltage sources. By a proper control of the switching devices, these can generate stepped output voltages with low harmonic distortions [1-2]. These multilevel inverters are widely used in manufacturing factories and acquired public recognition as one of the new power converter fields because they can overcome the disadvantages of traditional inverters. Multilevel inverters can be divided into three remarkable topologies: diode clamped, flying capacitors, and cascaded H-bridge cells with separate DC sources [3].Now, inverters are static power electronics device which is converts dc input voltage to ac output voltage with the desired magnitude and frequency. The output voltage waveforms of ideal inverters should be sinusoidal. But in practically it is square-wave or quasi-square-wave [4]. The multilevel voltage source inverters unique structure allows them to reach

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medium voltages and high power levels without use of transformers. They are especially suited to high voltage vehicle drives where low output voltage total harmonic distortion (THD) and electromagnetic interference (EMI) are needed. The general function of multilevel inverter is to synthesize a desired voltage from several levels of dc voltages [5-7]. Basically, there are three types of multilevel inverter topologies i. e. Diode clamped, Flying capacitor and cascaded h-bridge MLI. Out of that, the cascaded h-bridge MLI topology is beneficial because in that topology the circuit complexity and layout is simple also there are no extra components are required like clamping diode or flying capacitor compare to diode clamped and flying capacitor MLI topology [8-10].Essentially, there are four sorts of losses in multilevel inverter, which are: conduction loss, switching loss, OFF state loss and gate loss. The OFF state and gate loss are little and typically ignored [11]. Hence, in this paper only switching and conduction losses are considered through entire analysis.

II. MULTILEVEL INVERTERS

Multilevel inverter presents a sine wave output with many DC levels along time period as shown in Fig.1. Commonly used topologies for multilevel inverter are flying capacitor, Cascaded H Bridge and Diode clamped. These topologies are having advantages as well limitation based on which selection of topologies for a particular application is done. Flying capacitor clamped inverters having less power losses but higher in weight and cost. Cascaded H Bridge inverters having less weight and cost on other edge high power losses as compared to other topologies. Diode clamped multilevel inverter stands in middle between capacitor clamped and cascaded H bridge multilevel inverters as far as cost, weight and power loss is concerned [4]. Diode clamped and capacitor clamped inverter requires large value of DC source input and also suffers from the problem of voltage balance across capacitor. Cascade multilevel inverters are having series connected H bridges with individual DC supply. It provides sinusoidal voltage as a sum of DC voltages generated by each cell. Cascaded multilevel inverter requires small DC source, less numbers of components as compared to diode and capacitor clamped inverters and also offers high quality output voltages due to these cascaded multilevel inverter finds its importance in medium voltage inverter market [5, 6].

III.Conventional switching pattern of 7 level cascaded H bridge inverter

Fig.2 shows configuration of 7 level cascaded H bridge inverter, where S1a, S2a, S3a, S4a, S1b, S2b, S3b, S4b, S1c, S2c, S3c, S4c are IGBT switches and D1a, D2a, D3a, D4a, D1b, D2b, D3b, D4b, D1c, D2c, D3c, D4c are their parasitic diodes respectively. Each H bridge is supplied through DC voltage of 'V' voltage, i.e. Va = Vb = Vc = V.

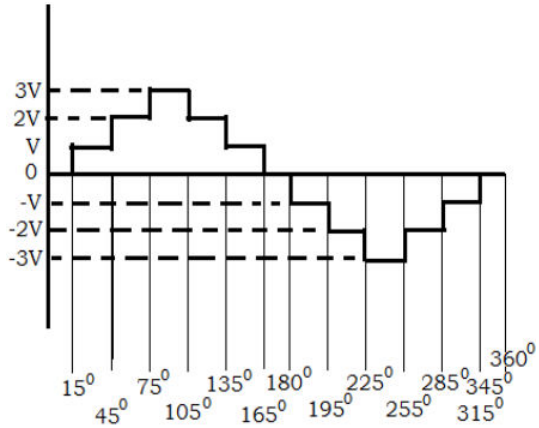

Fig.1.Stair case output voltage waveform.

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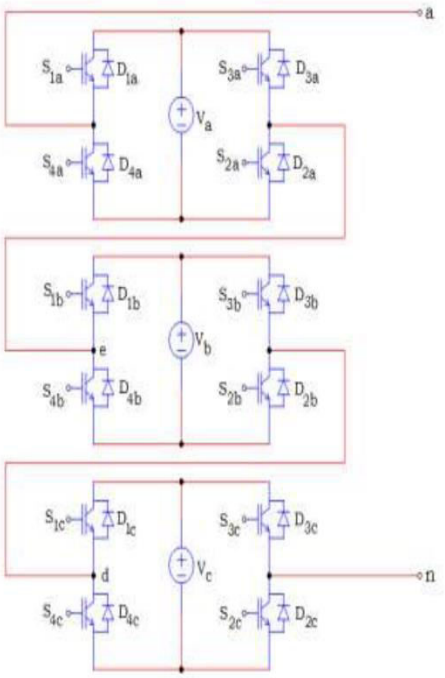

Fig.2 Configuration of 7 level Cascaded H bridge inverter.

Following switching combination synthesize 7 level voltage across 'a' and 'n'.

- For Van = 3V, S1a , S2a , S1b, S2b, S1c,S2c are turned on.
- For Van = 2V, S1a , S2a , S1b, S2b, S4c,S2c are turned on.
- For Van = V, S1a , S2a , S4b, S2b, S4c,S2c are turned on.
- For Van = 0, S4a , S2a , S4b, S2b, S4c,S2c are turned on.
- For Van = -V, S4a , S3b , S1b, S3b, S1c,S3c are turned on.
- For Van = -2V, S4a , S3b , S4b, S3b, S1c,S3c are turned on.
- For Van = -3V, S4a , S3b , S4b, S3b, S4c,S3c are turned on.

Table: 1 shows truth table of conventional switching pattern. Fig.1 shows stair case output voltage waveform in which each voltage level last for duration of 300.

Table: .1 conventional switching pattern

Switch	S1a	S2a	S3a	S4a	S1b	S2b	S3b	S4b	S1c	S2c	S3c	S4c
Interval												
0 - 15		1		1		1		1		1		1
15 - 45	1	1				1		1		1		1
45 - 75	1	1			1	1				1		1
75 - 105	1	1			1	1			1	1		
105 - 135	1	1			1	1				1		1
135 - 165	1	1				1		1		1		1
165 - 180		1		1		1		1		1		1
180 - 195	1		1		1		1		1		1	
195 - 225			1	1	1		1		1		1	
225 - 255			1	1			1	1	1		1	
255 - 285			1	1			1	1			1	1
285 - 315			1	1			1	1	1		1	
315 - 345			1	1	1		1		1		1	
345 - 360	1		1		1		1		1		1	

IV. Modification in switching pattern

It is must to operate switches S1a , S2a , S1b, S2b, S1c,S2c and S4a , S3b , S4b, S3b, S4c,S3c in order to get voltage level 3V and - 3V respectively in output voltage waveform/ there is no other alternative of switching pattern for voltage level 3V and -3V but for voltage levels 2V, V, -V, -2V there is as follows.

Voltage level: 2V

When switches S1a, S2a, S1b, S2b are turned on the negative terminal of Vb is brought to point'd', which makes D4c forward biased. By turning on S2c potential difference 2V can be provided across 'a' and 'n' without operating switch S4c. The modified switching pattern is S1a, S2a, S1b, S2b, D4c and S2c as shown in Fig.3.

Voltage level: V

When switches S1a, S2a are turned on the negative terminal of Va is brought to point 'e', which makes D4b forward biased. Turning on switch S2b, in turn makes D4c forward biased. Finally switch S2c brings the potential difference 'V' across 'a' and 'n', without operating switches S4b and S4c. The modified

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switching pattern is S1a, S2a, D4b, S2b, D4c,S2c as shown in Fig.4.

Voltage level:-V

When switches S4a, S3a are turned on the positive terminal of Va is brought to point 'e', which makes D1b forward biased. Turning on switch S3b the same con be provided to point'd' which in turn makes D1c forward biased and D4c reverse biased. Finally switch S3c bring the potential difference across 'a' and 'n'. The modified switching pattern is S4a, S3a, D1b, S3b, D1c,S3c.

Voltage level:-2V

When switches S4a, S3a, S4b, S3b are turned on the positive terminal Vb is brought to point'd', which makes D1c forward biased. Turning on switch S3c potential difference '-2V' is provided across 'a' and 'n' without operating S1c. The modified switching pattern is S4a, S3a, S4b, S3b, D1c and S3c as shown in Fig.6.The truth table of modified switching pattern for the same stair case output voltage is shown in Table: 2.

Table.2 Modified switching pattern

Switch	S1a	S2a	S3a	S4a	S1b	S2b	S3b	S4b	S1c	S2c	S3c	S4c
Interval												
0 - 15		1		1		1		1		1		1
15 - 45	1	1				1				1		
45 - 75	1	1			1	1				1		
75 - 105	1	1			1	1			1	1		
105 - 135	1	1			1	1				1		
135 - 165	1	1				1				1		
165 - 180		1		1		1		1		1		1
180 - 195	1		1		1		1		1		1	
195 - 225			1	1			1				1	
225 - 255			1	1			1	1			1	
255 - 285			1	1			1	1			1	1
285 - 315			1	1			1	1			1	
315 - 345			1	1			1				1	
345 - 360	1		1		1		1		1		1	

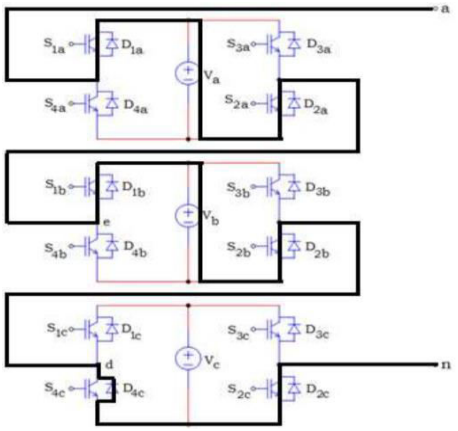

Fig.3 Modified switching for 2V voltage level.

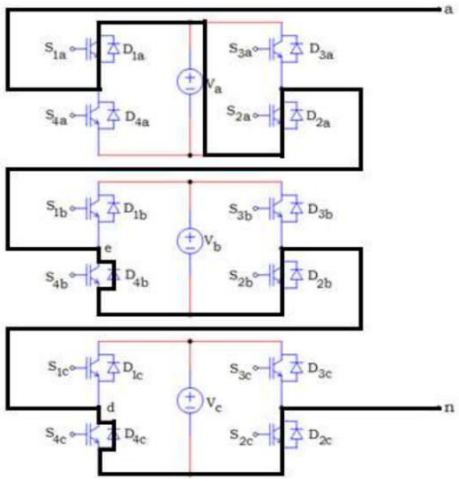

Fig.4 Modified switching for voltage level V.

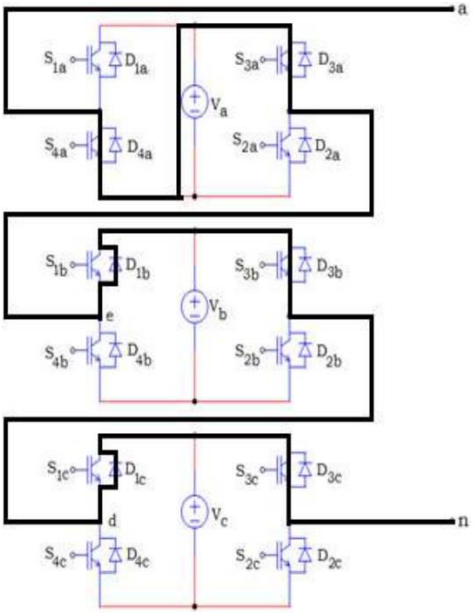

Fig.5 Modified Switching for voltage level '-V'

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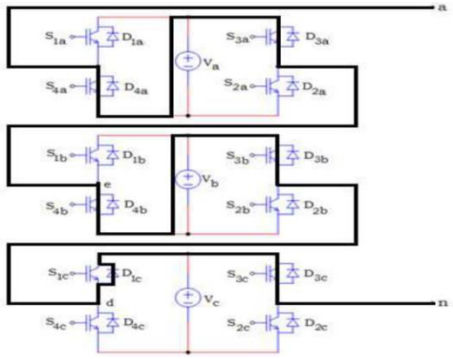

Fig.6 Modified Switching for voltage level '-2V'.

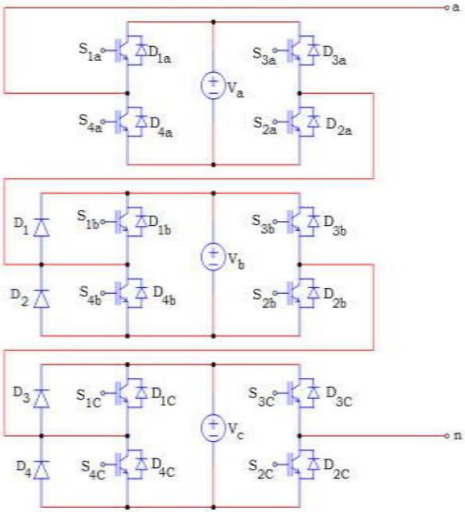

Fig.7 Modified topology of cascaded h bridge inverter

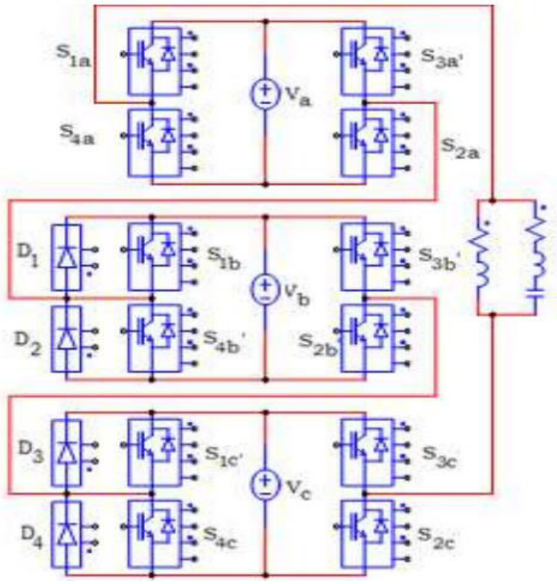

Fig.8 Test Circuit.

V. INDUCTION MOTOR

In recent years the control of highperformance induction motor drives for general industry applications and production automation has received widespread research interests. Induction machine modeling has continuously attracted the attention of researchers not only because such machines are made and used in largest numbers but also due to their varied modes of operation both under steady and dynamic states. Traditionally, DC motors were the work horses for the Adjustable Speed Drives (ASDs) due to their excellent speed and torque response. But, they have the inherent disadvantage of commutator and mechanical brushes, which undergo wear and tear with the passage of time. In most cases, AC motors are preferred to DC motors, in particular, an induction motor due to its low cost, low maintenance, lower weight, higher efficiency, improved ruggedness and reliability. All these features make the use of induction motors a mandatory in many areas of industrial applications. The advancement in Power electronics and semiconductor technology has triggered the development of high power and high speed semiconductor devices in order to achieve a smooth, continuous and low total harmonics distortion (THD). Three phase induction motors are commonly used in many industries and they have three phase stator and rotor windings. The stator windings are supplied with balanced three phase ac voltages, which produce induced voltages in the rotor windings due to transformer action. It is possible to arrange the distribution of stator windings so that there is an effect of multiple poles, producing several cycles of magneto motive force (mmf) around the air gap. This field

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establishes a spatially distributed sinusoidal flux density in the air gap. In this paper three phase induction motor as a load. The equivalent circuit for one phase of the rotor is shown in figure.9.

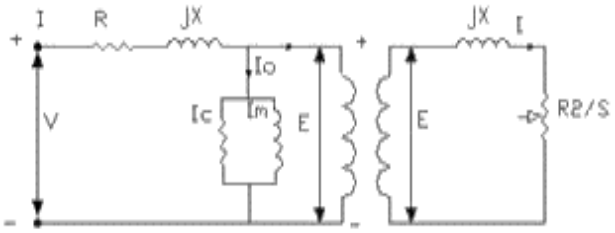

Fig. 9. Steady state Equivalent circuit of an induction
Motor.

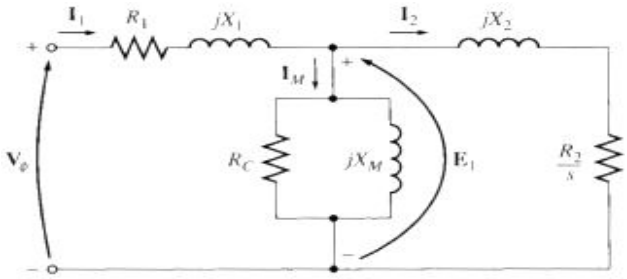

Fig.10. Equivalent circuit refer to stator.

The rotor current is

$$I_r = \frac{sE_r}{R_r + jX_r} = \frac{E_r}{\frac{R_r}{s} + jX}$$

VI. Modification in topology

The modified switching pattern makes switches S4b and S4c in positive half cycle of output waveform, and switches S1b and S1c in negative half cycle, to function as diode. This make conduction losses of the inverter to rise. This is compensated by connecting fast recovery diode in parallel with D4b, D4c, D1b, D1c as shown in Figure.3. As diode connected in parallel to parasitic diode offers least forward resistance majority ofthe load current is shared by parallel diode. Hence, the conduction losses are controlled.

Table.3 inverter losses

	In Watt
Conventional Cascaded H bridge Inverter (CHI) overall losses	160
Overall Losses in CHI with proposed modification	150
Reduction in overall losses attained	10

VII.MATLAB/SIMULATION RESULTS

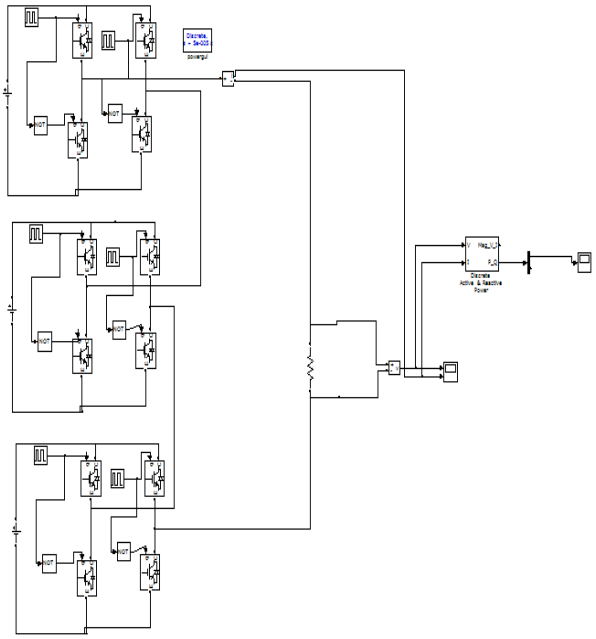

Fig.11.Matlab/Simulation Model of 7 level Conventional Cascaded H-Bridge Inverter.

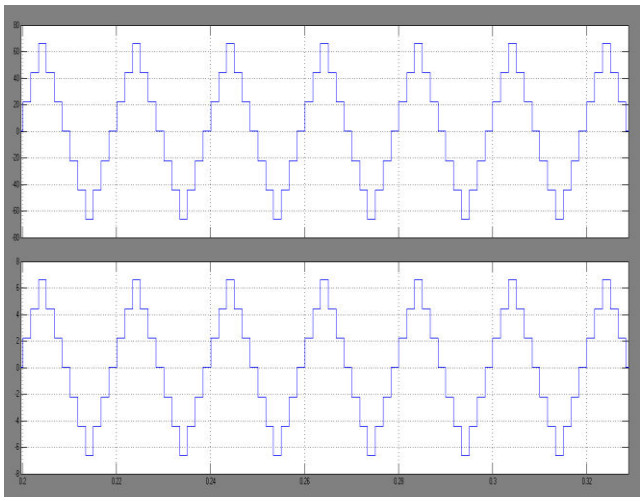

Fig.12.Simulation results for conventional inverter voltage and Current.

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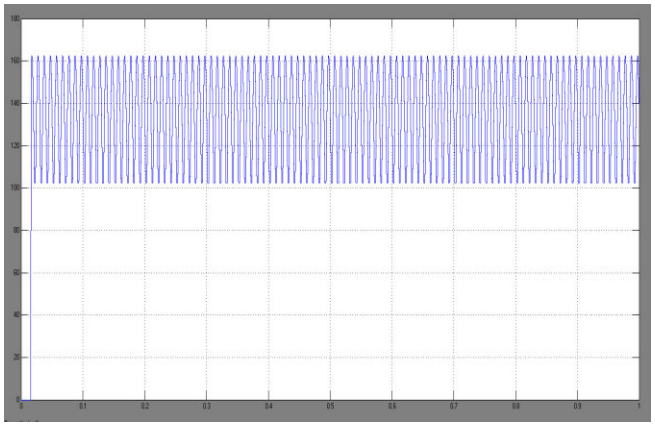

Fig.13. Power loss in conventionally switched Cascaded H Bridge inverter.

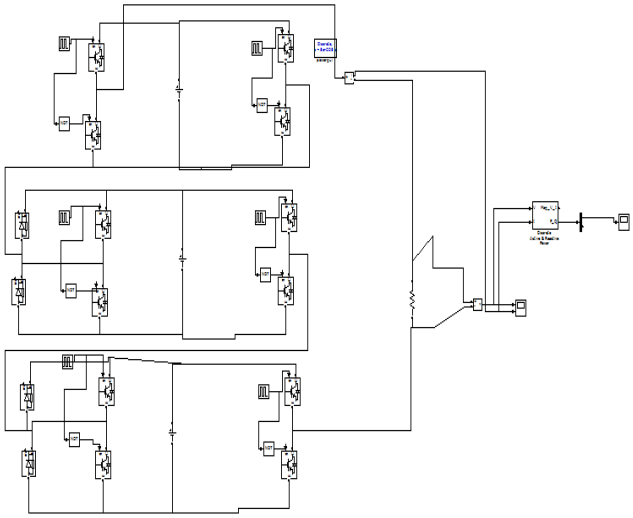

Fig.14.Matlab/Simulation Model of 7 level Proposed Cascaded H-Bridge Inverter.

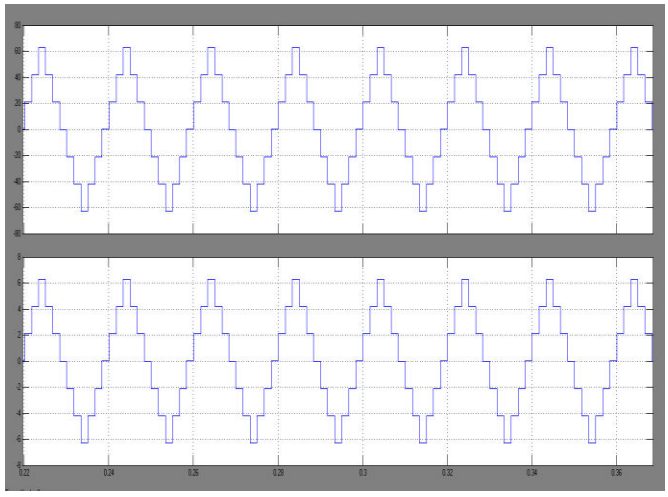

Fig.15.Simulation results for proposed inverter voltage and Current.

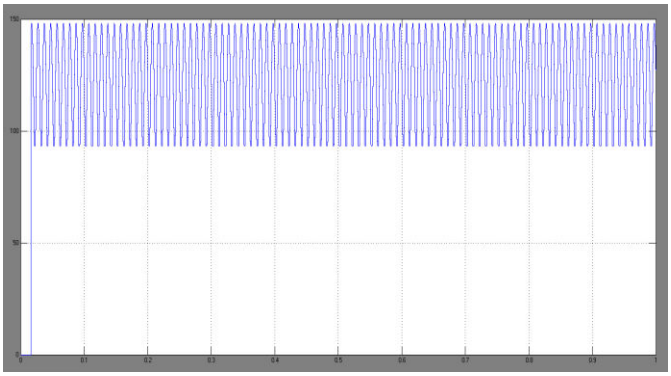

Fig.16.Power loss in Proposed switched Cascaded H Bridge inverter.

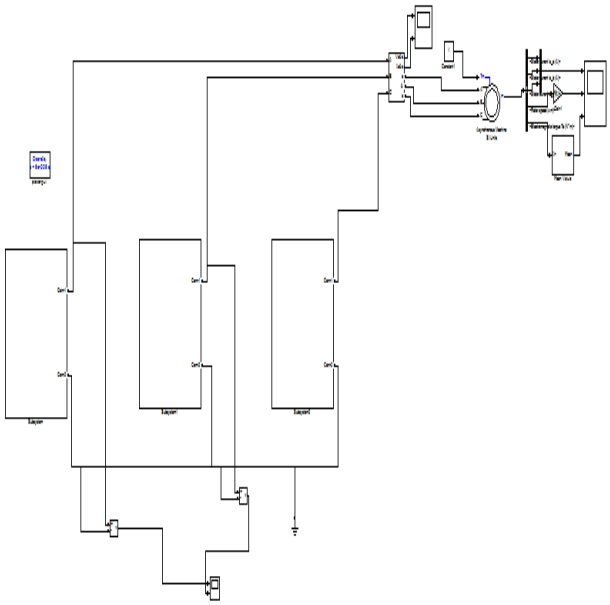

Fig.17.Matlab/Simulation Model of three phase 7 level Proposed Cascaded H-Bridge Inverter fed induction motor.

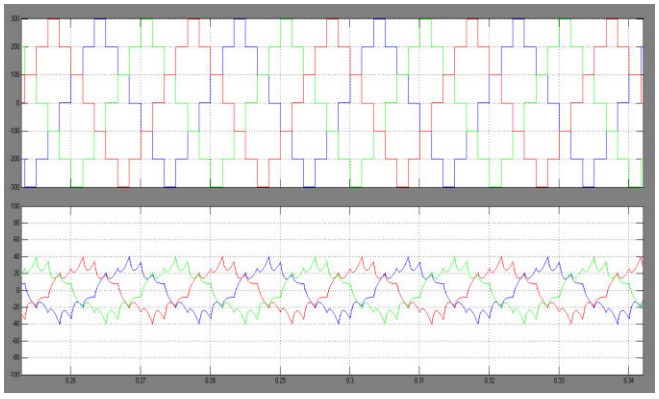

Fig.18.Simulation model of the three phase seven level inverter voltage and Current.

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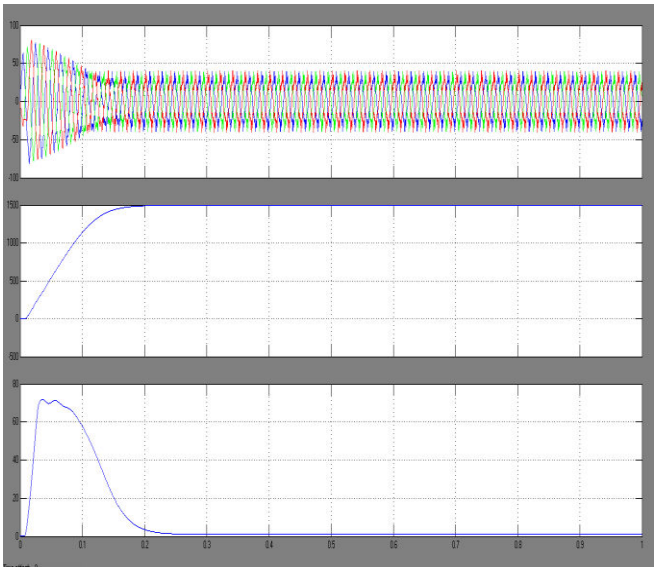

Fig.19.Stator Currents, Speed, Electromagnetic Torque.

VIII.CONCLUSION

We hereby conclude that Multi-level inverters are a very promising technology in the power industry. In this paper, the advantages and applications of Multi-Level Inverters are mentioned and a detailed description of different multi-level inverter topologies is presented. Single Phase H-Bridge Inverter functioning is realized virtually using MATLAB SIMULINK. A detailed Multi-Level Inverter is presented from which we concluded that the harmonic content is greatly reduced in Multi-Level Inverter. The cascaded H-bridge has the lowest weight and cost between the multilevel inverters, but its power losses is more that all the other topologies. Proposed switching pattern is having reduced events of switching as compared to conventional switching pattern. Lesser is the switching lesser is the switching losses. It is also observed that the inclusion of parallel diodes do not increase conduction losses of inverter. With the adoption of this proposed scheme losses of the inverter is reduced by 10 W.

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