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Optimized Test compression bandwidth management for Ultra-large-Scale System-on-Chip Architectures performing Scan Test Bandwidth Management

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Abstract

This paper presents several techniques employed to resolve problems surfacing when applying scan bandwidth management to large industrial multicore system-on-chip (SoC) designs with embedded test data compression. These designs pose significant challenges to the channel management scheme, flow, and tools. This paper introduces several test logic architectures that facilitate preemptive test scheduling for SoC circuits with embedded deterministic test-based test data compression. The same solutions allow efficient handling of physical constraints in realistic applications. Finally, state-of-the-art SoC test scheduling algorithms are rearchitected accordingly by making provisions for: 1) setting up time-effective test configurations; 2) optimization mof SoC pin partitions; 3) allocation of core-level channels based on scan data volume; and 4) more flexible core-wise usage of automatic test equipment channel resources. A detailed case study is illustrated herein with a variety of experiments allowing one to learn how to tradeoff different architectures andtest-related factors.

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INTRODUCTION

Today's multicore chip architectures require no trivial test solutions imposed by the relentless miniaturization of semiconductor devices, which have become much faster and less power hungry than their predecessors. This trend has given rise to the growing popularity of system-on-chip (SoC) designs because of their ability to encapsulate many disparate types of complex IP cores running at different clock rates with different power requirements and multiple power-supply voltage levels. Many SoC-based test schemes proposed so far utilize dedicated instrumentation, including test access mechanisms (TAMs) and test wrappers. TAMs are typically used to transfer test data between the SoC pins and embedded cores, whereas test wrappers form the interface between the core and SoC environment. Solutions involving both TAMs and wrappers accomplish such tasks as optimizing test interface architecture or control logic while addressing routing and layout constraints or hierarchy of cores [2], [5], scheduling test procedures and minimizing power consumption Techniques proposed in [4],and attempt to minimize SoC test time. The integrated scheme of reduces the test time by optimizing dedicated TAMs and pin-count aware test scheduling. Packet-switched networks-on-chip can replace dedicated TAMs in testing of SoC by delivering test data through an on-chip communication infrastructure.

There are techniques addressing synergistically TAM and wrapper design as well as test data compression [3]. In fact, test compression is now becoming an integral part of SoC-based design-for-test (DFT) schemes. For example, the approach of encodes tests for each core separately through linear feedback shift register (LFSR) reseeding with time-multiplexed automatic test equipment (ATE) channels delivering data to successive cores. Similarly, a scheme of utilizes static reseeding to test SoCs, where all cores share a single LFSR. The XOR test logic performs compression in [6], which further guides a TAM design process. ATE channel bandwidth management for SoC designs can play a key role in increasing test data

compression with no visible impact on test application time. The approach presented in [13] encompasses: 1) a solver capable of using input and output channels dynamically; 2) test scheduling algorithms; and 3) TAM design schemes, all devised for the embedded deterministic test (EDT) environment.

It is assumed that all cores in the SoC are either heterogeneous modules, or wrapped testable units, and they come with their individual EDT-based compression logic, which is subsequently interfaced with ATE through an optimized number of channels. As a result, test scheduling and TAMs can assign a fraction of the ATE interface capacity to each core. It increases compression ratios and allows tradeoffs between the test application time, volume of test data, test pin count, and interface design complexity. The scheme of [13] is applicable to any SoC-based test data reduction scheme capable of working with a varying number of In and output channels. Implementing a hierarchical DFT methodology for designs with a large number of cores poses significant challenges. First of all, the number of chip-level pins is limited and does not suffice to drive all cores in parallel. Given the pin limitations, it is impossible to determine the optimal allocation of pins to cores for the best compression. Furthermore, since a particular core can be reused in multiple designs, an optimal number of channel pins for this core when embedded in one design may invalidate test reuse in other designs. Under such circumstances, the chip integrators collect data for all individual cores, examine the data along with all constraints for the design, and then manually determine test schedules. This may result in suboptimal test data volume and compromised test application time, especially because of some outlier blocks having large pattern counts (PCs). Bandwidth management mitigates the dependence of core channels on the number of available chip-level pins, allows automatic scheduling of tests by making it transparent to the users, and significantly improves test planning at the core level. It also arbitrates the sharing of the chip-level channel pins, thereby guaranteeing the best

data volume and test time reductions for the overall design. In this paper, we present a bandwidth management scheme for hierarchical designs that lets a designer tradeoff fixed and flexible channel allocations per core as well as physical constraints to minimize the routing overhead of the TAM-based networks.

Furthermore, several techniques to deliver the control data during test are examined altogether with a new scheduling algorithm that allows changing the In and output channel allocations when switching the channel configurations. The remainder of this paper is organized as follows. After recalling principles of the EDT-based bandwidth management in Section II, Section III describes cost-effective schemes used to deliver control data, and subsequently to setup SoC test configurations. introduces a conditional merging-based test scheduler. It paves the way for more advanced test time reduction techniques based on balanced I/O pins partitioning, priority-based routing, and selective adjusting of interface throughput. Partitioning of SoC designs and handling their pin layout constraints are among key factors details experimental results obtained for this design.

II. PRIOR WORK

The SoC test environment (Fig. 1) of this paper comprises two switching networks, as introduced in [13]. An external ATE In channel i (ICi) feeds an In-switching network that reroutes compressed test data to different cores (in the remaining parts of this paper a given core k is denoted as Ck) based on the control data produced by a test scheduler. Since the scan routing paths from the chip-level test pins to the core-level test pins are dynamically selected by patterns, this interconnection network is also referred to as a dynamic scan router (DSR). Identical modules may share the same test data in the broadcast mode. In addition to individual EDT decompressions, each core features X-masking logic protecting its response compactor against unknown states and connecting the core with an output-switching network. This network allows the compressed output streams from successive cores to reach an output channel i (OCi),

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and to be sent back to the ATE. In order to facilitate test pattern reuse, test wrappers isolate all cores so that they are independent of each other

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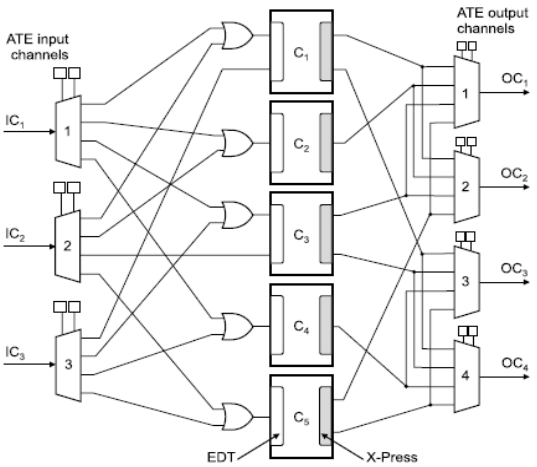

Fig. 1. SoC test environment with on-chip compression.

As shown in Fig. 1, the In DSR consists of demultiplexers whose number matches the number of ATE In channels. Given a group of test patterns, each demultiplexer connects the corresponding channel to one of several destination cores, as indicated by the content of address register. The number of ATE In channels cannot be smaller than the capacity of the largest single core in terms of its EDT In. Clearly, in the worst case, we can still test the largest cores, one at a time. Typically, low-order In of each core are used more frequently than others [13]. Hence, OR gates are deployed to assure that these In can receive data from more than a single ATE channel to increase flexibility of a test scheduler. Given the ATE In channels, the associated demultiplexers, and all cores with OR gates driving their EDT In, the actual connections between these terminals are arranged as follows. The EDT In (alternatively, OR gate In, if any) are connected with the demultiplexers in such a way that n EDT In of a given core are linked with n different ATE In channels, and each ATE channel serves approximately the same number of cores.

This method yields the actual size of the In demultiplexers and their control registers. Some final adjustments within a single module are also possible to simplify the resultant DSR layout and avoid costly and long connections. It is worth noting that a flexible use of ATE channels results in increased compression and elevated encoding efficiency. Moreover, testing many cores in parallel by dynamically allocating ATE channels to different cores in accordance with their needs may shorten test

application time. Finally, having individual de compressors running in appropriate time slots makes it easier to reduce the number of external channels compared with the total number of EDT In featured by all cores together. In preparation for the actual test session, the following steps are carried out.

1) For each core, automatic test pattern generation (ATPG)- produced test cubes are passed to a solver that merges and encodes them to arrive with final compressed test patterns; furthermore, the solver determines the minimal number of EDT In channels needed to compress a given test pattern.

2) For each test pattern at the core level, information regarding the minimal number of EDT In channels is paired with data concerning the required EDT output channels.

3) All test patterns are clustered to form groups (classes) of patterns having identical both In channels and observation points.

4) Upon completion of the above operations for each core, all classes are passed to a test scheduler; given architecture of both test access networks and various constraints (ATE channels, DSR architecture, power consumption, and others), it yields the final allocation of ATE In/output channels to selected cores when applying successive test patterns.

III. CONTROL DATA DELIVERY

The approach summarized in Section II does not make any specific provisions for the way control data is delivered to SoC test logic in order to setup test configurations. It appears, however, that the number of test configurations, and hence the amount of control data one needs to employ and transfer between the ATE and DSR address registers, may visibly impact test scheduling and the resultant test time. Consequently, we begin this paper by analyzing three alternative schemes that can be used to upload control bits and show how they determine the final SoC test logic architecture.

A. Using IJTAG

The IEEE 1687 is a proposed standard for accessing on-chip test and debug features

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via the IEEE 1149.1 test access port (TAP). The purpose of this internal Joint Test Action Group (IJTAG) standard is to automate the way one can manage on-chip instruments, and to describe a language for communicating with them via the IEEE 1149.1 test data registers (TDRs). If there is an IJTAG network available on the SoC, and the total number of test configurations is relatively small, one can use it to deliver the control data, as shown in Fig. 2. The SoC design of Fig. 2 has a single TAP and three different blocks: 1) two cores (C1 and C2) under test and 2) the DSR interfacing ATE with C1 and C2. TAP can be instructed to enable a test path via the IEEE 1687 segment insertion bits (SIBs). Every SIB is used to either enable or disable the inclusion of an instrument into the path from a test data In to a test data output. The TDR in C1 or C2 can be either bypassed or loaded with data putting both cores into specific test modes. The TDR in DSR receives the control data indicating which core and which of its test channels are connected to which ATE channels.

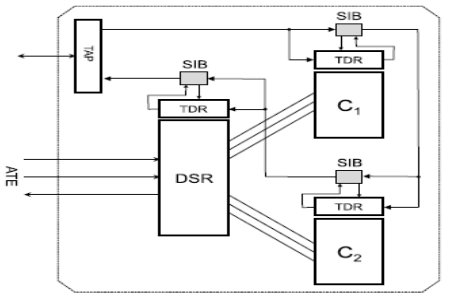

Fig. 2. Using IJTAG network to transfer control data.

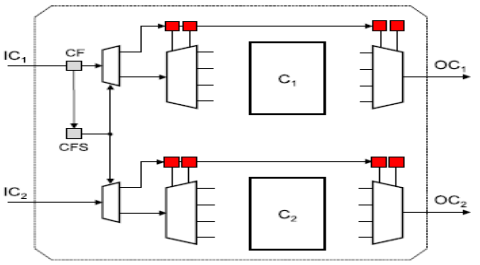

Fig. 3. Dedicated control chain-based architecture.

B. Dedicated Control Chain

The SoC design of Fig. 3 uses two dedicated control chains (shown as red squares) to deliver the control data. In principle, registers of both DSRs. Let the design have n In test pins and m output test pins at the chip-level. One can insert n control chains driven by n In test pins through n demultiplexers. The selector pin of each demultiplexers is controlled by a signal CFS. It is worth noting that if $n \geq m$, then n control chains suffice to supervise both In and output sides. If $n < m$, one chain can be used to control one In channel and multiple

output channels for the number of control bits per channel is typically much smaller than the pattern shift cycles. When CFS is set to 0, a test pattern is only used to deliver the control data for demultiplexers and multiplexers of the In and output DSR, respectively. This particular pattern does not have to be observed, and hence it only features an upload phase. Typically, however, the number of shift cycles for control patterns has to match the shift cycles of conventional tests as many ATEs may not distinguish between control patterns and regular test vectors. If CFS is equal to 1, patterns are applied as regular test vectors. The DSR, which has already been configured, connects then the respective ATE channels with the core test channels as indicated by the content of the address registers.

IV. TEST TIME REDUCTION

The tester bandwidth management in present large SoC designs and future kilo-core architectures with considerable diversity in the design styles and test needs of individual modules requires solutions beyond the capabilities of stateof- the-art DFT schemes. In particular, a test scheme will have to dynamically adapt to particulars of a given SoC architecture to assure an optimal utilization of its interface bandwidth.

In this section, we identify the key reasons for existing solutions' inability to further reduce tes application time and demonstrate how rearchitecting a test scheduler and DSR networks can mitigate it. Finally, we show how these methods reduce the test time in a global bandwidth management scheme.

A. Conditional Merging

The test-scheduling algorithm of Section II attempts (in a greedy fashion) to optimize the total test application time, whereas the number of test configurations remains virtually unlimited. Under certain circumstances, however, minimizing the number of test configurations may decrease the actual test time. Indeed, considering one would need to transfer control data necessary to reconfigure DSRs many times, reducing this activity may translate into some significant test time savings. The

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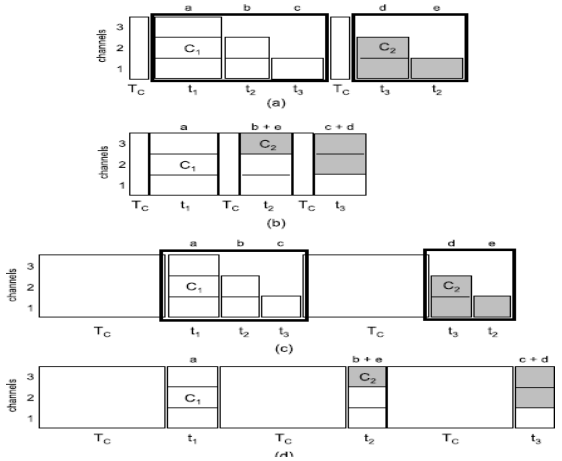
additional test-scheduling step taking care of this phenomenon will be further referred to as conditional merging, and it can be detailed as follows.



B. SoC In–Output Pin Partition

Optimizing SoC pin allocation based on scan data volume (SDV) at the In and output sides can further improve test scheduling. As typical SoC designs pack hundreds of cores—interfaced by strictly limited channel resources—into a space of a single chip, it is not unusual that the number of channels assigned to a single core as well as the ratio of EDT In to EDT outputs vary significantly. The same ratio also depends on a test pattern as the solver always selects the minimal number of In that suffice to encode a given vector while still observing all outputs. This disproportion is even more pronounced when several identical cores receive the same data in the broadcast mode, whereas their outputs must be observed independently to guarantee high quality of fault detection and diagnosis. Consider, for example, a circuit comprising eight identical cores with five In and outputs. Such a design would require supplying different subsets of five In channels while uninterruptedly monitoring all 40 outputs. The above observations clearly indicate that the DSRs should provide each core with channel resources adequate to its bandwidth requirements. Although the total number of ATE channels is typically fixed, most of SoC pins are bidirectional and can be configured either as In or outputs. One can exploit this flexibility; ultimately, it is the optimal proportion between improving bandwidth management.

SIMULATION RESULTS

The below figure shows the RTL Schematic

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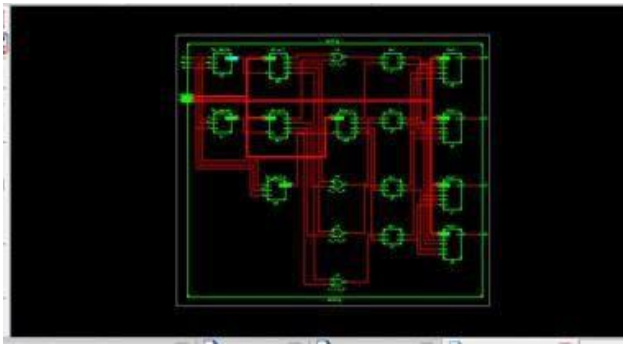

Fig. Simulation output waveform of the Soc testing

CONCLUSION

As Moore's law continues to provide smaller devices, designs with a range of core counts, capability per core, and energy per core make a dramatic impact on SoC design and test procedures. As shown in this paper, the I/O resources provided by a tester can be dynamically allocated to selected cores, whereas the total number of channels in use may remain unchanged. This paradigm clearly calls for efficient schemes minimizing the overall test application time, while taking into account physical constraints, in particular, SoC pin allocations. Assuming that all SoC cores are wrapped testable units, this paper studies several practical issues regarding SoC-based testing that deploys on-chip test data compression with the ability to dynamically use ATE channels. The proposed solutions include methods used to deliver control data and test scheduling algorithms minimizing the overall test application time. Experimental results obtained for a large industrial SoC design confirm feasibility of the proposed schemes and their ability to trade-off the number of test pins, design complexity of the TAM, and test application time.

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