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BIDIRECTIONAL INTELLIGENT SEMICONDUCTOR TRANSFORMER FOR POWER QUALITY ENHANCEMENT

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ABSTRACT: The transformers are the fundamental components of power distribution system. The conventional transformer does not guarantee the quality of power; it can only vary the magnitude of voltage. A Bidirectional Intelligent Semiconductor Transformer (BIST) is introduced where the power quality is of tremendous importance. The BIST is capable of bidirectional power flow, compensating voltage sags, swell & harmonics, offers input-output isolation, occupies less space and light in weight. The Space Vector Pulse Width Modulation (SVPWM) inverter is employed for suppressing the harmonics in the BIST. By using the SVPWM technique the dc bus utilization is also improved. As a result one can output the AC voltage of good power quality. The performance evaluation is done in terms of power quality by using MATLAB/SIMULINK environment.

Keywords: Bidirectional DC/AC Converter, Bidirectional Intelligent Semiconductor Transformer (BIST), High-Voltage AC/DC Rectifier, Hybrid-Switching

I. INTRODUCTION

The transformer is the one of the main component of electric power distribution systems. The configuration of the traditional transformer usually consists of iron core and it made up of aluminium / copper. The transformer oil serves as coolant and dielectric medium. But, in this type of construction significant weight, losses, environmental concerns regarding transformer oil and poor power quality are inherent. The new transformer is designed to overcome these problems. The transformer made of electronic devices that are coil free, self regulating and capable of correcting power quality problems can be developed. The complexity of electrical grid is increasing day by day due to enormous use of renewable energy sources. To cope up with this complexity, for reliable operation and better control, in such areas new topologies of grid components are investigated. One such topology is a bidirectional intelligent semiconductor transformer (BIST). So the traditional transformer cannot be employed in the areas where the power quality and light weight are of major concern such as smart grids and traction systems. Intelligent universal transformer proposed by the EPRI can address the drawback of traditional transformer. The design features include high frequency operation compact size and

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no mineral oil [1]. Various topologies of these intelligent universal transformers were investigated [2]. These offers the compensation to voltage sags and has the capability of addressing drawbacks of traditional transformers [1]-[9]. But some of them do not have bidirectional power flow capability. So, these topologies cannot be employed in micro grids and smart grids [1], [5]-[9]. The topology in [3] introduces a solid state transformer with a thee stage configuration [2] based on quad active bridge converter. But it has complexity in the control techniques. This topology introduces load isolation, distributed generation and storage. The charge dynamics in the high voltage semiconductors are investigated [4]. Most of the desired topologies are investigated in [5] which has the capability of replacing the conventional distribution transformer and operate at a high frequency. It has accounted for the benefits and the major problems associated with the solid state transformer [6]. The topologies [7]-[9] suffer from large switch counts and low efficiencies. The power factor cannot be controlled n the topologies [10],[11] through they offer the bidirectional power flow. The topology in [12] can address for power quality problems associated with the critical loads but it employs heavy and bulky line frequency transformers. The SST model in [13] has more number switches in each single phase module which results in increased losses and poor efficiency. The topologies introduced in [14]-[17] optimal three stage structure. It comprises of ac/dc converter, active bridge dc-dc converter and an inverter. These topologies have the capability of providing power factor correction and reactive power compensation. They suffer from heavy turn off losses in the dc/dc stage and complex control. The topology in [18]-[20] employ a LLC converter as a rectifier which offers at high frequency operation at high efficiency. But at the input stage efficiency of these topologies is low and have not concentrated on total harmonic distortion (THD). This paper proposes a bidirectional semiconductor transformer for power quality enhancement. It can be employed in the areas where the power quality is of major importance. It can cope up withhigh voltage at the input side as well as low voltage at the output side. It has a three part topology consisting of a high voltage, high frequency bidirectional ac/dc rectifier and bidirectional dc/dc converter and a space vector pulse width modulated dc/ac inverter.

II. HIGH FREQUENCY BIDIRECTIONAL AC/DC CONVERTER

The fig.1 shows the topology of the bidirectional high frequency ac/dc converter which is basically a LLC converter. This high frequency bidirectional ac/dc converter is configured with the help of three half bridge modules connected. These modules are connected in series at the input side to operate under higher voltages at the input side. This converter converts a single phase voltage of 1.06 KV into rectified voltage of into 190V. The IGBT switches are both connected in anti parallel manner at the input side, so as to cope with the low voltage at the output side, these half bridge modules are connected in shunt. It consists of high

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frequency transformers to provide high frequency resonance. They also offer better input to output isolation. To reduce the size of the system, switching loss the AC/DC converter is operated at a 50% duty ratio. The resonant stage is a basically a LLC converter.

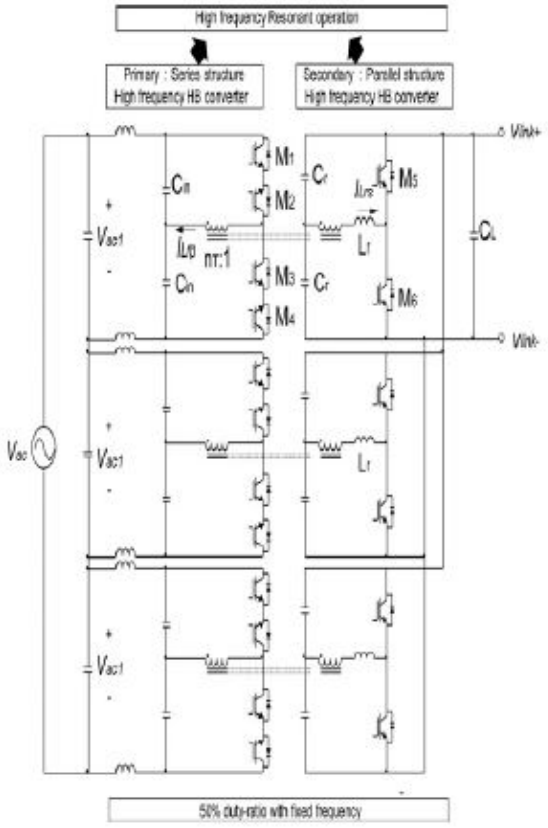

Fig.1. Bidirectional High Frequency AC/DC Converter.

The LLC resonant converter can operate over a wide range of input voltages at high power density and high power supply efficiencies. Further the zero voltage switching (ZVS) and zero current switching can be achieved through out its operating condition. The gain of each half bridge module is given by. The input given to the each half bridge module Vac1 = . The resonant frequency fr is equal to switching frequency fsr which is given by , with the resonant inductor Lr and two resonant capacitors Cr .

A. Operation of AC/DC Converter

Fig.

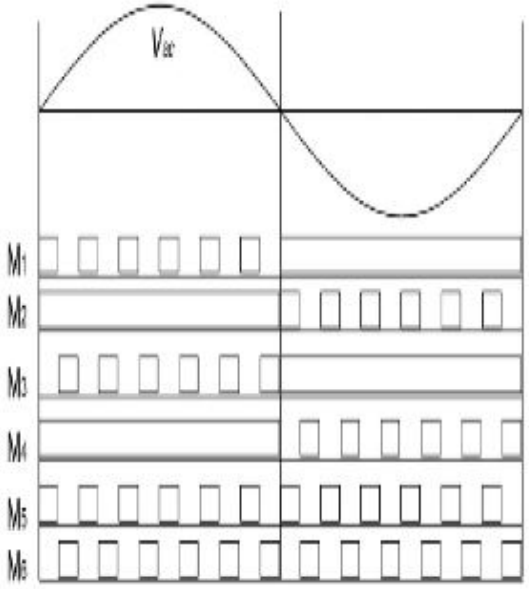

Fig.2. Driving signals of high-voltage resonant stage.

The AC/DC converter operates in four different modes. The modes are classified based on direction of power flow and polarity of input of input voltage. It is operated in resonant stage and the driving signals are shown in fig.2.

Mode 1: During mode 1 the polarity of input voltage is positive and the direction of power flow is forward. The switch M1 is turned on and is forward biased with the driving signal and the primary current flows through transistor in M1 and the diode in M2 is given a driving the M2T is reverse biased as the IGBTs are connected in anti parallel manner. The primary current flows

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through diode in M2 (M2D). Due to the transformer flux linkages the secondary current flows through diode in M5. In the next stage when M3 turn on, the primary current flows through the transistor in M3 (M3T) and the diode in M4 (M4D). Again due to flux linkages the current flows through the diode in M5 (M5D).

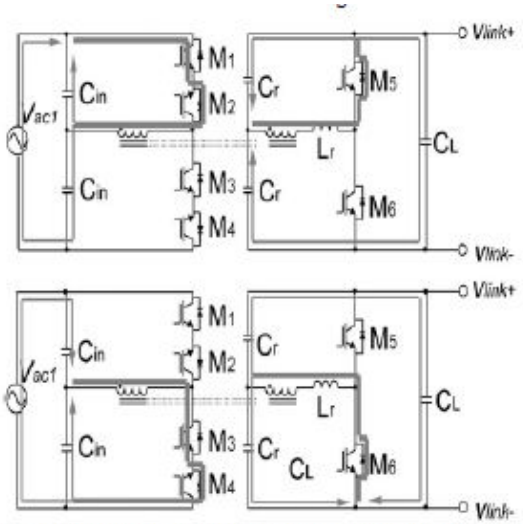

Fig. 2. (A) Mode 1: Figure showing the current path during forward power flow with positive input voltage.

Mode 2: During mode 2 the polarity of input voltage is negative and the direction of power flow is forward. In the mode 2 the primary current flows through the M2 transistor (M2T) and diode in switch M1 (M1D) and when the M2 is turn on. At this instant, the secondary current flows through the diode in M6 (M6D). When switch M4 is turned on, the primary current flows through transistor in M4 (M4T) and through the diode in M3 (M3D). At this instant the secondary flows through diode in M5 (M5D).

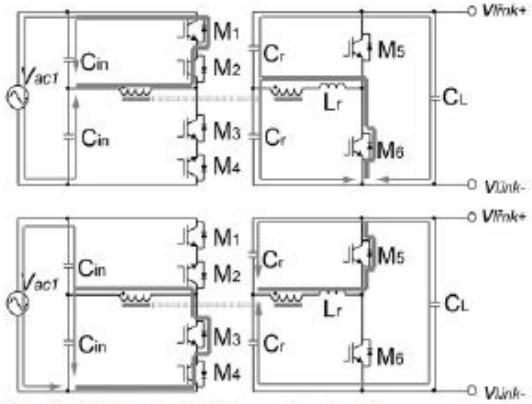

Fig. 2. (B) Mode 2: Figure showing the current path during forward power flow with negative input voltage

Mode 3: During mode 3 the polarity of input voltage is positive and the direction of power flow is reverse. In the mode 3 the secondary current flows through the M5 transistor (M5T) and primary current flows through diode in switch M1 (M1D) and transistor in M2 (M2T). In the next stage thesecondary current flows through transistor in M6 (M2T). The primary current flows through diode in M3 (M3D) and transistor in M4 (M4T).

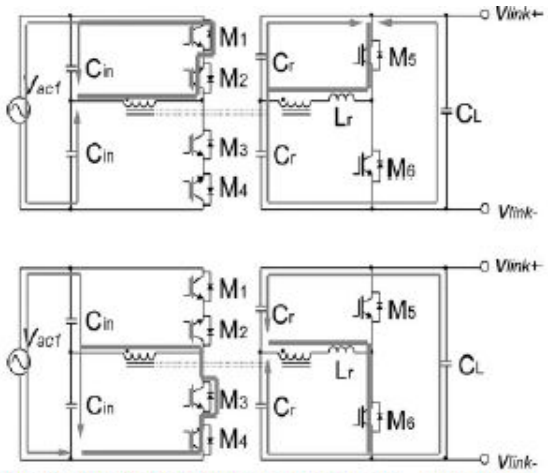

Fig. 2. (C) Mode 3: Figure showing the current path during reverse power flow with positive input voltage.

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Mode 4: During mode 4 operation the polarity of input voltage is negative and the direction of power flow is reversed. In the mode 4 the secondary current flows through the M6 transistor (M6T) and primary current flows through transistor in switch M1 (M1T) and diode in M2 (M2D). In the next stage the secondary current flows through transistor in M5 (M5T). The primary current flows through transistor in M3 (M3T) and in diode M4 (M4D).

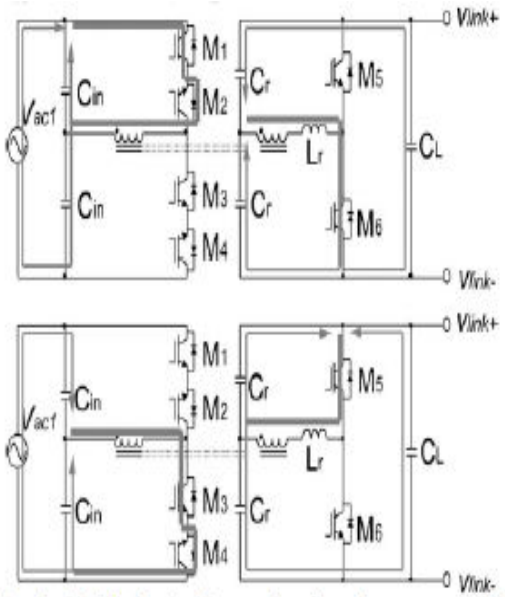

Fig. 2. (D) Mode 4: Figure showing the current path during reverse power flow with negative input voltage.

B. Zero voltage switching (ZVS) operation of BIST

It is assumed to have infinite magnetizing inductance Lm in the operational mode analysis of BIST, but practically it isnot possible. Hence the operational modes are to be analyzed more keenly. As all operational modes of BIST have similar operation, the ZVS operation is briefly explained for mode 1.

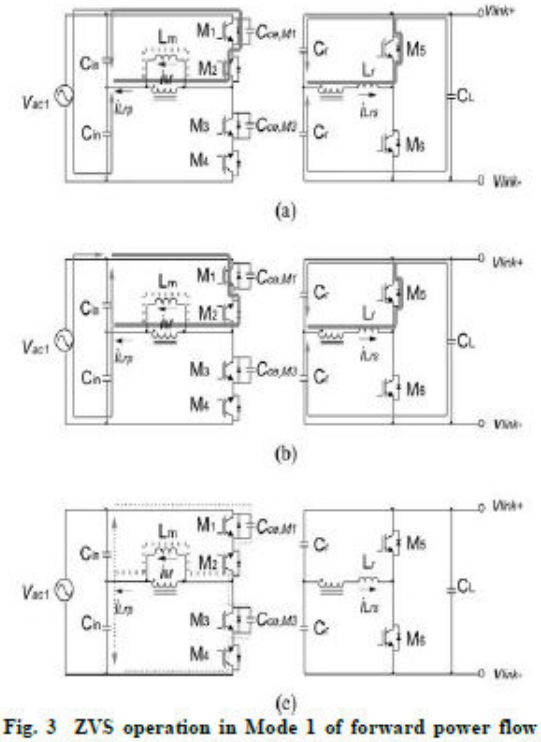

Fig. 3 ZVS operation in Mode 1 of forward power flow with positive input voltage. (a) Mode A. (b) Mode B. (c) Mode C.

Mode A: The function of the magnetizing current is to charge collector to emitter capacitance of and at the same time it discharges the collector to emitter capacitance of . During this process the collector to emitter voltage () of increases, while the collector to emitter voltage of () decreases. The mode A starts at the instant when exceeds the source voltage or crosses zero. Then starts to conduct the current. During mode A, the secondary resonant current is divided into half currents that flow through the two resonant capacitors as shown in Fig. 3(a). The primary resonant current is the sum of the magnetizing current and secondary resonant referred to the primary side (). Since is smaller than , the primary resonant current is negative so that it flows through M1D and M2T from the

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negative peak value of the magnetizing current. This mode continues until is equal to .

Mode B: After is greater than , flows through M1T and M2D. Since the resonant frequency is equal to the switching frequency , is nearly reduced to zero at the end of this mode. The mode B is shown in fig.3(b) .

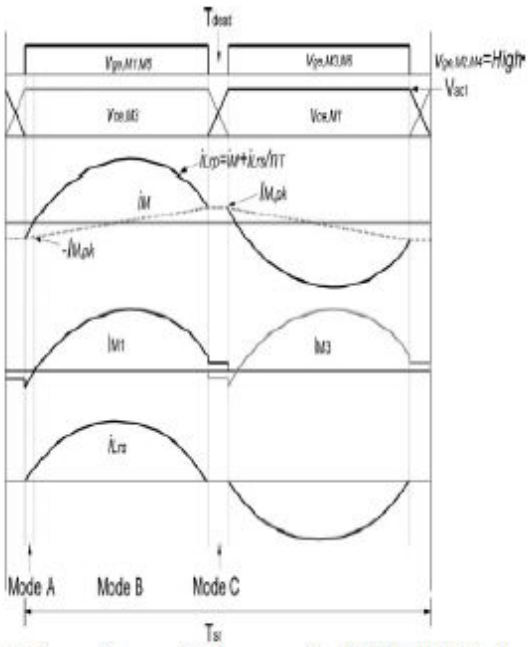

Fig.4.Zero voltage switching operation(ZVS) of Mode 1.

Mode C: The magnetizing current exists on the primary side when is turned off. It is assumed to be constant as mode C is a short dead-time period. As shown in Fig. 3(c), all switches of and are in turn-off state so that they can be modelled as their collector to emitter capacitances. The magnetizing current flows through two paths that is through Lm, , collector to emitter capacitance of , and through Lm, , , collector to emitter capacitance of . Therefore, the collector to emitter capacitance of is charged from zero to by the half of the magnetizing current and collector to emitter capacitance of is discharged from to zero by the half of the magnetizing current. It is made to complete the mode C operation before is turned on, to accomplish the ZVS of .The ZVS operation of is similar to that of as shown in Fig.4.

III. DC/DC CONVERTER

The low-voltage part consists of the dc/dc converter and the dc/ac inverter connected in cascade as shown in Fig. 5. The dc/dc converter changes the full-bridge rectified waveform of 190v peak to peak value into the constant dc voltage of 370 V.

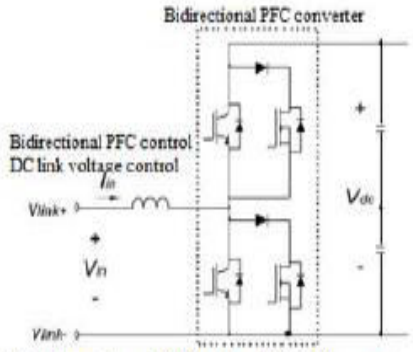

Fig. 5 Configuration of Bidirectional DC/AC converter.

The dc/dc converter and dc/ac inverter use a hybrid switch with IGBT and MOSFET connected in parallel. The dc/dc converter and dc/ac inverter are composed of two half-bridges connected in cascade. The dc/dc converter operates to control the power factor and the dc-link voltage, while the dc/ac As the inverter operates to control the output voltage. switching frequency in IGBT increases, the switching loss increases due to

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tail-current, which critically reduces the system efficiency as shown in Fig.6.

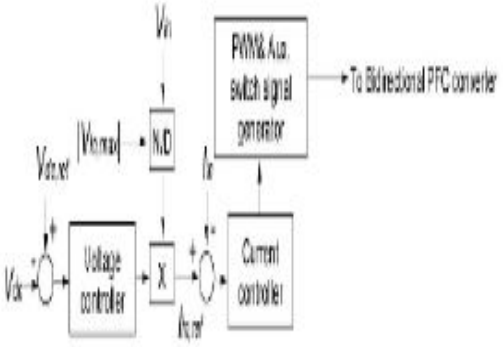

Fig.6. Control scheme for the bidirectional dc/dc converter.

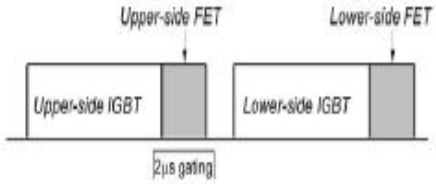

Fig.7. Gating method for hybrid switch.

To reduce the loss due to switching, the hybrid switch is implemented in the dc/dc converter. The MOSFET connected in parallel with the IGBT is the hybrid switch. The gating method for the hybrid switch is shown in Fig7. The MOSFET is switched on a few microseconds before the IGBT is switched OFF. The IGBT is turned OFF immediately after the MOSFET is turned ON. Now the MOSFET is turned OFF at the instant when the IGBT is must actually put OFF. This type of switching offers reduction of recovery loss due to tail-current. A diode is connected in series with MOSFET so that the destruction due to counter electromotive force can be protected.

IV. SPACE VECTOR PULSE WIDTH MODULATION INVERTER

The inverter employed here is a three phase voltage source inverter. The structure of a typical three-phase Voltage Source Inverter (VSI) is shown in Fig. 8. The major drawback of the PWM techniques is lower dc bus utilization. The space vector modulation technique improves dc bus utilization by 15.5%. This is one of the major advantages of this method. It has been shown to generate less harmonic distortion in the output voltages and currents of load and provides more efficient use of DC supply voltage, in comparison to direct sinusoidal modulation technique.Q1 through Q6 are the six power transistors and Va, Vb and Vc are the output voltages of the inverter. When an upper IGBT is switched on (i.e., when a or b or c is 1), the corresponding lower transistor is switched off (i.e., the corresponding a'or b' or c' is 0). The on and off states of the upper transistors, Q1, Q3 and Q5 are sufficient to evaluate the output voltage.

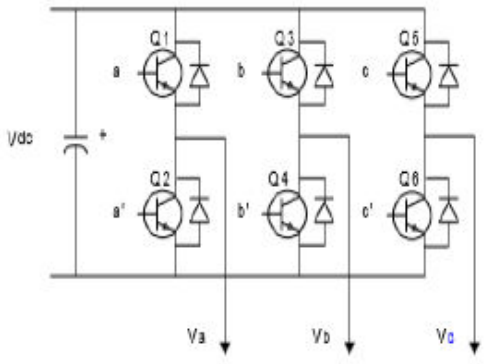

Fig. 8. Three phase voltage source inverter.

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The relationship between the switching variable vector [a, b, c]T and the line-to-line output voltage vector [VabVbcVca]T is given by (1).

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (1)$$

The relation between switching voltage vector and the phase (line-to-neutral) output voltage vector [VaVbVc]t is given by equation 2 below.

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{1}{3} V_{dc} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (2)$$

Vdc - DC supply voltage, or bus voltage.

Eight combinations are possible with on and off states of the upper three switches. The eight combinations and the derived output line-to-line and phase voltages in terms of DC supply voltage Vdc, according to equations (1) and (2), are shown in Table 1.

TABLE I: Device On/Off States and Corresponding Outputs of a Three-Phase VSI

A	B	C	V_a	V_b	V_c	V_{ab}	V_{bc}	V_{ca}
0	0	0	0	0	0	0	0	0
1	0	0	2/3	-1/3	-1/3	1	0	-1
1	1	0	1/3	1/3	-2/3	0	1	-1
0	1	0	-1/3	2/3	-1/3	-1	1	0
0	1	1	-2/3	1/3	1/3	-1	0	1
0	0	1	-1/3	-1/3	2/3	0	-1	1
1	0	1	1/3	-2/3	1/3	1	-1	0
1	1	1	0	0	0	0	0	0

Let us assume d and q are the fixed horizontal and vertical axes. The d-q transformation of the phase voltages corresponding to eight possible switching combinations is given by (3).

$$T_{abc-dq} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \quad (3)$$

The above transformation results in six non-zero vectors and two zero vectors as shown in Fig. 9. The nonzero vectors form the axes of a hexagon. The angle between any two adjacent non-zero vectors is 60 degrees. The zero vectors are at the origin and apply zero voltage to a three-phase load. The eight vectors are called the basic Space Vectors and are denoted here by V0, V60, V120, V180, V240, V300, and . This dq transformation can be applied to a desired three-phase voltage output to obtain a desired reference voltage vector in the d-q plane. To approximate the reference voltage instantaneously by any combination of the switching states corresponding to the space vectors is the main aim of SVPWM technique. One way to achieve this is to require, for any small period of time T, the average inverter output be the same as the average reference voltage as shown in (4). The T1 and in (4) are the respective durations for which switching states corresponding to and (or) are applied. and (or) are the basic space vectors that form the sector containing . Assuming that the change in reference voltage is small in the interval T, then equation (4) becomes (5), where. Therefore, it is critical that T be small with respect to the speed of change of . In practice the approximation is done for every PWM period, Tpwm. Therefore it is

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critical that the PWM period be small with respect to the speed of change of .

$$\int_{nT}^{(n+1)T} V_{out}(t) = \frac{1}{T}(T_1 V_x + T_2 V_{x\pm 60}) \quad (4)$$

$$V_{out}(nT) = \frac{1}{T}(T_1 V_x + T_2 V_{x\pm 60}) \quad (5)$$

Equation (5) means that for every PWM period, can be approximated by having the inverter in switching states and (or) for and duration of time respectively. Since the sum of and should be less than or equal to Tpwm, the inverter needs to be in state for the rest of the period. Therefore, equation (5) becomes (6), where.

$$T_{pwm} V_{out} = T_1 V_x + T_2 V_{x\pm 60} + T_0(O_{000} or O_{111}) \quad (6)$$

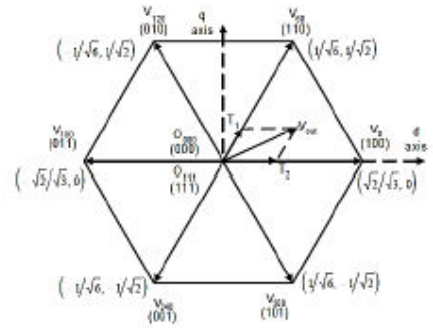

Fig.9. The Space Vectors Normalized w.r.t. V_{dc} and Switching States.

From equation (6), we get equation (7) for T1 and T2.

$$[T_1 T_2]^T = T_{pwm}[V_x V_{x\pm 60}]^{-1} V_{out} \quad (7)$$

where is the normalized decomposition matrix for the sector. Assuming the angle between and is , we can also obtain equation (8) in the following for and .

$$T_1 = \sqrt{2} T_{pwm} ||V_{out}|| \cos(\alpha + 30°)$$
$$T_2 = \sqrt{2} T_{pwm} ||V_{out}|| \sin(\alpha) \quad (8)$$

Depending on specific application, calculation of and can be done either with equation (7) or equation (8). Equation (7) is sector dependent. This approach is useful when is given in the form of vector [,]t. Equation (8) is independent of sector and is useful when is given in the form of magnitude and phase angle. can be the closest basic space vector on either side of . (or) is then the basic space vector on the opposite side. In either case, represents the component on , represents the component on the other basic space vector. The advantages of SVM are Utilization of D.C. link voltage is good and current ripple is low.

Optimize switching waveforms are flexible

V. TRANSFORMER DESIGN

To understand the BIST it is necessary to analyse and derive the expressions. During nth switching period, The input voltage,

$$V_{ac1}[n] = V_{ac1} \text{ Sin } \dot{\omega}_n T_{sr} \quad (9)$$

The link voltage,

$$V_{link}[n] = \frac{Vac1}{n_T} \text{ Sin } \dot{\omega}_n T_{sr} \quad (10)$$

$\dot{\omega}$ - angular frequency of V_{ac1}

T_{sr} – switching frequency of resonant converter

n_T- transformer turns ratio

The resonant waveform can be mathematically expressed as,

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$$i_{Lp}[n] = \sqrt{2} I_{Lp,rms}[n] \sin(2\pi f_{sr}(t-(n-1)T_{sr}) - \varphi[n] \quad (11)$$

$$i_{Ln}[n] = \frac{\pi V_{ac1,pk} \sin(\omega_n T_{gr})}{n_T R_B} \sin(2\pi f_{sr}(t-(n-1)T_{sr})) \quad (12)$$

where Rb is the effective resistor model of secondary stage

$$R_b = \frac{(V_{ac1,pk}/n_T)^2}{P_o} \quad (13)$$

P_0 - output power of each resonant converter.

The magnetizing inductance Lm for ZVS operation is given by

$$L_m = \frac{T_{dead}}{16 f_{sr} [Cce1 (Vac1) + Cce2 (n_T Vac1) n_T^2]} \quad (14)$$

Cce1, Cce2 – collector-emitter capacitances of primary and secondary switches respectively. From the above analysis, it can be concluded that the Vac1 and Lm chosen at minimum loss condition are the optimal design points for the LLC converter.

VI. COMPUTER SIMULATION

The computer simulation using MAT LAB/simulink software is performed to check the technical feasibility of the proposed BIST. The following fig.10 shows the simulation diagram of BIST. The fig. 11 show the operation of BIST during forward power flow and power flow reversal. The waveforms of input voltage, current, resonant current at a frequency of 50 KHz, rectified voltage, rectified current, dc link voltage output voltage and output current shown in fig.11 respectively. It can be observed that though the power flow is reversed at 0.1 ms the output voltage and output current waveforms are free from any kind of distortions. It can be observed that the dc link voltage is constant with negligible ripple and is maintained at 370V. It is concluded from the results that the proposed BIST operates properly according to the theoretical approach

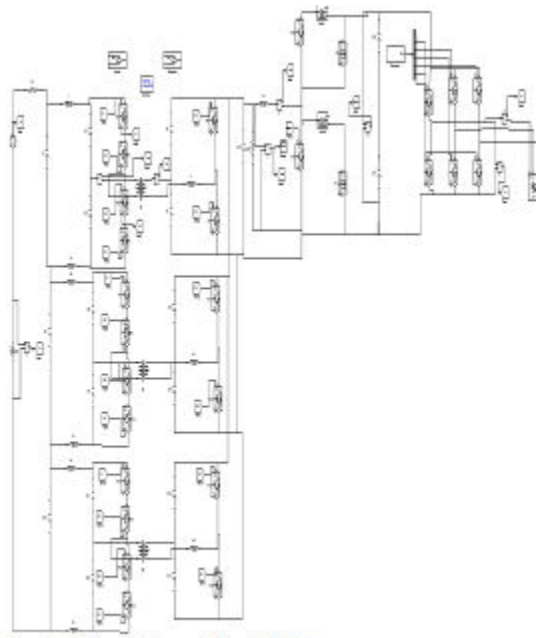

Fig. 10 Simulink model of BIST.

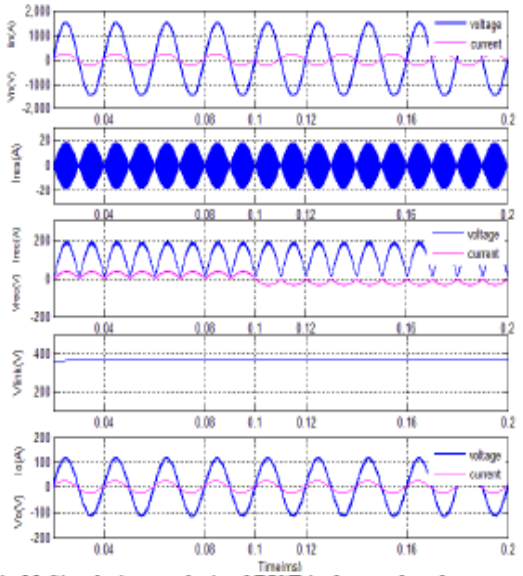

Fig.11.Simulation analysis of BIST in forward and reverse power flow.

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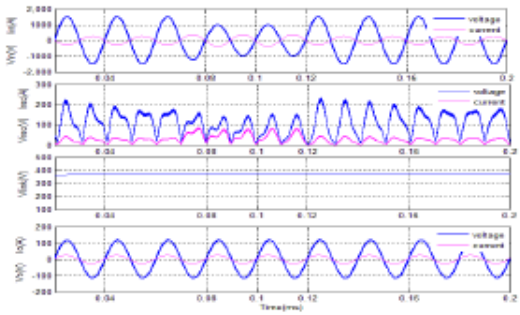
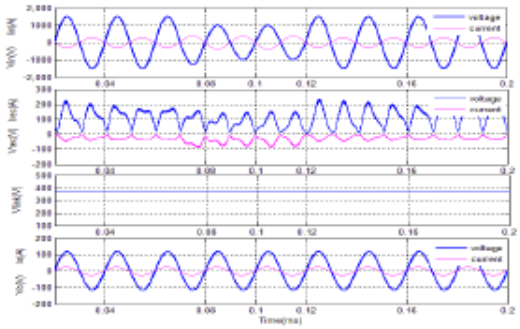
The waveform of input voltage, input current, rectified voltage, rectified current, dc link voltage output voltage and output current shown in fig.12(a) and fig. 12(b) during voltage sag condition under forward power flow and reverse power flow condition. The voltage sag is created from 0.07ms to 0.12ms and it can be observed that the dc link voltageslightly is maintained constantly at 370v by the voltage control of dc/dc converter. The output voltage and current are unaffected by the voltage sags



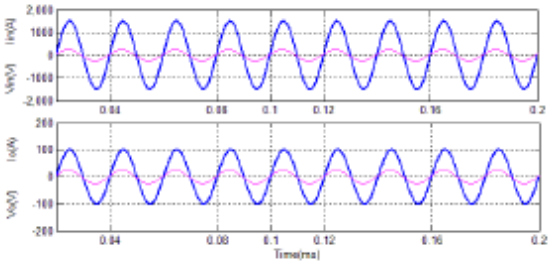
(a) Forward power



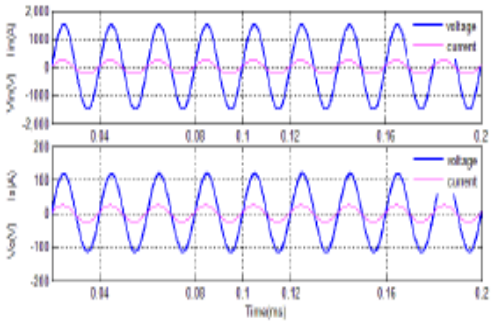
(b) Reverse power flow

Fig 12. Simulation analysis against input voltage sag.

can be observed that the output voltage and output current waves in both the cases (i.e. forward power flow and reverse power flow) are unaffected because the rectified current and input current slightly increases to maintain constant power output. From the figs. 13(a) and 13(b) the voltage output by the BIST with PWM inverter and SVPWM inverter can be compared for the same value of input voltage respectively. It can be observed that the voltage output by the BIST with SVPWM inverter is slightly greater than the voltage output by the BIST with PWM inverter for the same value of the given input in both the cases as SVPWM inverter has greater dc bus utilisation factor than PWM inverter



(a)



(b)

Fig. 13 Comparision of voltages output by PWM and SVPWM inverters.

A. FFT Analysis

The FFT analysis is done to study the harmonics of output voltage and current before and after using the SVPWM inverter. The THD of load voltage by using both PWM and SVPWM are tabulated. The harmonics are reduced in the load voltage by using a SVPWM inverter as shown in Fig.14.

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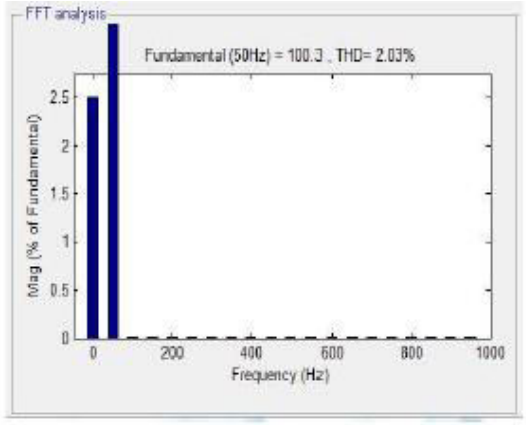

Fig. 14. FFT Analysis showing THD of load voltage using PWM & SVPWM inverters.

TABLE II: Comparison of THD with PWM and SVPWM Inverters

Inverter modulating technique	THD in Load Voltage (%)
PWM	2.03
SVPWM	0.88

VII. CONCLUSION

In this thesis the concept of a electronic transformer called BIST with new configuration is proposed. It has a rating of 1.5kV/120 V. The transformer consists of high voltage ac/dc rectifier, dc/dc converter and a SVPWM inverter. Its Operational feasibility is verified by MATLAB/Simulation. Though the PWM (Pulse Width Modulation) inverters have better control over output voltage magnitude and result in reduction in magnitude of harmonics, they account for lower magnitude of output voltage. The Space Vector Pulse Width Modulation (SVPWM) Technique can be employed for further reduction of harmonics and total harmonic distortion (THD). By using the SVPWM technique the THD of the output voltage is reduced to 0.88% from 2.03%.Thus the power quality is further improved. The output voltage is also increased from 100V to 120V. Hence the overall efficiency of the BIST is also improved.

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