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Volume 06, Issue 07, Pages: 390-400.
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AN EFFICIENT MULTIPLE-POLE MULTILEVEL DIODE CLAMPED CONVERTER WITH REDUCED COMPONENTS

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Abstract-Multilevel inverter technology has emerged recently as a very important alternative in the area of high power medium-voltage control and also for improving the total harmonic distortion by reducing the harmonics. Generally, the poor quality of voltage and current of a conventional inverter fed induction machine is obtained due to the presence of harmonics and hence there is a significant level of energy losses. The five level inverter and seven level inverter are used to reduce the harmonics. So, this paper presents the simulation of three phases five level and seven level inverter. In inverters by increasing the number of steps it generates the very high quality of the output voltage and current. This paper presents a five & seven levels multi-level inverter and these can follow a voltage reference with accuracy and with the advantage that the generated voltage can be modulated in amplitude instead of pulse-width modulation. To operate effectiveness of proposed topologies, a level-shifted pulse width modulation (LS-PWM) technique is presented and simulation results are verified for the operating stages of the proposed 5L &7L converter. And a novel multilevel ac/dc/ac converter with reduced number of semiconductor devices to achieve light weight, efficiency, and better input current quality. Comparative studies are conducted to analyze the performances of the two proposed front-end rectifiers and simulation results are presented by using Mat lab/Simulink environment.

Index Terms—Five-level (5L) multiple-pole converter, reduce number of semiconductor devices, transformer less drive.

I.INTRODUCTION

Majority of industrial drives use ac induction motor because these motors are rugged, reliable, and relatively inexpensive. Induction motors are mainly used for constant speed applications because of unavailability of the variable frequency supply voltage but many applications need variable speed operations. Historically, mechanical gear systems were used to obtain variable speed [1-2]. Recently, power electronics and control systems have matured to allow these components to be used for motor control in place of mechanical gears. Present day drive types are the Induction motor drives with voltage source inverters. Also the voltage waveforms of traditional two level inverter fed Induction motor shows that the voltage across the motor contains not only the required

"fundamental" sinusoidal components, but also pulses of voltage i.e. "ripple "voltage [3]. The recent advancement in power electronics has initiated to improve the level of inverter instead increasing the size of filter. The total harmonic distortion of the classical inverter is very high. The performance of the multilevel inverter is better than classical inverter. In other words the total harmonic distortion for multilevel inverter is low. The total harmonic distortion is analyzed between multilevel inverter and other classical inverter. A five level inverter consists of a series of H-bridge inverter units connected to three phase induction motor. The general function of this multilevel inverter [4-7].Power electronic devices contribute with an important part of harmonics, such as power rectifiers, thyristor converters and static var compensators. Even updated pulse-width modulation (PWM) techniques used to control modern static converters such as machine drives, power factor compensators, do not produce perfect waveforms, which strongly depend on the semiconductors switching frequency [8].

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency Pulse Width Modulation (PWM).Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced [9].Multilevel inverters have drawn tremendous interest in the power industry. They present a new set of feature that are well suited for use in reactive power compensation. Multilevel inverters will significantly reduce the magnitude of harmonics and increases the output voltage and power without the use of step-up transformer. A multilevel inverter consists of a series of H-bridge inverter units connected to three phase induction motor. The general function of this multilevel inverter is to synthesize a desired voltage from several DC sources. The AC terminal voltages of each bridge are connected in series [10]. Two combinations of 5L multiple-pole ac/dc/ac drives are the front-end bidirectional (5L-M2DCR, see Fig. 1) and unidirectional (5LM2SCR, see Fig. 3) rectifiers connected to the same rear-end (5L-M2DCI, see Fig. 1) inverter. To yield a fair analysis, the performances of both the front-end rectifiers with the 5L-M2DCI are evaluated with the power factor correction technique. The experimental results obtained along with the verified theoretical analysis have proven the feasibility of the topologies for any ac/dc/ac drive applications.

II. OPERATING PRINCIPLES OF 5L AC/DC/AC TOPOLOGIES

This section presents the operating principles of three different 5L ac/dc/ac PWM converters based on the classical MDCC and the existing M2DCC approaches. The derivation of the existing M2DCR and M2SCR topologies are explained here,

A. Classical Bidirectional Front-End 5L-MDCR With Rear-End 5L-MDCI Topologies

The classical 5L-MDCC ac/dc/ac is a back-to-back (BTB) configuration based on a frontend bidirectional rectifier (see Fig. 2) and a rear-end 5L diode clamped inverter. A total of 16 insulated-gate bipolar transistors (IGBTs) and 12 diodes in each phase leg is required in this topology to synthesize the 5L input and output voltage waveforms (see Fig. 3 for the front-end 5L unidirectional rectifier). The 5L voltage stepped waveform is obtained with the switching positions based on a single-pole circuit configuration, as shown in Fig. 4. It can be observed directly that the phase voltage

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levels are achieved across the point Va to the neutral point m.

B. Proposed Bidirectional Front-End 5L-M 2DCR With Rear-End 5L-M 2DCI Topologies.

The 5L-M2DCC ac/dc/ac drive presented in Fig. 1 consists of a front-end bidirectional 5L-M2DCR and a rear-end 5L-M2DCI. This BTB topology requires only eight power diodes in each phase leg to achieve the same input and output quality as the classical 5L-MDCC. However, when the number of cells in this topology increases, a total number of 6(n_3) diode components are reduced. The 5L voltage stepped waveform of the M2DCC topologies achieved with the switching positions based on the multiplepole hierarchy, as shown in Fig. 5. The 5L-M2DCC topology is configured with two classical 3L-MDCC cells (Outer cell—Cell 2 and Inner cell—Cell 1) in each phase leg, which is constructed based on the multiple-pole concepts. Hence

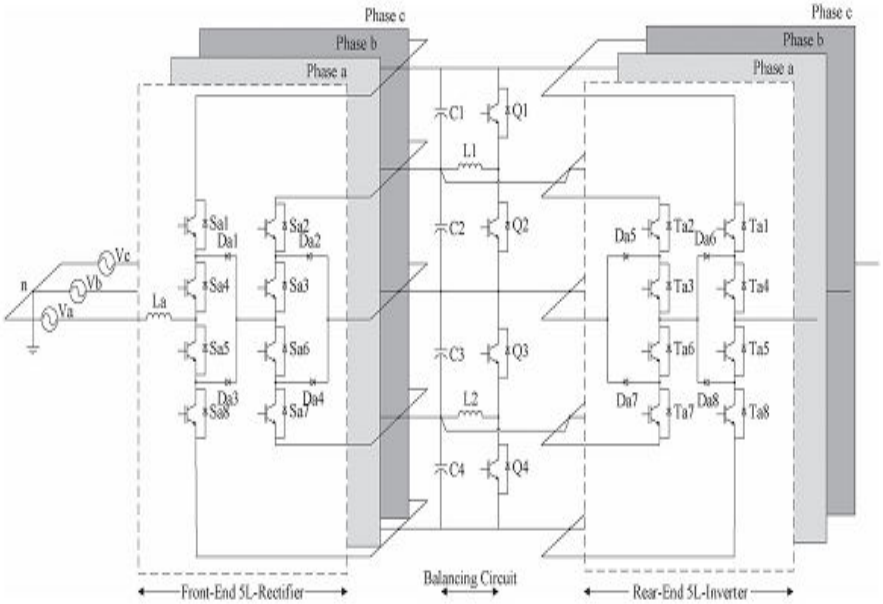

Fig. 1. Proposed 5L bidirectional ac/dc/ac drive based on multiple-pole multilevel diode-clamped converter (5L-M 2DCC) approach.

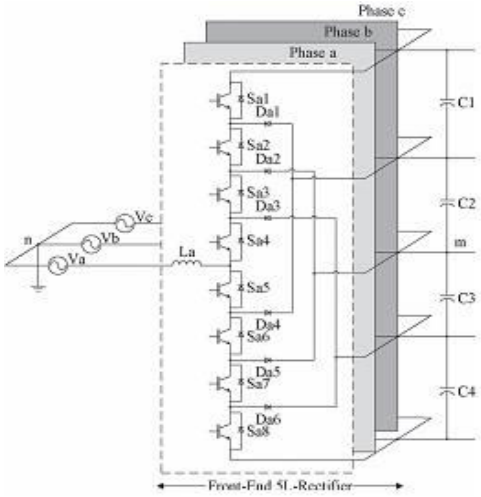

Fig. 2. Classical front-end 5L bidirectional rectifier (5L-MDCR).

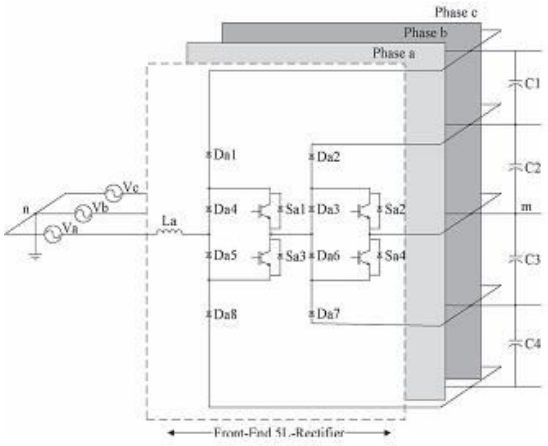

Fig.3. Proposed front-end 5L unidirectional rectifier (5L-M 2SCR).

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The 5L input and output voltage stepped waveforms are achieved with the multiplepole configuration according to the corresponding switching state listed in Table I.

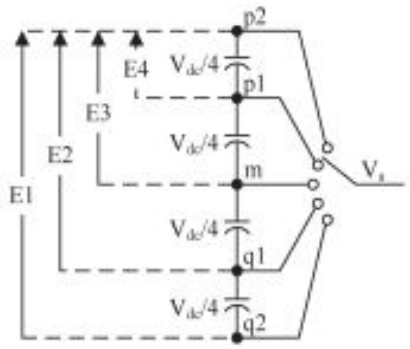

Fig. 4. Circuit diagram of per phase leg single-pole classical 5L-MDCCtopology with switching position.

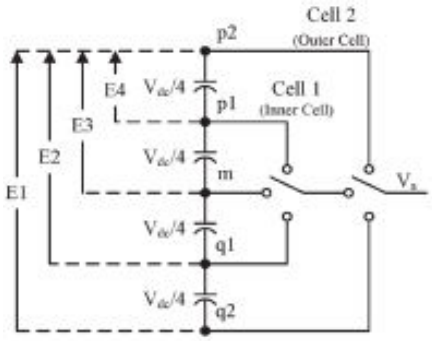

Fig.5. Circuit diagram of per phase leg multiple-pole 5L-M 2DCC topology with switching position.

TABLE I
Switching Logic for Respective IGBT in 5l-M2dcc Topology

Vom / Switch	Vdc/2 (Sector II)	Vdc/4 (Sector I & III)	0 (Sector I, III, IV & VI)	-Vdc/4 (Sector IV & VI)	-Vdc/2 (Sector V)
Sa1, Ta1	1	0	0	0	0
Sa2, Ta2	1	1	0	0	0
Sa3, Ta3	1	1	1	0	0
Sa4, Ta4	1	1	1	1	0
Sa5, Ta5	0	1	1	1	1
Sa6, Ta6	0	0	1	1	1
Sa7, Ta7	0	0	0	1	1
Sa8, Ta8	0	0	0	0	1

1: on and 0: off

C. Proposed Unidirectional Front-End 5L-M 2SCR With Rear-End 5L-M 2DCI Topology.

A bidirectional power flow in the front-end rectifier is not required for certain ac/dc/ac drive applications such as propulsion, compressor, or any non-Regenerative braking system. Thus, a transformerless front-end unidirectional rectifier is reconstructed in Fig. 3 with the arrangement of the semiconductor devices in the bidirectional M2DCR configuration (see Fig. 1). Hence, the unidirectional 5L rectifier in Fig. 3 is named as multiple-pole multilevel switch-clamped rectifier (M2SCR) instead. Each phase leg of the unidirectional 5L-M2SCR also requires two cells, as shown in Fig. 5, to achieve 5L input voltage stepped waveform. The states selection of the top and bottom diodes of a M2SCR is dependent on 1-Sa1 and 1-Sa2 for the outer cell and similarly for the inner cell. Hence, only two switching devices are required in each cell, with four series diodes connected to the terminals of the capacitors in the dc link. In Fig. 3, the two switching devices (Sa3 and Sa4) of the inner cell are connected directly to the neutral-point clamped of the four dc-link capacitors, whereas the other two switching devices (Sa1 and Sa2) of the outer cell are clamped to the output terminals of the inner cell. Due to lesser number of switches needed, higher power efficiency is achieved with lesser switching and conduction losses.

D. General Characteristic of the Classical and Proposed5L AC/DC/AC Converters

The front-end rectifier and the rear-end inverter of 5L ac/dc/ ac drives are operated independently with same level-shifted PWM (LS-PWM). The LS-PWM requires a reference signal and a set of four 1-kHz triangular carriers to achieve the desired switching signals for the respective

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semiconductor switches. The switching function of the LS-PWM technique for the 5Lrectifiers and inverters is expressed as

$$\begin{cases} S_{a1}(t) = T_{a1}(t) = 2m_a \sin \omega t - 1 \\ S_{a2}(t) = T_{a2}(t) = 2m_a \sin \omega t \\ S_{a3}(t) = T_{a3}(t) = 2m_a \sin \omega t + 1 \\ S_{a4}(t) = T_{a4}(t) = 2m_a \sin \omega t + 2 \end{cases} \quad (1)$$

Where m_a is the ratio of two times the fundamental component of pole voltage to the dc-link voltage.
Under the condition of steady state and balanced dc-link voltage, the general incremental output pole voltage equation is expressed as

$$V_{xm}(t) = \frac{V_{dc}(t)}{n-1}\left(\sum_{i=1}^{n-1} T_{xi} - \frac{n-1}{2}\right) \quad (2)$$

Where x represents phase "a," "b," and "c;" and n is the number of voltage level. T_{xi} is the switching states of each switching device depicted in the inverter side. The voltage transfer ratios of the converters system between the dc bus voltage to the input and output voltage are defined as

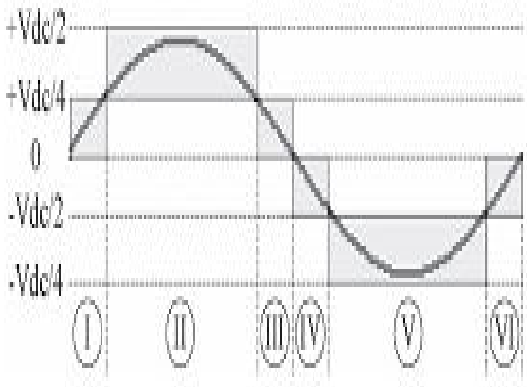

Fig 6. Incremental input and output voltage stepped waveform of a BTB ac/dc/ac drive.

$$\begin{cases} M_{x,\text{rectifier}}(t) = \dfrac{V_{dc}(t)}{V_{L-L}(t)}, & M_{x,\text{rectifier}}(t) > 1 \\ M_{x,\text{inverter}}(t) = \dfrac{2V_{xm}(t)}{V_{dc}(t)}, & M_{x,\text{inverter}}(t) \le 1 \end{cases} \quad (3)$$

Where $V_{x,L-L}(t)$ is the line-to-line grid voltage, and $V_{xm}(t)$ is the output pole voltage referred to the inverter side. In general, high modulation index (Mx, rectifier (t) >1) of the front-end rectifier is required to mitigate the input current distortion and achieve good voltage tracking due to its boosting effect in nature. Meanwhile, the rear-end inverter must be operated at the linear region (Mx, inverter (t) <1) to prevent any high-order harmonic components incurred in the load. Thus, low switching frequency can be used for a 5L rectifier to achieve better power conversion efficiency. The ripple current is expressed in the following equation based on the previous ones, namely, (2) and (3):

$$\Delta I_{Lx}(t) \approx \frac{k}{L_x f_s}\left\{\frac{3V_{x,L-L}(t) - 3\sqrt{3}V_{mn}(t)}{3\sqrt{3}} - \frac{M_{x,\text{rectifier}}(t)V_{x,L-L}(t)}{(n-1)}\left(\sum_{i=1}^{n-1} S_{xi,d} - \frac{n-1}{2}\right)\right\} \quad (4)$$

Where fs is the switching frequency of the rectifier circuit, and $V_{mn}(t)$ is the virtual ground voltage referred from node m to node n in Fig. 1. $S_{xi,d}$ is the switching transition with respect to the respective sector in Fig. 6. k is the duty ratio of switching transition (see Fig. 6), and this is expressed as

$$\begin{cases} 0 \le [k = 2\sin \omega t] \le 1, & 0 \le \omega t \le \frac{\pi}{6} \\ 0 \le [k = 2(\sin \omega t - 1/2)] \le 1, & \frac{\pi}{6} \le \omega t \le \frac{\pi}{2}. \end{cases} \quad (5)$$

The critical input inductance value for front-end 5L-M2DCR can be estimated with the duty cycle and the switching states with respect to the sectors shown in Fig. 6. According to (4), the maximum peak value of the input ripple current is determined at ωt =

30◦, Thus, the critical inductance value is estimated as follows:

$$L_{x,\max} \approx \frac{4(0.5V_{xn} - V_{mn}) - V_{dc}}{4\Delta I_{Lx} f_s} \quad (6)$$

Where V_{xn} is the peak value of the grid phase voltage.

The minimum capacitance value in the dc link can be estimated in (7) with the change of ampere-second (ΔAcap sec) and the switching state Ta1 of the rear-end side. The expression

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of ΔAcap sec is obtained by subtracting the peak value of the grid phase current with the average input current of the converter. Assume that all the dc-link capacitors are equal toC. Then

$$C \approx \frac{4\Delta A_{\cap}\sec}{\Delta V_{\text{cap}}} = \frac{4T_{a1}\left(I_a - I_{\text{inv(avg)}}\right)}{\varepsilon V_{\text{dc}} F_s} \tag{7}$$

Where ε is the percentage value of the permissible ripple voltage content, and Iin V(avg) is the average input current value of the rear-end 5L inverter. By expanding the expression of (7), the final capacitance value is expressed as (8), shown at the bottom of the page, where $I_{rms}$is the root-mean-square (RMS) value of the grid current, and θ is the power factor angle between the grid phase voltage and current

III. HIGH-POWER-FACTOR OPERATION OF THREE-PHASE 5L M2DCR AND M2SCR RECTIFIERS

A. SEMICONDUCTORS VOLTAGE AND CURRENT STRESSES

Voltage and current stresses are the dominant factors considered in the converter design, so that the converter can achieve optimum performance with higher reliability. Proper selection of device rating for the proposed front-end rectifiers is determined based on the global stress analysis. The voltage and current stress expressions for the respective front-end rectifiers are derived with the switching function in (1) and based on the following factors: 1) high-power-factor operation; 2) current and voltage ripple free; 3) constant switching frequency; 4) balanced dc-link capacitors voltage; and 5) zero voltage dropped across boost inductors (Lx).The maximum voltages across the power devices of unidirectional 5L-M2SCR and bidirectional 5L-M2DCR are respectively expressed in the following:

$$\begin{cases} V_{Da1} = \frac{3V_{\text{dc}}}{4} \\ V_{Da4} = V_{Sa1} = \frac{3V_{\text{dc}}}{8} \\ V_{Da2} = V_{Da3} = V_{Sa2} = \frac{V_{\text{dc}}}{4} \end{cases} \tag{8}$$

$$\begin{cases} V_{Sa1} = \frac{3V_{\text{dc}}}{4} \\ V_{Sa4} = \frac{V_{\text{dc}}}{2} \\ V_{Sa2} = V_{Sa3} = V_{Da1} = V_{Da2} = \frac{V_{\text{dc}}}{4} \end{cases} \tag{9}$$

Since the maximum voltage stress expressions (8) and (9) are for the power devices in the upper phase leg, the respective complimentary power devices in the lower phase leg are also determined using the same expressions. The average current stress is analyzed over one period of the fundamental frequency based on the assumed five factors (1)–(5). For simplification, the average current stress is approximated as follows based on respective switching functions in (1):

$$\begin{aligned} I_{Sa\{\text{Outer Cell}\}}(t) &= I_{\text{Da }\{\text{Outer Cell}\}}(t) \\ &= \frac{1}{2\pi}\int_0^{2\pi} I_a \sin(\omega t) S_{a\ \{\text{Outer Cell}\}}\, d\omega t \\ I_{Sa\ \{\text{Inner Cell}\}}(t) &= I_{\text{Da }\{\text{Inner Cell}\}}(t) \\ &= \frac{1}{2\pi}\int_0^{2\pi} I_a \sin(\omega t) \\ &\quad \times \left[2 - \frac{4V_{\text{am(1)}}}{V_{\text{dc}}}\sin\omega t\right] S_{a\ \{\text{InnerCell}\}}\, d\omega t. \end{aligned} \tag{11}$$

TABLE II
Number of Components Used In the Front-End Rectifier Topologies

Devices	Topologies				
	Unidirectional Rectifier			Bidirectional Rectifier	
	Classical 5L-MDCR (ref. to Fig. 6 of [1])	Classical 5L-MDCR (ref. to Fig. 7 of [1])	Proposed 5L-M^{2}SCR	Classical 5L-MDCR	Proposed 5L-M^{2}DCR
Diode	24	24	24	18	12
IGBT/MOSFET	18	18	12	24	24
Capacitors	4	4	4	4	4
Complementary Switch	0	9	0	12	12
Isolated Gate Driver	18	18	12	24	24
Cost (USD)	$7472.72	$8943.56	$5698.07	$6616.08	$7410.76
Efficiency (%)	77.37	80.44	85.42	80.99	82.30
Weight (kg)	8.01	9.63	6.17	7.14	7.91

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TABLE III
Maximum Voltage Stress Level for Respective Power Devices under Unbalanced Dc-Link Capacitor Voltages Condition

Topologies	Semiconductor	IGBTs				Diodes			
		Sa1	Sa2	Sa3	Sa4	Da1	Da2	Da3	Da4
Unidirectional Rectifier	5L-MDCR (ref. to Fig. 6 of [1])	0	$V_{dc}/2$	V_{dc}	V_{dc}	0	$V_{dc}/2$	$V_{dc}/2$	$V_{Da4}< V_{dc}/4$
	5L-MDCR (ref. to Fig. 7 of [1])	$V_{dc}/2$	$V_{dc}/2$	$2V_{dc}$	$2V_{dc}$	0	0	$V_{Da3}< V_{dc}$	$2V_{dc}$
	5L-M^{2}SCR	$V_{Sa1}< V_{dc}/2$	$V_{dc}/2$	$V_{Sa3}< V_{dc}/2$	$V_{dc}/2$	V_{dc}	$V_{dc}/2$	$V_{dc}/2$	$V_{Da4}< V_{dc}/2$
Bidirectional Rectifier	5L-MDCR	$V_{dc}/4$	$V_{dc}/2$	$V_{dc}/2$	$V_{Sa4}< 2V_{dc}$	$V_{dc}/4$	V_{dc}	$2V_{dc}$	$V_{Da4}< 2V_{dc}$
	5L-M^{2}DCR	V_{dc}	$V_{dc}/2$	$V_{dc}/2$	$V_{Sa4}< V_{dc}/2$	$V_{Da1}< V_{dc}/2$	$V_{Da2}< V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$

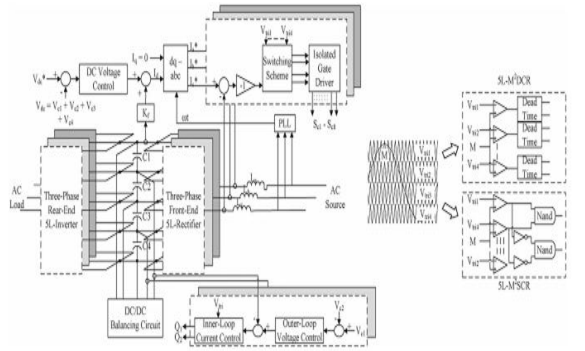

Fig. 7. Front-end rectifier controller for the 5L ac/dc/ac converter.

B SRF CURRENT CONTROL SCHEME

The control algorithm with power factor correction technique is shown in Fig.7. Two control loops, i.e., synchronous-reference-frame (SRF) current control and constant switching frequency modulation, are implemented to regulate the dc-link voltage and mitigate the current distortions. Due to the simplicity of the control strategy, low-cost integrated control circuit can be designed. The balancing control for the dc–dc balancing circuit is presented. The unity power factor controller for the front-end 5L rectifiers (M2DCR or M2SCR) designed in Fig.7.is based on the SRF current control with the LS-PWM technique. The detailed analyses of the outer-loop dc-link voltage control and the inner-loop current control are both presented. SRF controller provides a good dynamic response to achieve high quality input sinusoidal current with constant unity powerfactor performance. The open-loop transfer function of the dc-link voltage control under steady-state condition is written as follows to achieve a stable control system:

$$L(s) = \frac{K_p s + K_I}{s} \cdot \frac{L_x I_d}{C_{eq} V_{dc}} \cdot \frac{\left(\frac{\sqrt{3}V_p}{L_x I_d}\right) - s}{s + \left(\frac{I_{dc}}{C_{eq} V_{dc}}\right)} \quad (11)$$

Where $K_p$and $K_I$are the proportional and integral parameters of the dc voltage control loop selected at 0.4 and 15, respectively. $C_{eq}$and $L_x$are the equivalent capacitance of the dc bus and the input (phases a, b, and c) filter inductance with the values of 600 μF and 5 mH, respectively. $V_p$is the RMS value of the grid phasevoltage, and V_{dc} is the mean value of the dclink voltage. Id is the peak value of the reference current, which is obtained from the summation of I_{dc} (output of dc voltage control) and feed forward current (output of Kf). The feed forward current control loop under steady-state condition is derived based on the power balanced principle, which is expressed in the following:

$$K_f = \frac{V_{dc}}{\sqrt{3}V_p} \quad (12)$$

Where Vp is the RMS value of the grid phase voltage.

V.MATLAB/SIMULATION RESULTS

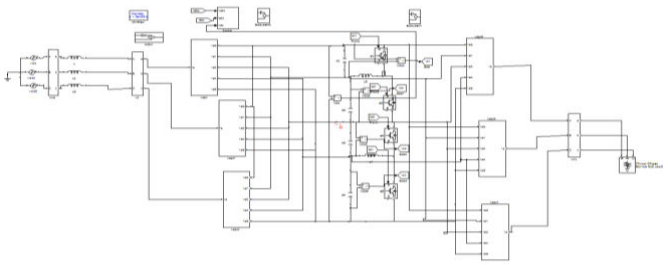

Fig.8.Matlab/Simulation model of 5L bidirectional ac/dc/ac drive based on multiple-pole multilevel diode-clamped converter (5L-M 2DCC) approach.

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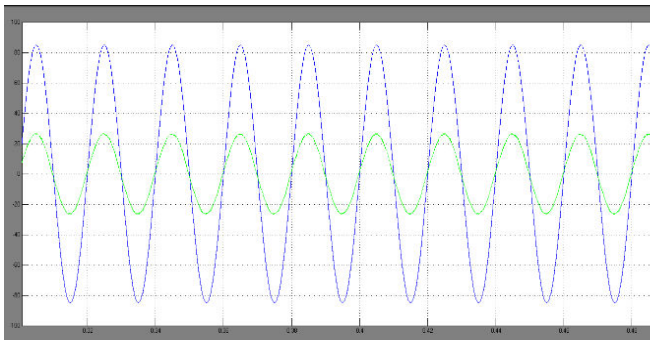
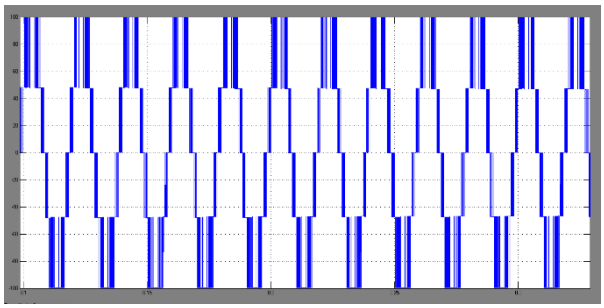
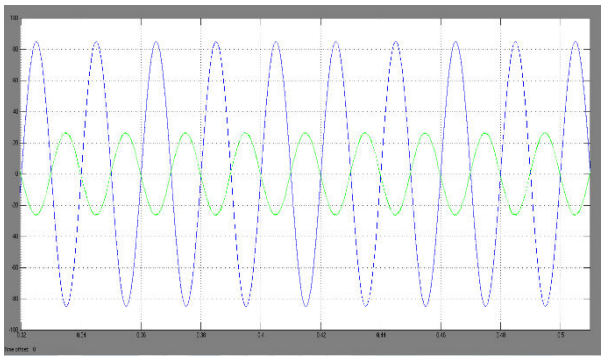


(a)

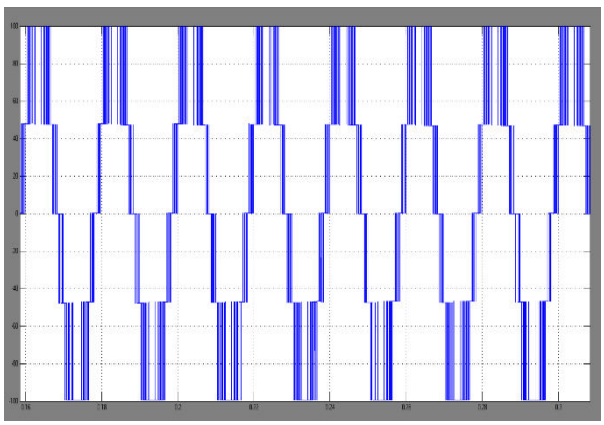


(b)

Fig. 9. Unity power factor operation with rectifying mode. (a) Voltage and current at the grid side. (b) Pole voltage at the rectifier side.

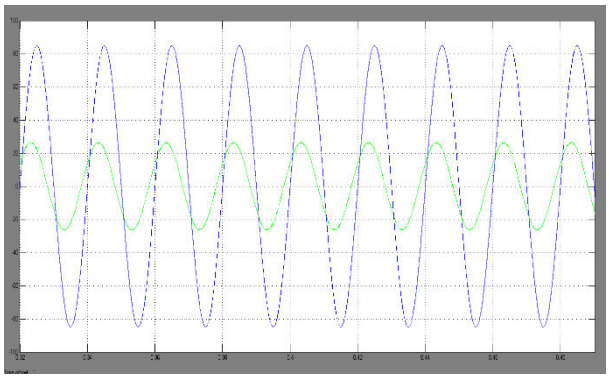


(a)

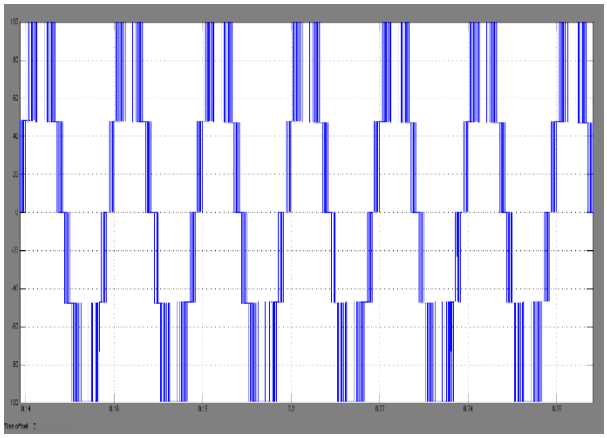


(b)

Fig. 10. Unity power factor operation with inverting mode. (a) Voltage and current at the grid side. (b) Pole voltage at the rectifier side.

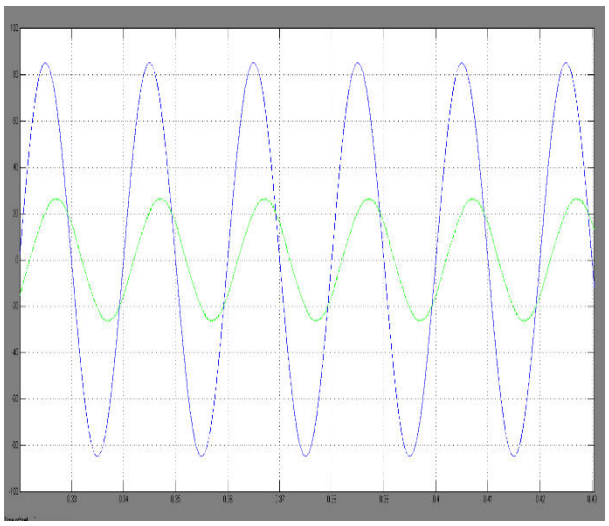


(a)



(b)

Fig. 11. Leading power factor, PF = 0.43. (a) Voltage and current at the grid side. (b) Pole voltage at the rectifier side.



(a)

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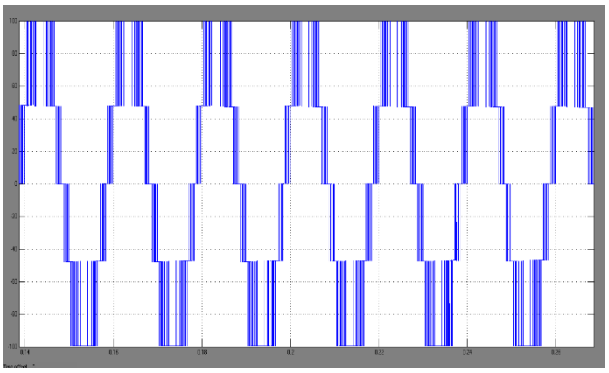

(b)

Fig. 12. Lagging power factor, PF = 0.43. (a) Voltage and current at the grid side. (b) Pole voltage at the rectifier side.

MATLAB/SIMULATION RESULTS OF 7L AC-AC Converter

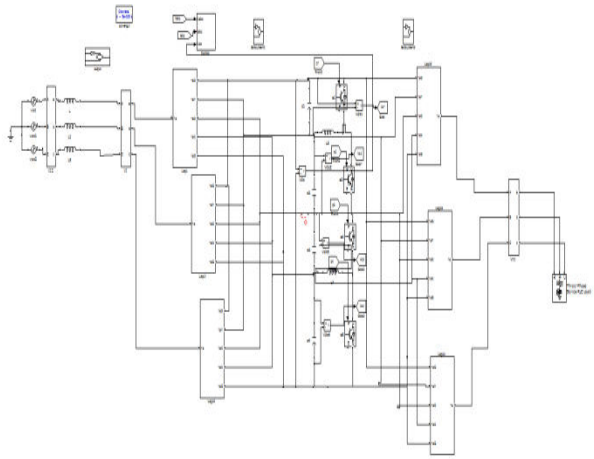

Fig.13.Matlab/Simulation model of Proposed 7L bidirectional ac/dc/ac drive based on multiple-pole multilevel diode-clamped converter (5L-M 2DCC) approach.

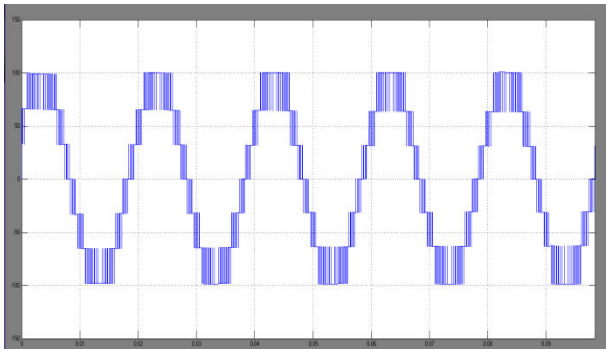

Fig.14.shows the output voltage of the proposed seven level inverter.

Parameter setting for AC-AC Converter

Parameter	Value of 5L Converter	Value of proposed 7L Converter
Input Grid Voltage	60Vrms (50Hz)	60Vrms (50Hz)
DC-Link Voltage	200V DC	200V DC
Input Inductors(Lx)	5mH	5mH
Switching Frequency	1kHz	1kHz
THD(Voltage)	29.46	18.26
THD(Current)	3.27	2.21

Comparison of 5L and 7L AC-AC Converter with classical Diode clamped converter

DEVICES	Classical 5L-MDCR	5L-MMDCR	Classical 7L-MDCR	Proposed 7L-MMDCR
Diode	18	12	30	12
IGBT	24	24	36	36
Capacitors	4	4	6	4
Isolated gate driver	24	24	36	36

Comparison of Components for classical 7L AC-AC Converter with proposed 7L AC-AC Converter

DEVICES	Proposed 7L-MMDCR	Existing 7L-MDCR
Diode	12	30
IGBT/MOSFET	36	36
Capacitors	4	6
THD(Voltage)	18.26	24.23
THD(Current)	2.21	<5%

VI. CONCLUSION

A new generation of front-end unidirectional 5L-M^{2}SCR, 7L- M^{2}SCR and bidirectional 5L-M^{2}DCR topologies has been introduced in this paper to reduce the number of semiconductor devices compared with the conventional converters. The agreement between the theoretical analysis is validated and has proven the feasibility of the two proposed ac/dc/ac topologies. Excellent performance and low input current distortion with high power factor is achieved with low operational switching frequency of 1 kHz without the aid of any bulky *LC* passive filter. In addition to that, the reduction of component counts allows the proposed converters to achieve low voltage/current stress and low switching losses. The total harmonic distortion is very low compared to that of classical inverter and five level inverter. Also seven level inverter is having less THD than five level inverter. The simulation result shows that the harmonics have been reduced considerably. The five level and seven level inverter has been successfully simulated and the results of voltage waveforms, current waveforms. The inverter system can be used for industries where the adjustable speed drives are required.

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