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A Three-Phase Dual-Buck Inverter with Unified PWM Applied to Induction Motor

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Abstract:- This paper presents a three phase voltage source dual buck inverter using unified PWM technique. This technique enhances the system reliability. It is a hard switching voltage source inverter. This dissertation proposes a new type of cascade inverters based on dual-buck topology and phase-shift control scheme. Compared to traditional cascade inverters, they have enhanced system reliability thanks to no shoot-through problems and lower switching loss with the help of using power MOSFETs. With phase-shift control, The AC induction motor is a rotating electric machine designed to operate from a 3-phase source of alternating voltage. The unified PWM technique reduces the computational burden in real time implementations by making use of a digital signal processor. Different PWM methods like Sinusoidal PWM, Space Vector PWM and Discontinuous Space Vector PWM (DSVPWM) can be applied to a three phase dual buck inverter. It does not need dead time and has no shoot through concerns. A three level cascaded dual buck inverter is also controlled using unified PWM technique. An induction motor (IM) is a type of asynchronous AC motor where power is supplied to the rotating device by means of electromagnetic induction. The Induction motor is a three phase AC motor and is the most widely used machine.

Index Terms— Space Vector PWM, three phase AC motor, Dual-buck inverter, three-phase inverter, PWM, voltage source inverter.

I. INTRODUCTION

Among various multilevel voltage-source inverters, the most commonly used and commercially available ones are the flying capacitor inverter and cascade H-bridge inverter. Cascade inverters are with separate dc sources, and each dc source is associated with a single-phase inverter while the ac terminals of each inverter are connected in series.The cascade types of inverters are capable of reaching higher output voltage level by using commercially standard lower voltage devices and components, and it features the modular design concept which makes the maintenance less burdensome. The standard half-bridge or full-bridge inverter is a typical voltage source inverter (VSI) with two active switches in one phase leg. It needs dead time to prevent shoot-through problems between the switches in one leg. Because of dead time effect, the output waveforms can be distorted and the equivalent transferred energy of pulse-width modulation (PWM) is reduced. At some fault conditions, even with added dead time, shoot-through is still the reason for dominant failure of the circuit. In addition, with higher dc bus voltage operation, this standard inverter cannot simply employ power MOSFETs as the active switches due to the reverse recovery problem of the body diode of MOSFETs. To utilize the benefits of power MOSFETs, such as lower switching loss, resistive conduction voltage drop, and fast switching speed which reduces the current ripple and the size of passive components, the dual buck inverter had been proposed. The dual-buck inverter typically consists of two buck inverters with one operating at the positive half-cycle while the other one working at the negative half-cycle. The dual-buck type inverters do not need dead time, and they totally eliminate the shoot-through concerns, thus leading to greatly enhanced system reliability. It can be hard switched because the body diode of MOSFET never conducts, and the external diodes can be independently selected to minimize switching losses. A Three level cascaded dual buck inverter in which two three-phase dual-buck inverter shown in Fig. 1 are connected in series.. It is hard-switching-based, but it can incorporate power MOSFETs as the active switches. The number of switches is the same as that of the standard three-phase voltage source inverter using insulated-gate-bipolar-junction-transistors (IGBTs). It does not need dead time since there is only one active switch per leg. It can be modulated with unified pulse width modulation to further reduce the switching losses and make use of the dc bus voltage completely.

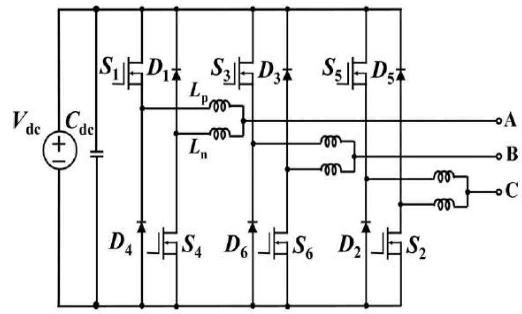

Fig.1. Three-phase dual buck VSI with MOSFET

This paper proposes a three-phase dual-buck inverter, shown in Fig. 1. It is hard-switching-based, but it can incorporate power MOSFETs as the active switches. The device count is the same as that of the standard three-phase VSI using insulated-gate-bipolar-junction-transistors (IGBTs). The idea of a three-phase dual-buck inverter originated from single-phase half-bridge and full-bridge dual-buck inverters [10]–[12]. It does not need dead time and has no shoot-through concerns. Because the body diode of the MOSFET never conducts, it can be hard-switched. The free-wheeling diodes can be chosen independently with fast reverse recovery features to minimize switching loss. Compared to single-phase dual-buck inverter, the three-phase counterpart does not have double fundamental frequency ripple on the dc bus, and can be modulated with discontinuous space vector PWM (DSVPWM) to further reduce the switching losses and fully utilize the dc bus voltage.

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II. DUAL BUCK INVERTER

This is a new type of three phase voltage source inverter (VSI), called three phase dual-buck inverter. The proposed inverter does not need dead time, and thus avoids the shoot through problems of traditional VSIs, and leads to greatly enhanced system reliability. Though it is still a hard-switching inverter, the topology allows the use of power MOSFETs as the active devices instead of IGBTs typically employed by traditional hard switching VSIs. As a result, the inverter has the benefit of lower switching loss, and it can be designed at higher switching frequency to reduce current ripple and the size of passive components. Pulse width modulation (PWM) is introduced to reduce computational burden in real-time implementation. PWM methods were applied to a three-phase dual-buck inverter ,the output of the three phase dual buck converter is fed to induction motor and its performance are analyzed in PWM modulation techniques The widely used standard three-phase voltage source inverter (VSI) has two active switches in one phase leg that present some common problems. First, dead time is needed between the two active switches of the same phase leg, which reduces the equivalent pulse width-modulated voltage, and leads to output waveform distortions and less energy transfer. Second, even with dead time, shoot-through is still the major killer of VSIs, especially at some fault conditions. Third, people cannot simply employ power MOSFETs because of the reverse recovery problems of the body diode. In order to obtain the benefits of using MOSFETs, such as low switching loss, resistive conduction voltage drop, and fast switching speed that allows reduction of current ripple and the size of passive components, conventional approaches adopt soft switching techniques, the basic operation principle of the proposed inverter. Second, it analyzes the specific unified PWM technique applied to the three-phase dual-buck inverter. Finally, it shows a 2.5-kW hardware prototype and the test results under different dc bus voltage and duty cycle conditions to pwm. Efficiency of different cases was measured and compared.

III. UNIFIED PWM ANALYSIS

Even though MOSFETs are used for the three phase dual buck inverter to cut down switching losses, it is still a hard switching VSI. Therefore, it is better to further reduce the switching loss by incorporating DSVPWM. At the same time, the dc bus voltage can be fully utilized by adopting SVPWM or DSVPWM rather than SPWM. Traditionally, the SVPWM methods need to do trigonometric calculation and perform recombination of actual gating times, which is Unfavorable for real-time implementation by a digital signal processor. SVPWM and DSVPWM can be equivalently generated using triangle carrier comparison like SPWM, which greatly reduces computational burden and is very easy to implement by DSP. The unified PWM generation block diagram. The switch to which PWM is applied is selected based on the current reference polarity. The phase duty cycles da, db and dc are provided by a closed-loop controller. The injected zero

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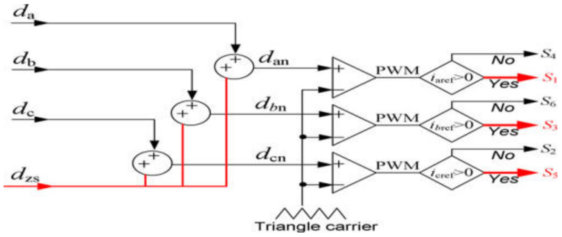
sequence duty cycle dzs is generated by the following equation. Renewable energy and distributed generation are getting more and more popular, including photovoltaic modules (PV), wind turbines, and fuel cells. The renewable energy sources need the power electronics interface to the utility grid because of different characteristics between the sources and the grid. No matter what renewable energy source is utilized, inverters are essential in the microgrid system. Thanks to flexible modular design, transformerless connection, extended voltage and power output, less maintenance and higher fault tolerance, the cascade inverters are good candidates for utility interface of various renewable energy sources. This dissertation proposes a new type of cascade inverters based on dual-buck topology and phase-shift control scheme. Compared to traditional cascade inverters, they have enhanced system reliability thanks to no shoot-through problems and lowers witching loss with the help of using power MOSFETs. With phase-shift control, it theoretically eliminates the inherent current zero-crossing distortion of the single-unit dual-buck type inverter. In addition, phase-shift control can greatly reduce the ripple current or cut down the size of passive components by increasing the equivalent switching frequency.



Uniform Pulse Width Modulation

The harmonic content can be reduced by using several pulses in each half cycle of output voltage. The generation of gating signals for turning ON and OFF transistors by comparing a reference signal with a triangular carrier wave. The frequency Fc, determines the number of pulses per half cycle. The modulation index controls the output voltage. This type of modulation is also known as uniform pulse width modulation (UPWM)

Sinusoidal Pulse Width Modulation

Instead of, maintaining the width of all pulses of same as in case of multiple pulse width Modulation, the width of each pulse is varied in proportion to the amplitude of a sine wave Evaluated at the centre of the same pulse. The distortion factor and lower order harmonics are reduced significantly. The gating signals are generated by comparing a sinusoidal reference Signal with a triangular carrier wave of frequency Fc. The frequency of reference signal Fr, determines the inverter output frequency and its peak amplitude Ar, controls the modulation Index M and rms output voltage Vo. The number of pulses per half cycle depends on carrier Frequency

A. Single pulse width modulation

In this control, there's only one pulse per half cycle and the width of the pulse is varied to control the inverter output. The gating signals are generated by comparing a rectangular reference signal of the amplitude Ar with triangular carrier wave of amplitude Ac, the frequency of the carrier wave determines the fundamental frequency of output voltage. By varying Ar from 0 to Ac, the pulse width can be varied from 0 to 100 percent. The ratio of Ar to Ac is the control variable and defined as the modulation index

B. Multiple pulse width modulation

The harmonic content can be reduced by using several pulses in each half cycle of output voltage. The generation of gating signals for turning ON and OFF transistors by comparing a reference signal with a triangular carrier wave. The frequency Fc, determines the number of pulses per half cycle. The modulation index controls the output voltage. This type of modulation is also known as uniform pulse width modulation (UPWM).

C. Sinusoidal pulse width modulation (SPWM)

Instead of, maintaining the width of all pulses of same as in case of multiple pulse width modulation, the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the centre of the same pulse. The distortion factor and lower order harmonics are reduced significantly. The gating signals are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency Fc.The frequency of reference signal Fr ,determines the inverter output frequency and its peak amplitude Ar,controls the modulation index M,andVrms output voltage VO.The number of pulses per half cycle depends on carrier frequency .Inverters that use PWM switching techniques have a DC input voltage that is usually constant in magnitude. The inverters job is to take this input voltage and output ac where the magnitude and frequency can be controlled. There are many different ways that pulse-width modulation can be implemented to shape the output to be AC power. A common technique called sinusoidalPWM will be explained. In order to output a sinusoidal waveform at a specific frequency a sinusoidal control signal at the specific frequency is compared with a triangular waveform.The inverter then uses the frequency of the triangle wave as the switching frequency. This is usually kept constant The triangle waveform, vtri, is at switching frequency fs; this frequency controls the speed at which the inverter switches are turned off and on. The control signal, vcontrol, is used to modulate the switch duty ratio and has a frequency f1. This is the fundamental frequency of the inverter voltage output. Since the output of the inverter is affected by the switching frequency it will contain harmonics at the switching frequency. The duty cycle of the one of the inverter switches is called the amplitude modulation ratio, m_a

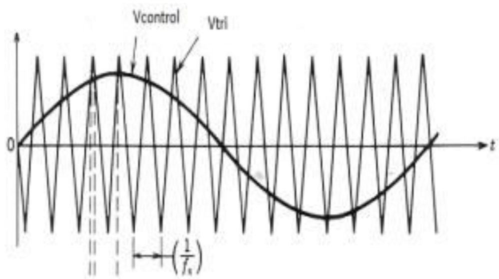


Fig.3 Desired frequency is compared with a triangular waveform

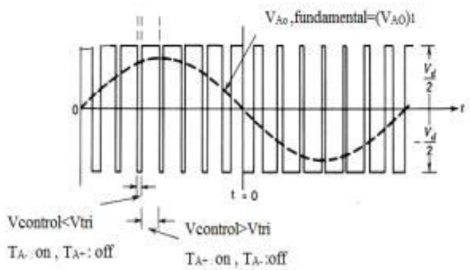


Fig.4 Pulse-width Modulation (PWM)

Three Phase Voltage Source Inverters

The standard three-phase VSI topology is shown in Fig. 2.24 and the eight valid switch states are given in Table 2.3. As in single-phase VSIs, the switches of any leg of the inverter (S1 and S4, S3 and S6, or S5 and S2) cannot be switched on simultaneously because this would result in a short circuit across the dc link voltage supply. Similarly, in order to avoid undefined states in the VSI, and thus undefined ac output line voltages, the switches of any leg of the inverter cannot be switched off simultaneously as this will result in voltages that will depend upon the respective line current polarity. Of the eight valid states, two of them produce zero ac line voltages. In this case, the ac line currents freewheel through either the upper or lower components. The remaining states produce non-zero ac output voltages. In order to generate a given voltage waveform, the inverter moves from one state to another. Thus the resulting ac output line voltages consist of discrete values of voltages that are Vi , 0, and -Vi for the topology shown in Fig. 2.25. The selection of the states in order to generate the given waveform is done by the modulating technique that should ensure the use of only the valid states.

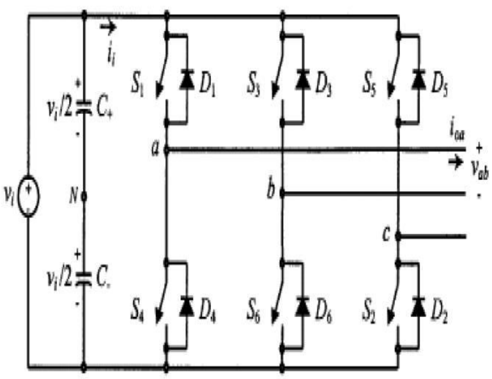


Fig. 5 Three-phase VSI topology

IV. MATLAB/SIMULINK RESULTS:

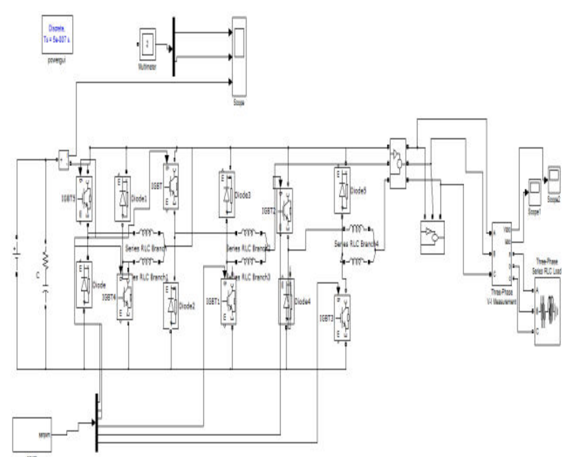


Fig 6 Matlab/simuink model of Proposed three-phase dual buck VSI with MOSFET'S

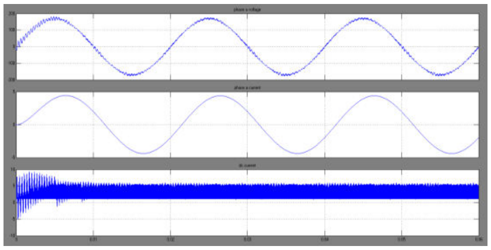


Fig 7 Simulated output wave forms of Phase voltage, Phase current and Dc currents

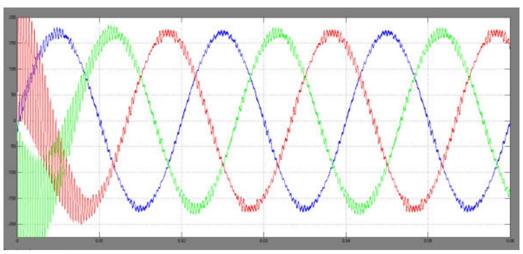


Fig 8 Simulated output voltage wave form of three phase dual buck VSI

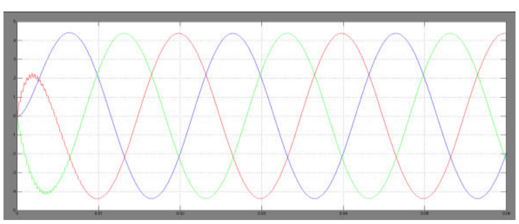


Fig 9 Simulated output Current wave form of three phase dual buck VSI

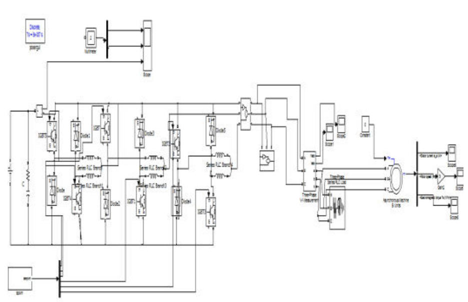


Fig 10 Matlab/simulink model of proposed three phase dual buck VSI connected to the Induction motor.

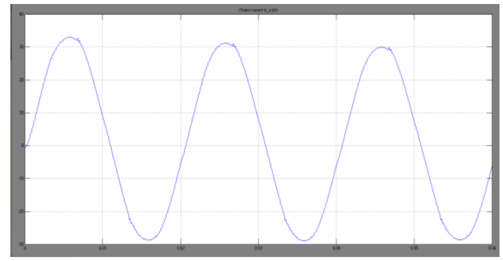


Fig 11 Simulated output wave form of the Stator currents of the Induction motor

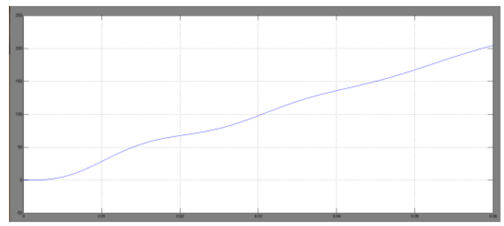


Fig 12 Simulated output wave form of the Rotor speed of the Induction motor

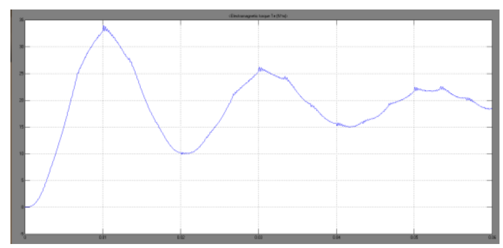


Fig 13 Simulated output wave form of the Electromagnetic torque of the Induction motor

V. CONCLUSION

The proposed concept can be implemented in real time; the inverter output voltage can be given to grid with lowering the harmonic content from the inverter output voltage, the three-phase dual-buck inverter, has been proposed. It has the advantage of utilizing power MOSFETs as active switches, and improves inverter reliability by eliminating the possibility of shoot-through and the need for dead-time. In order to reduce the computational load on the digital signal processor, unified PWM was analyzed and applied, To prove the effectiveness of the proposed topology and control scheme, a three-phase dual-buck inverter system operating at standalone mode with 2.5 kW, 208VAC output capability has been designed and tested. Different PWM methods were tested under different dc bus voltage and duty cycle conditions. The efficiency of different cases was reported, and the peak efficiency was 98.8%.The proposed concept is connected to Induction motor and performance characteristics has been shown and studied.

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