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Paper Authors

DR PAGIDIMARRI KRISHNA, MRS D. LAXMI, MRS B. SUSHMA
Nalla Malla Reddy Engineering College,Hyderabad.

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A NEW GRID INTERFACING CONVERTER FOR GROUND LEAKAGE CURRENT REDUCTION IN SOLAR BASED SYSTEMS

[1]DR PAGIDIMARRI KRISHNA, [2]MRS D. LAXMI, [3]MRS B. SUSHMA
[1]Professor in EEE Dept.,Nalla Malla Reddy Engineering College,Hyderabad.
[2]Assistant Professor in EEE Dept.,Nalla Malla Reddy Engineering College, Hyderabad.
[3]Assistant Professor in EEE Dept.,Nalla Malla Reddy Engineering College, Hyderabad.
[1]pagidimarrik@gmail.com [2]laxmi.devam@gmail.com [3]sushma.vidyapuram@gmail.com

Abstract- Photovoltaic (PV) inverters become more and more widespread within both private and commercial circles. These grid-connected inverters convert the available direct current supplied by the PV panels and feed it into the utility grid. There is a strong trend in the photovoltaic inverter technology to use transformerless topologies in order to acquire higher efficiencies combining with very low ground leakage current. In order to limit the ground leakage current (which deteriorates the power quality and generates EMI), new converter topologies have been proposed. The proposed concept is verified by using MATMAL/SIMULINK software and the corresponding results are presented.

Key words- Active power filter (APF), one-cycle control, power-factor correction (PFC), power quality control.

I.INTRODUCTION

PHOTOVOLTAIC (PV) inverters become more and more widespread within both private and commercial circles. These grid-connected inverters convert the available direct current supplied by the PV panels and feed it into the utility grid. There are two main topology groups used in the case of grid-connected PV systems, namely, with and without galvanic isolation [1]. Galvanic isolation can be on the dc side in the form of a high-frequency dc–dc transformer or on the grid side in the form of a big bulky ac transformer. Both of these solutions offer the safety and advantage of galvanic isolation, but the efficiency of the whole system is decreased due to power losses in these extra components. In case the transformer is omitted, the efficiency of the whole PV system can be increased with an extra 1%–2%. Transformerless PV inverters use different solutions to minimize the leakage ground current and improve the efficiency of the whole system, an issue that has previously been treated in many papers [2]–[9]. In order to minimize the ground leakage current through the parasitic capacitance of the PV array, several techniques have been used. One of them is to connect the midpoint of the dc-link capacitors to the neutral of the grid, like the half-bridge, neutral point clamped (NPC), or three-phase full bridge with a split capacitor topology, thereby continuously clamping the PV array to the neutral connector of the utility grid. Half-bridge and NPC type of converters have very high efficiency, above 97%, as shown in [6]. Furthermore, the topology proposed in [6]

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reduces the dc current injection, which is an important issue in the case of transformerless topologies and is limited by different standards. The non injection of dc current into the grid is topologically guaranteed by adding a second capacitive divider to which the neutral terminal of the grid is connected. An extra control loop is introduced that compensates for any dc current injection, by controlling the voltage of both capacitive dividers to be equal. A disadvantage of half-bridge and NPC type of converters is that, for single-phase grid connection, they need a 700-V dc link. In this paper a solution was proposed for the particular converter architecture named UniTL .

II. TRANSFORMERLESS FULL-BRIDGE TOPOLOGIES

The common-mode voltage variations can greatly affect the ground leakage current that flows through the parasitic capacitance of the PV array. In full-bridge topologies, additional switches are inserted either in the DC or in the AC converter side, in order to decouple the grid from the DC source during the freewheeling phases. The existing full-bridge solutions can be divided in two classes: those that leave the V_{AO} and V_{BO} voltages floating during freewheeling and those that fix these voltages, and therefore V_{cm}, to $V_{BUS}/2$.The latter performs better than the former because it assures a less variation of V_{cm} and, therefore, lower ground leakage current.

A. Topologies That do not Fix V_{AO} and V_{BO} during Freewheeling

Fig.1 presents the full-bridge topology with two additional blocks used alternatively: the former is inserted in the DC converter side and the latter in the AC converter side, both reducing the ground leakage current. The AC decoupling, called Highly Efficient Reliable Inverter Concept (HERIC), is used in Sun ways converters while the DC decoupling, called H5 topology, is used in SMA converters.

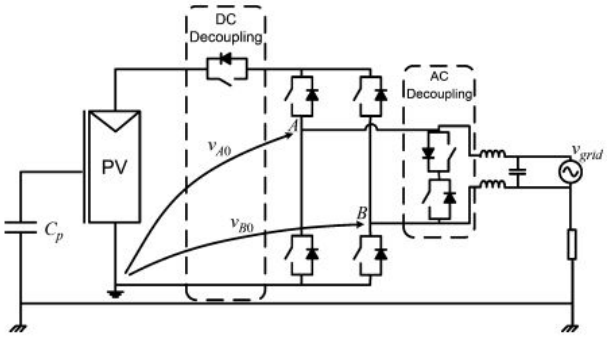

Fig.1. Full-bridge topology with DC and AC decoupling additional blocks

Both decoupling blocks allow, during the freewheeling diode conductions, the disconnection of the grid voltage from the PV array. In the case of symmetrical commutations of the power switches, both topologies fix the V_{cm} to a constant value. Nevertheless, it is important to note that V_{AO} and V_{BO} cannot be clamped in the freewheeling interval, and their levels depend on the parasitic parameters of the freewheeling path and the grid voltage amplitude. For this reasons, in case of asymmetrical commutations, they could have a value very different from $V_{BUS}/2$ (see Fig. 2), leading to high common-mode voltage variation and hence high ground leakage current.

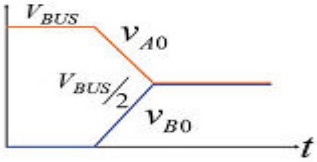

Fig. 2(a).

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V_{AO} and V_{BO} waveforms during the transitionfrom an active to a freewheeling phase- Symmetrical and asymmetrical case.

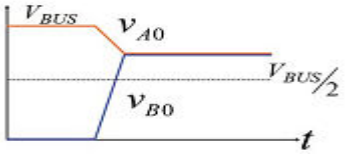

Fig. 2(b).

V_{AO} and V_{BO} waveforms during the transition from an active to a freewheeling phase - powerswitches commutation case

B. Topologies That fix V_{AO} and V_{BO} during Freewheeling

A solution able to keep constant the common mode voltage at the output of the converter during the freewheeling intervals was proposed. It represents an attempt of evolution of the H5 topology. A controllable switch and a capacitor divider are added to form a bidirectional clamping branch which guarantees that the load is clamped to half DC bus voltage in the freewheeling period (see Fig. 3).

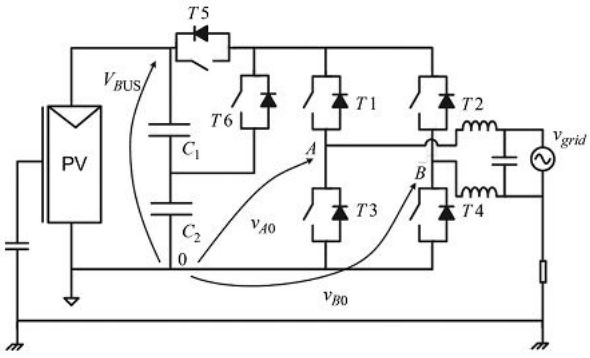

Fig. 3. Topology presented in [6].

The modulation strategy is exactly the same as H5, with T5 and T6 that are switched complementarily at high frequency. It is essential that the DC bus voltage is reliably divided across the capacitors C1 and 2 to guarantee that the midpoint voltage is kept constant to $V_{BUS}/2$. In this way, the capacitors work safely and the freewheeling path is clamped to half DC bus voltage in the freewheeling intervals. In fact, the midpoint voltage may deviate due to any asymmetry of the power switches, gate drivers and parasitic parameters of the circuit. In [6], this deviation is suppressed by some means such as adding a resistor divider (with additional high power losses) or with the introduction of a power converter to balance the midpoint voltage of the DC bus. Obviously, this latter solution implies an increased complexity while an effective solution, instead, should prevent the voltage imbalance without additional power electronics. A different architecture, that implies additional switches in the AC side of the full-bridge, was presented in [3]. The topology is detailed in Fig. 4, showing an extra bidirectional switch made of one IGBT and one diode bridge. This bidirectional switch is clamped to the midpoint of the DC bus capacitors in order to fix V_{AO} and V_{BO} also during the freewheeling interval when all the power switches of the full-bridge are Off. An extra diode is used to protect from short-circuiting the lower DC bus capacitor C2 .

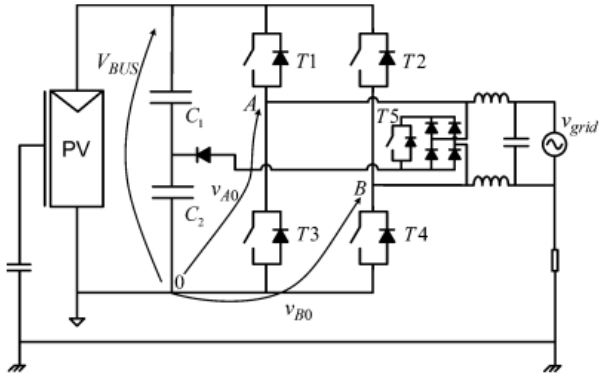

Fig. 4. Topology presented in [3]

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The modulation strategy is similar to that used in HERIC. During the positive half-wave of the grid voltage, T1 and T4 are switched simultaneously at high frequency, supplying a positive voltage to the load, while T2 and T3 are Off. The freewheeling path is achieved by turning On T5 when T1 and T4 are turned Off, clamping the outputs of the inverter to the midpoint of the DC bus ($V_{AO} = V_{BO} = V_{BUS}/2$) . The gate signal of T5 is the complementary gate signal of T1 and T4, with a small dead-time to avoid short-circuiting the DC bus capacitors. During the negative half-wave of the grid voltage, the behavior is dual: the other diagonal of the full-bridge (T2 and T3) is switched instead of the diagonal formed by T1 and T4. Differently from what happens in HERIC topology here it is possible to inject also reactive power to the grid. The midpoint voltage of the DC bus must be controlled because asymmetrical transients of the power switches and variations of the circuit parasitic parameters can unbalance it, resulting in a change of the V_{cm} and security issues. This problematic was not dealt with in [3]. Another full-bridge topology, named H6, with an additional DC decoupling block, was presented in, where two additional switches are inserted in the DC rails. Moreover, two diodes are connected between the DC rails and the midpoint voltage, see Fig. 5.

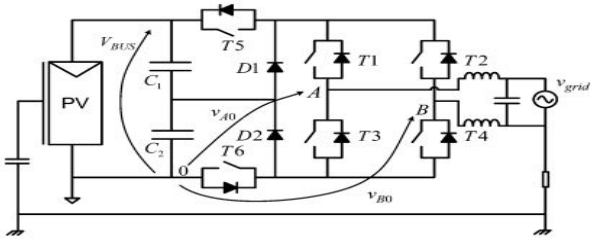

Fig. 5. The H6 topology

This topology is driven by a particular modulation strategy where the DC decoupling transistors, T5 and T6, commutate at the switching frequency, while a diagonal of the full-bridge is kept On during a whole grid voltage semi-period. For example, considering the positive semi-period of the grid voltage, T1 and T4 are always On. In this way, during the freewheeling phase, the DC decoupling transistors are Off, and the four full bridge switches are On; the freewheeling current will then split across the two paths constituted by the transistor T1 and the freewheeling diode of T3, and the transistor T4 and the freewheeling diode of T2. The additional diodes D1 and D2 will fix the common-mode voltage to $V_{BUS}/2$. When the commutations of T5 and T6 are identical the common-mode voltage is kept constant to $V_{BUS}/2$ without any imbalance of the midpoint voltage of the DC Bus. Nevertheless, the balance of the voltage across the capacitor divider is not guaranteed by the modulation strategy in case of asymmetrical commutations of T5 and T6; anyway this issue was not addressed. The UniTL (Unipolar Transformerless) solution was presented, which will be described in the following paragraph. Also in this topology, in case of asymmetrical commutations, Vcm is not constant and the midpoint voltage of the DC bus drifts from its correct value. For this solution, a method for the control of the midpoint voltage of the DC bus, completely integrated into UniTL control strategy, was developed. It permits, also in case of power switches asymmetrical commutations, to assure a limited variation of Vcm regardless the parameters tolerance of the power circuit. In the following paragraphs.

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III. COMPENSATION OFASYMMETRICCOMMUTATIONS FOR UNITL ARCHITECTURE

A.Unitl Architecture

As mentioned in last part of the previous paragraph the UniTL architecture, based on the H6 topology (Fig. 5), was proposed to limit the common-mode current in PV grid-connected systems adopting a full-bridge power converter driven by a unipolar modulation (i.e., three level output voltage and frequency of the output current ripple twice the switching one). This solution relies on decoupling the grid from the DC voltage source during both the freewheeling phases taking place respectively in the high side and in the low side of the full-bridge. To this aim, two additional switches T5 and T6 (the former in the high and the latter in the low side of the full-bridge) are required. The PWM switching strategy is presented in Fig. 6, where x and y are the driving signals of the standard unipolar PWM. Since the converter, in order to improve the efficiency, must inject current into the grid with a unity power factor, two transistors are kept off during the positive and negative semi-periods of the grid voltage, as the injected grid current would flow through the freewheeling diode anyway.

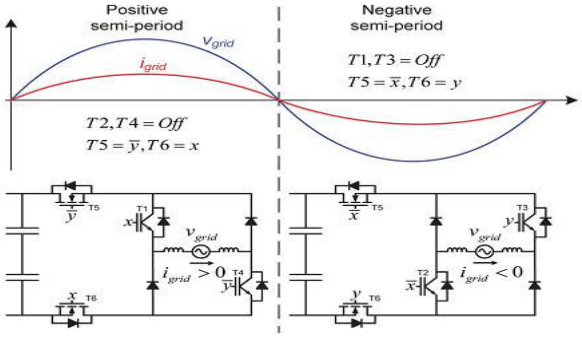

Fig. 6. UniTL modulation switching scheme

During the high-side freewheeling phase (when the injected grid current is flowing through IGBT T1 and the diode D3) T5 is Off and the voltage at the high-side of the full-bridge, in ideal conditions, equals $V_{BUS}/2$. Similarly, during the low-side freewheeling, T6 is Off and the voltage at the low-side of the full-bridge, in ideal conditions, equals $V_{BUS}/2$. It is important to highlight that a small asymmetry in the switching circuit would lead to strong variation of Vcm, up to V_{BUS}, i.e., the same variation of a classical full-bridge driven by unipolar PWM.

B. Additional Clamping Diodes to Reduce Common Mode Voltage Variations

The reduction of the common mode voltage variations due to asymmetric commutations, that take place only during freewheeling phases, is realized by clamping the high or the low sides of the full-bridge (which become floating due to the turnoff of one of the decoupling transistors T5 and T6) to the midpoint voltage V_{MP} with two diodes. Fig. 7 reports the UniTL topology with the two additional diodes ; also the midpoint voltage and current, V_{MP} and I_{MP} , are depicted.

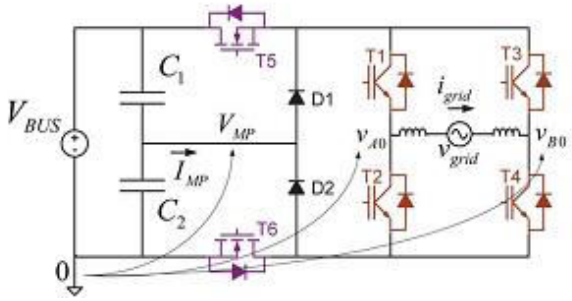

Fig. 7. UniTL solution with additional clamping diodes.

A better solution would involve two additional transistors instead of diodes D1 and D2, but this implies an excessive increase in system

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complexity and cost. It is important to note that the topology with additional diodes is the same of the H6 solution (see Fig. 5), but the switching strategy differs radically from the one proposed. In order to clamp, by uncontrolled switches, both the floating sides of the full-bridge to the midpoint voltage V_{MP}, a little delay $\Delta t_{DC}^{\overline{Hs}}$ is introduced between the commutations of the decoupling switches and the full-bridge ones. Turning off the decoupling switches with a small leading time the current is forced to flow through one of the two added diodes, clamping the floating side of the full-bridge to V_{MP}. This behavior is illustrated in Fig. 8, where and are, respectively, the gate signals of a full-bridge transistor and of a transistor of the DC decoupling block. It is to be noted that, in case of a good balancing, it holds $V_{MP} = V_{BUS}/2$.

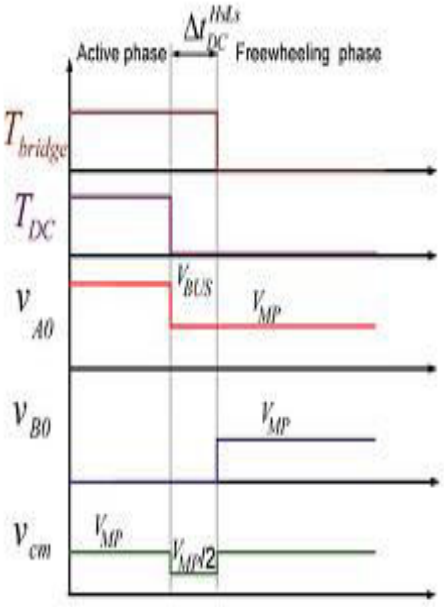

Fig. 8. Example of waveforms for a transition from active phase to High Side freewheeling with the introduction of $\Delta t_{DC}^{\overline{Hs}}$

During the leading time $\Delta t_{DC}^{\overline{Hs}}$, when the full-bridge transistor is On and the decoupling transistor is Off, the freewheeling phase has not started yet, so VAO = VMP and VBO = 0. The common mode voltage is VMP/2, different from the mid-supply voltage $V_{BUS}/2$. Therefore the leading phase, mandatory in case of asymmetric commutations, must be as small as possible.

C. Balancing Strategy of the Midpoint Voltage

During the leading phases in which one of the two added diodes is On, the injected grid current is provided by only one of the two capacitor of the DC bus. With reference to Fig. 7, at the beginning of the high-side freewheeling phase (during the leading time) D1 is On and C2 is discharging, on the contrary, in case of low-side freewheeling, D2 is On and C1 is discharging. In a fully symmetric system, the electric charge extracted from the low-side capacitor equals the charge extracted from the high-side capacitor. Whichever asymmetry in the whole system can cause a drift of the midpoint voltage VMP. A strategy for keeping the midpoint voltage VMP at the mid supply voltage level $V_{BUS}/2$ can be realized making the high side Δt_{Dc}^{Hs} leading time suitably different from the low side one Δt_{Dc}^{Ls}. This allows to control the amount of charge extracted from the two capacitors, balancing the system. This strategy can be embedded in a feedback control system, which modifies Δt_{Dc}^{Hs} and Δt_{Dc}^{Ls} in order to prevent the drift of the midpoint voltage VMP from the correct mid-supply voltage $V_{BUS}/2$. The block scheme of the balancing strategy is shown in Fig.9 , where the power converter, connected to the grid through a simple LC filter, is presented.

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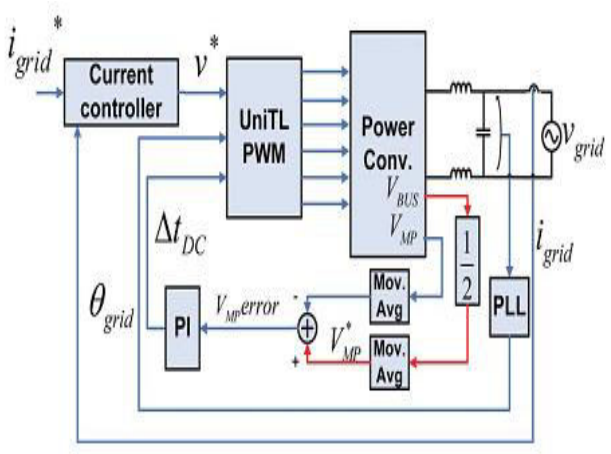

Fig. 9. Block scheme of the balancing strategy

VI.MATLAB MODELING AND SIMULATION RESULTS

Here simulation is carried out in different conditions, in that 1) Proposed Bi-Polar Asymmetric Converter without Clamping Circuit 2) Proposed Bi-Polar Asymmetric Converter with Clamping Circuit 3) Proposed Bi-Polar Asymmetric Converter with Clamping Circuit using PV Source

Case 1: Proposed Bi-Polar Asymmetric Converter without Clamping Circuit

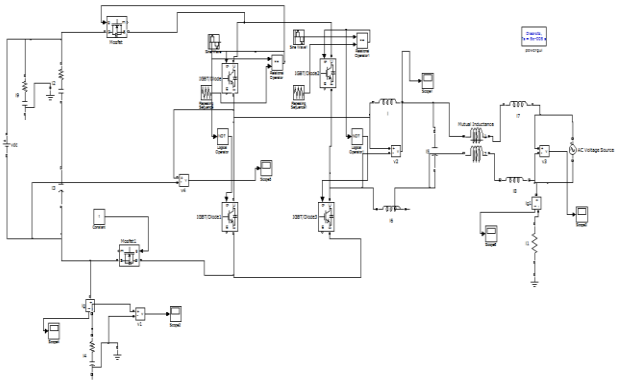

Fig.10 Matlab/Simulink Model of Proposed Bi-Polar Asymmetric Converter without Clamping Circuit

Fig.10 shows the Matlab/Simulink Model of Proposed Bi-Polar Asymmetric Converter without Clamping Circuit using Matlab/Simulink Package.

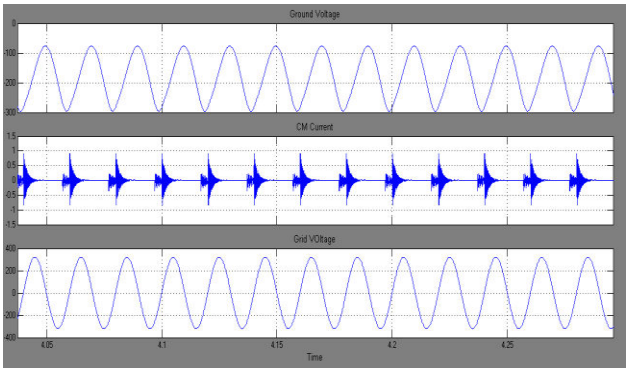

Fig.11 Ground Voltage, Common Mode Current, Grid Voltage

Fig.11 shows the Ground Voltage, Common Mode Current, Grid Voltage of Proposed Bi-Polar Asymmetric Converter without Clamping Circuit.

Case 2: Proposed Bi-Polar Asymmetric Converter with Clamping Circuit

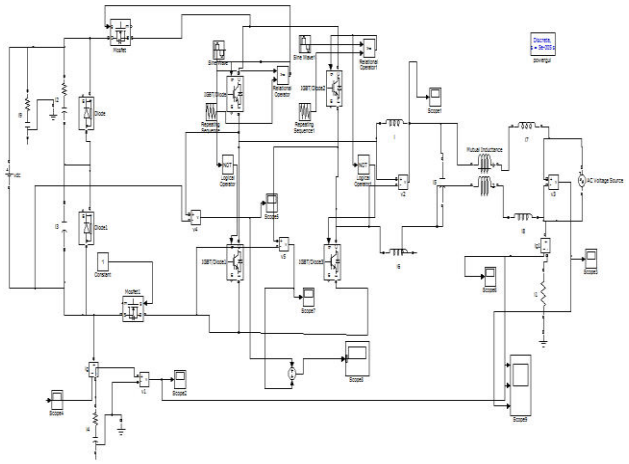

Fig.12 Matlab/Simulink Model of Proposed Bi-Polar Asymmetric Converter without Clamping Circuit

Fig.12 shows the Matlab/Simulink Model of Proposed Bi-Polar Asymmetric Converter with

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Clamping Circuit using Matlab/Simulink Package.

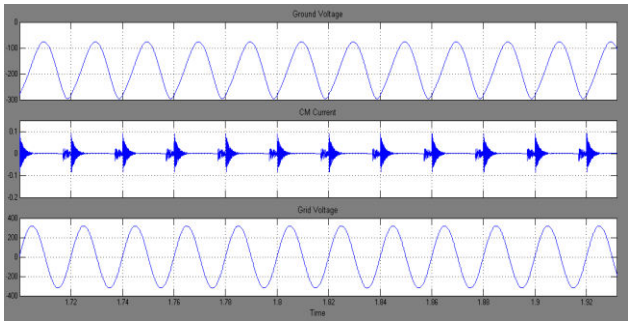

Fig.13 Ground Voltage, Common Mode Current, Grid Voltage

Fig.13 shows the Ground Voltage, Common Mode Current, Grid Voltage of Proposed Bi-Polar Asymmetric Converter with Clamping Circuit using Diodes.

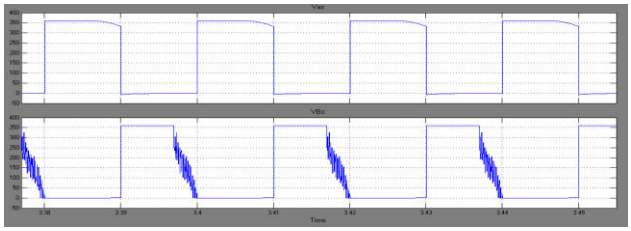

Fig.14 VAo & VBo of Proposed Bi-Polar Asymmetric Converter with Clamping Circuit using Diodes

Case 3: Proposed Bi-Polar Asymmetric Converter with Clamping Circuit using PV Source.

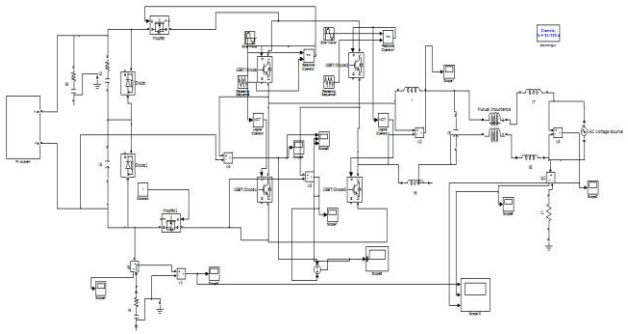

Fig.15 Matlab/Simulink Model of Proposed Bi-Polar Asymmetric Converter without Clamping Circuit with PV Source

Fig.15 shows the Matlab/Simulink Model of Proposed Bi-Polar Asymmetric Converter with Clamping Circuit with PV Source using Matlab/Simulink Package.

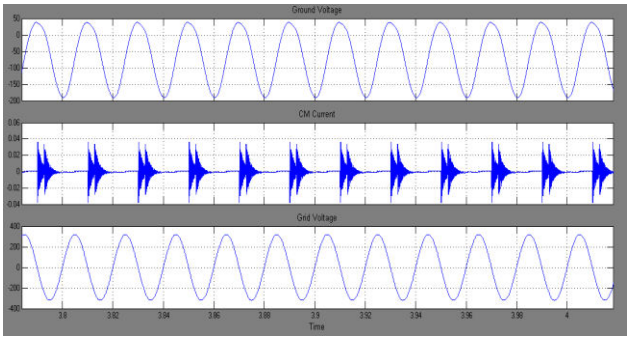

Fig.16 Ground Voltage, Common Mode Current, Grid Voltage

Fig.16 shows the Ground Voltage, Common Mode Current, and Grid Voltage of Proposed Bi-Polar Asymmetric Converter with Clamping Circuit using Diodes with PV Source.

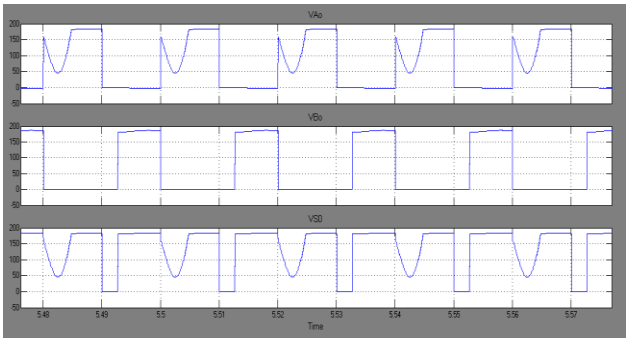

Fig.14 VAo & VBo ,Vsa of Proposed Bi-Polar Asymmetric Converter with Clamping Circuit using Diodes with PV Source

VI.CONCLUSION

With the increase in load demand, the Renewable Energy Sources (RES) are increasingly connected in the distribution systems which utilizes power electronic Converters/Inverters. Renewable energy systems such as PV, solar thermal electricity such as dish-stirling systems, and WT are appropriate solar and wind technologies that can

be considered for electric power generation.The most up to date topologies of grid-connected transformerless photovoltaic converters rely on the use of additional switches to fix the common mode voltage at the output of the power converter. Nevertheless, correct operations need a symmetric switching behavior during the freewheeling phases in order to guarantee a low level of common mode current (ground leakage current). Parameters tolerance and differences in power devices switching times can lead to asymmetrical switching behavior, increasing the common mode current (ground leakage current). This paper proposed a solution for the power converter topology. It clamps, during freewheeling phases, the floating sides of the full-bridge to the midpoint supply voltage , realized with the series of two capacitors are able to effectiveness and robustness with respect to asymmetries in power switches turn-on and turnoff.

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