Paper Authors

G.SRAVANTHI, B.SWETHA, R.KALPANA, G.SANDYA RANI

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per UGC Guidelines We Are Providing A Electronic Bar Code

A COMPARATIVE ANALYSIS OF A THREE PHASE NEUTRAL POINT CLAMPED MULTILEVEL INVERTER

G.SRAVANTHI[1] B.SWETHA [2] R.KALPANA[3] G.SANDYA RANI [4]

[1,2,3] B TECH Students, Department of EEE, Princeton Institute of Engineering & Technology For Women, Hyderabad, Telangana, India.

[4] Assistant Professor, Department of EEE, Princeton Institute of Engineering & Technology For Women, Hyderabad, Telangana, India.

ABSTRACT:

Three-level Neutral-Point Clamped inverter has become established to be a preferred topology for medium-power motor drive applications operating at several kilovolts. Still several researches continue to find solutions to the problem of maintaining a stable neutral-point voltage in the converter. This paper presents the analysis and simulation of a three-level diode-clamped multilevel inverter, employing a sine-triangle modulator with addition of continuous variable offset voltage which regulates the midpoint potential of the dc bus. By maintaining dc-bus voltage balance, a significant reduction in the voltage distortion at the neutral point and also allowing a definitive reduction in the required dc bus capacitance. The effectiveness of the Pulse Width Modulation (PWM) strategies developed with continuous offset addition is demonstrated by MATLAB/SIMULINK based simulation presented in this paper

Keywords: Multi level inverter, 5level inverter, MATLAB, RES network.

1. INTRODUCTION

Multilevel converters provide more than two voltage levels. And general topology of the multi-level inverter can achieve a balance between the level of effort in itself, regardless of the drive control and load characteristics. The concept was introduced multi-level inverters since 1975. The applications are diverse and affect a wide field of electrical engineering from a few watts to several hundred megawatts. They are devoted to medium and high-voltage for current applications. The output quality of the current and voltage of multilevel inverter can be determined by high frequency switching techniques. The semiconductor power (e.g. GTO or IGBT high caliber) usually operate at relatively low frequencies. [1]. The structure of the nine-level inverter is most suitable, as compared to the conventional structure, since the voltages and currents output has a much lower harmonic distortion. The voltage of each switch is half and the chopping frequency is lower [2]. Multilevel inverter topologies are the Neutral-Point Clamped (NPC) inverters (or Diode-Clamped inverters), the cascaded H-bridge inverters (CHB), and the Flying

Capacitor (FC) inverters (or Capacitor Clamped inverters).

OVER VIEW:

Diode clamped/Neutral point clamped multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium voltage energy control. The structure of diode clamped inverters allows them to reach high voltages and therefore lower voltage rating devices can be used. As the number of levels increases the synthesized output waveform has more steps producing a very fine stair case wave and approaching very closely to the desired sinusoidal wave.
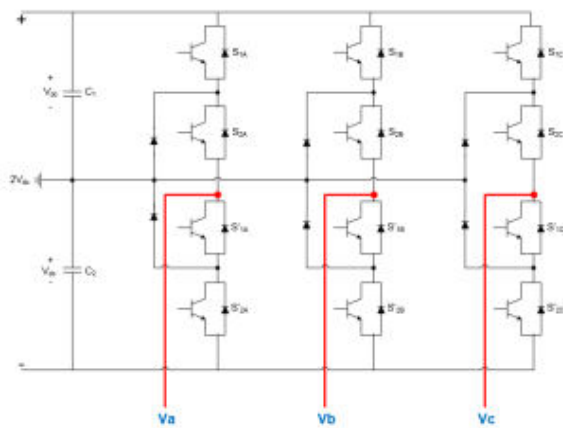

Fig.1.1. Three-Level NPC Multilevel Inverter.

2. LITERATURE SURVEY

The term multilevel thus begins with the three-level inverter [3]. In 1975, the multilevel concept introduced itself by proposing a cascaded inverter [4]. For this series of power semiconductor switches, DC sources with low magnitudes are used. Even though the cascaded multilevel inverter came out earlier, it found its application in 1990. This resulted in a neutral point clamped multilevel inverter (NPC-MLI), which became the first generation of multilevel technology [3]. The main objective of recent novel topologies is to reduce the number of components required as compared to c1assical topologies. Recently introduced and updated topologies have been reviewed. However, the novel topologies have some drawbacks, such as the loss of modularity, problems with switching frequencies and restrictions on the modulation and control method. Many different modulation methods exist to control multilevel inverters. These are sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM) and space vector modulation (SVM), etc. These methods can be c1assified according to the switching frequencies used. In industrial applications, the SPWM control method is very popular. Based on the c1assical SPWM for multilevel technology, various multi-carrier techniques have been developed [5]. They are helpful in reducing the harmonics in the output waveforms. The analysis of the MATLAB simulated models of a three and five-level NPC multilevel inverter in this paper, utilizes the SPWM control method. The striking features of multilevel inverters are as follows [6]:

1) They can generate output voltages with extremely low distortion and a lower dv/dt.

2) They draw input current with very low distortion.

3) They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, they use sophisticated modulation methods in eliminating CM voltages.

4) They can operate with a lower switching frequency

3. RELATED STUDY

Hence diode clamped multilevel inverters offer a better choice at a high power end because the high volt-ampere ratings are possible with these inverters without the problems of high dv/dt and the other associated ones. NPC inverter has an inherent problem of unbalanced voltages across dc-link capacitors due to load unbalancing, non uniform distribution of charges, and non-identical properties of dc-link capacitors provided from the manufacturer. Several open loop strategies have been proposed for the reduction of the harmonic content. The authors have proposed two ways of mid-point voltage balancing in NPC three level inverters. One way of voltage balancing based upon the addition or modification of hardware circuitry to the inverter, which modify the charging and discharging currents of DC-link capacitors. Second way of voltage balancing is based upon modification in inverter control strategy based on PWM schemes. Many carrier and SVPWM based strategies have been proposed for the modulation of theses inverters.

A closed loop control strategy, which reduces the harmonic content as well as maintains voltage stability in the neutral point, is presented in this paper. Closed loop regulator is based on injecting offset magnitude to the modulating signal as a function of a control input that corrects any existing imbalance. In this paper main considerations given to regulate the voltage imbalance of NPC inverter employing sine triangle modulator in conjunction with a closed-loop controller, which considerably reduces the harmonic distortions in the output voltage waveform, resulting in reduction of the required dc bus capacitance.

4. PROPOSED SYSTEM

The development of multilevel inverter topologies appeared a challenge to extend existing modulation methods (switch control) to the multilevel case. The methods that have been developed had to consider the additional complexity of the inverters having more power electronic devices to control the additional switching states. Amongst the commonly used modulation techniques, SPWM is simple and gives high performance by using the phase-shifting technique to reduce the harmonics in the load voltage.

Must be a PWM signal frequency is much higher than those of the modulation signal, the fundamental frequency to generate PWM signals addressed as follows:
1) Sinusoidal Pulse Width Modulation (SPWM).
2) Space vector PWM special switching sequence of three of the upper power of the three-phase power inverter. It can be used to expand the scope of control

strategies at the two higher levels The method of pulse width modulation PWM is the most common for comparing a modulating wave (generally sinusoidal). The PWM inverters are advancing to the previous method which is square-wave inverter in the following points:

(i) The ability of reducing total harmonic distortion,

(ii) Capable of controlling the output voltage,

(iii) higher power quality factor. The phenomenon of rapid and repeated switching at high speed causes the frequency of appearance of lowest order harmonic in the output voltage. The techniques of the carrier PWM approaches with several variant of phase relationships for a (MLI)[5-6] are given as follows:

1) The carriers are in phase disposition (IPD).

2) Phase opposition disposition (POD). If the triangular carriers are arranged in phase opposition, then the method is phase opposition disposition (POD) that is shifted by 1800 from those carriers if they are below the zero reference. This method more efficient than the PD of the harmonic point of view low values of the modulation index.

3) The carrier arranged in triangular phase as Phase Disposition (PD). Each of the carriers is shifted by $2\pi/$ (N-1) radians.
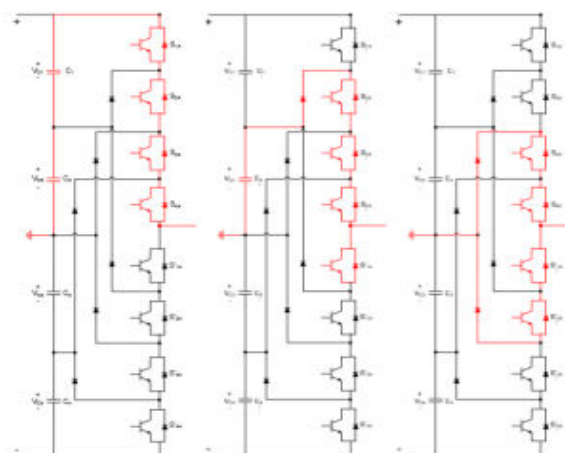

Fig.4.1. Proposed system.

SIMULATION RESULTS:

The SPWM switching technique is commonly used in industrial applications. The techniques are characterized by constant amplitude pulses with different duty cycles for each period. The width of these pulses are modulated to obtain inverter output voltage control and to reduce its harmonic content. SPWM is the most used method in motor control and inverter application [9]. In the SPWM technique, three sine waves and a high frequency triangular carrier wave are used to generate the PWM signal [9]. Hence, the switching signal is generated by comparing the sinusoidal waves with the triangular wave.
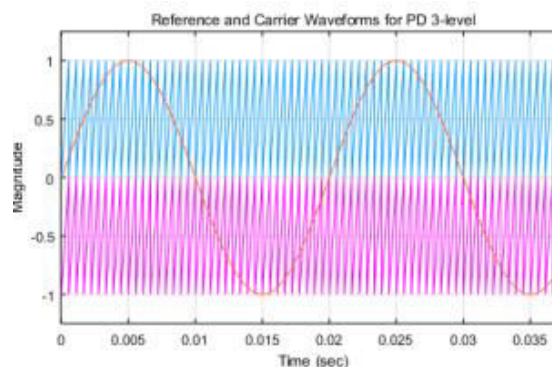

Fig.4.2. Output results.

The output voltage waveform of a three level NPC inverter with an R load. The FFT analysis tool on MATLAB simulated the output voltage waveforms. The THD of this output waveform is 35.45 % with a fundamental (50 Hz) peak value of 346.9.
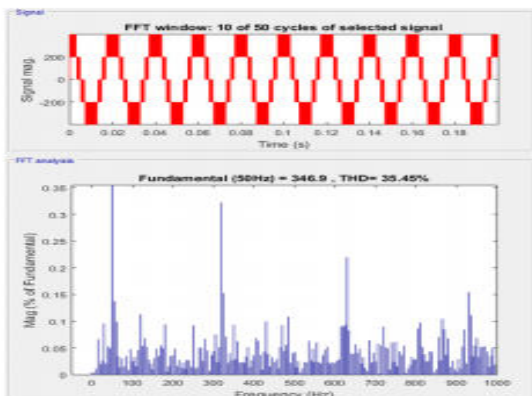

Fig.4.3.Three level output results.

The output voltage waveform of a five-level NPC inverter with an R-L load. The THD of this output waveform is 20.43 % with a fundamental (50 Hz) peak value of 694.7. The R-L load had minimum effect to the THD value.
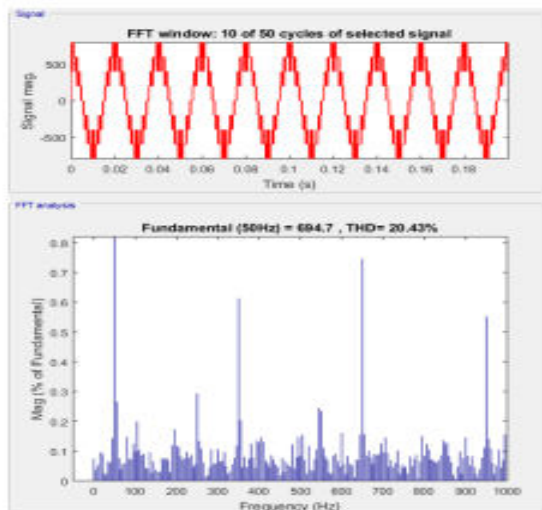

Fig.4.4. Output Voltage and FFT Analysis of a Five Level NPC MLI with an R-L Load.

5. CONCLUSION

This paper presents the comparison of a three phase, three-level and five-level NPC multilevel inverter. MATLAB/Simulink models for these multilevel inverters, together with simulation results indicate that the generated voltage spectrum for a five-level inverter has improved. The THD for a three-level inverter is 35.45 % and for a five-level inverter it is 20.73 %. As a result, the five- level inverter harmonic content is less than that of a three-level inverter. The use of multilevel inverters as opposed to the use of two-level inverters, made its breakthrough in obtaining lower THD in output voltage to lower the switching power losses.

REFERENCES

[1] P.K.Chaturvedi, S. Jain, Pramod Agrawal " Modeling, Simulation and, Analysis of Three level Neutral Point Clamped inverter using mat lab/ Simulink/Power System Blockst"

[2] G.Bhuvaneshwari and Nagaraju " Multilevel inverters – a comparative study" vol .51 No.2 Mar – Apr 2005.

[3] Tolbert. L. M and Pend. F. Z, "Multilevel Converter as a Utility Interface for Renewable Energy Systems," IEEE Power Engineering Society Meeting, Vol. 2, pp. 1271- 1274,2000.

[4] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls and applications," IEEE Transactions of Industrial Electronics, vol.49, no. 4, pp. 724-738, Aug. 2002

[5] Akhila.A,Manju Ann Mathews, "Simulation and Analysis of Diode clamped
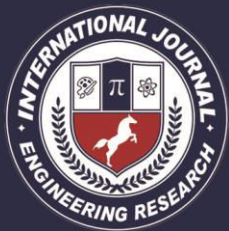
and Modular Multilevel Inverters Using SPWM," International Journal of Advanced Research in Electrical Electronics and Instrumentation Engineering Trends and Technology,vol.5,no.6,pp.4677-4686,Jun. 2016.

[6] A. Nabae, I. Takahashi, and H. Akagi, "A new neutralpoint clamped PWM inverter," IEEE Trans. Ind. Applicant. Vol. IA-17, pp. 518– 523,Sept. /Oct. 1981.

[7] B. Urmila, D. Subbarayudu, "Multilevel inverters: A comparative study of pulse width modulation techniques," International Journal of Scientific and Engineering Research, vol. 1, issue 3, pp. 1-5, Dec. 2010.

[8]JoseRodriguez,Leopoldo.G.Franquelo,Sa mirKouro,Jose.I.Leo

n,Ramon.C.Portil"Multilevel Converters an Enabling Technology for High power Applications," IEEE Trans. Ind. Applicat., vol. 97, no. 11, pp. 1786-1816,Nov 2009.

[9] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage source converter topologies for industrial medium-voltage drives," IEEE Transactions on Industrial Electronics, vol. 54, no.6, pp. 2930-2942, Dec. 2007.

[10] Kalle Ilves,Antonios Antonopoulost, Staffan Norrga, HansPeter Nee "A New Modulation Method for the Modular Multilevel Converter Allowing Fundamental Switching Frequency," IEEE Trans. Power Electron., vol. 27, no. 8, pp. 3482–3494, Aug. 2012.