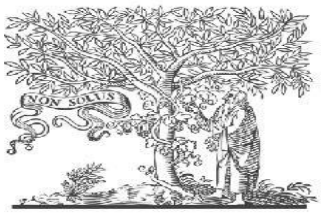
International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

COPY RIGHT



ELSEVIER SSRN

IJIEMR Transactions, online available on 5th Oct 2021. Link
:http://www.ijiemr.org/downloads.php?vol=Volume-10&issue=ISSUE-10

DOI: 10.48047/IJIEMR/V10/I10/33

Title **DESIGN A HIGH SPEED AND ACCURATE BOOTH MULTIPLIER FOR COMMUNICATION APPLICATIONS**

Volume 10, Issue 10, Pages: 195-201

Paper Authors
ANKEM SUDARSINI, BALA KRISHNA KONDA

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per UGC Guidelines We Are Providing A Electronic Bar Code

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

DESIGN A HIGH SPEED AND ACCURATE BOOTH MULTIPLIER FOR COMMUNICATION APPLICATIONS

[1]ANKEM SUDARSINI, [2]BALA KRISHNA KONDA
[1]M.Tech scholar, Dept of ECE, Eluru College of Engineering & Technology, Duggirala Village, Eluru, Andhra Pradesh, India
[2]Assistant Professor, Dept of ECE, Eluru College of Engineering & Technology, Duggirala Village, Eluru, Andhra Pradesh, India

ABSTRACT: In this paper, design a high speed and accurate booth multiplier for communication applications is implemented. Basically, booth multiplier is used in the applications of DSP, FFT and ALU to increase the speed of operation and reduce the delay. Eelier, approximate booth multiplier design is implemented. This approximate booth multiplier gives error values at the ouput. To overcome this accurate booth multiplier is implemented for communication applications. Hence from simulation results it can observe that the accurate booth multiplier gives effective results in terms of delay, speed and area. This is simulated using Xilinx technology.

Key Words: VLSI, Digital signal processing (DSP), Partial product generation, Partial product reduction, Shifter, rounding.

I.INTRODUCTION

A circuit specially designed for the purpose of doing multiplication of two binary numbers is called as multiplier. In digital processors and several other digital devices employs multipliers for processing of signals. The addition, subtraction and multiplication of two binary numbers are very essential and frequent operations that occur in arithmetic logic units, processors and DSP applications [1]. It is estimated that around 70% of the operations performed in various processors and DSP devices are addition and multiplication. As these operations occur most frequently. The speed of the processor depends upon the speed of the multiplier. Therefore the speed of the multiplier and adder circuits governs the performance of the processors.

Advancements in computer technologies and signal processing developments insist much faster arithmetic units. Several multiplier designs have been proposed so far.

The performance of multipliers is evaluated using parameters like operating speed, cost, and area and delay utilization. In present generation the growth of integrated circuit devices has increased a lot. The Very Large Scale Integrated Chip (VLSI) applications are given as digital signal processing and microprocessors. These applications are most widely used to perform arithmetic operations. Along with that multiplication, subtraction operations are also performed. By using some modules all these operations are performed on the 1 bit full adder circuit.

Approximate adders are implemented in a way to balance the trade-off between accuracy vs. performance/power. The areas of image and video processing appear as good case studies for the use of approximate results. The circuit design is addressed at different levels. The design parameters of the circuit produce good trade off in terms of speed and area [2]. Multiplication has been given careful consideration by utilizing analysts, because of the reality expansion which is essentially bitwise activity among two subject components, and the additional complex tasks, reversal, and might be finished with a few multiplications.

Montgomery's multiplier is classified into three types, they are bit-serial, bit-parallel,

and digit serial architectures. Bit-parallel shape is rapid; however it's far steeply-priced in phrases of vicinity. Bit-serial structure is region efficient. The digit-serial structure is flexible which may change the space and velocity, consequently, it achieves a moderate pace, reasonable price of implementation and hence it is most appropriate for practical use. Montgomery presented a technique for figuring modular multiplication productively. He introduced to move the portrayal of numbers from the Zn to an alternate area, called Montgomery Residual portrayal or Montgomery Domain [3].

Here for the purpose of security, the computers and communication system brought with a demand from private sector [4]. The Montgomery multiplication is the calculation that permits effectively for registering. The expense of the particular duplication is equivalent to three whole numbers which increases in addition to the expense of the change in the Montgomery area. Yet, in the event that the large scale task is an exponentiation, at point the change cost is insignificant contrasted with the quantity of augmentations executed in the Montgomery area. In the process of Montgomery multiplication, pre-processing unit and post-processing units are used [5]. The pre-processing unit produces N-Residue operands and in the same way post processing unit will eliminate the constant factor 2n. Hence to form N-Residue operands in the system, modular exponentiation is used.

Here for the purpose of supplanting division activities, shifting tasks are used. After the shifting process the least critical bits will remain zero. Now to eliminate these bits in the modular multiplication, add products are used. After the process of eliminating the bits, the remaining bits are augmented in the multiplicand. Hence from this it can observe that the process of multiplicand is completed. Now the output is obtained after the subtraction of bits. Here if the bits are increased then Montgomery bits also increases. At last the multiplicand bits are controlled without the use of subtraction calculation.

II. STRATEGY OF MULTIPLIER

Array multiplier is circuit which uses array of AND gates and full adders to perform multiplication of binary operands is called as Array multiplier. It is one of the widely used fundamental algorithms for multiplication. The array of AND gates present in the multiplier performs AND operation of multiplicand with each bit of the multiplier. These partial products produced by AND gates are shifted to left according to the position of multiplier bit. The shifted partial products are summed up with N-1 adders in parallel. However, addition performed in parallel there is large delay is introduced by CSAs. This is due to carry propagation in sequence of adders. The CSAs are replaced with Carry save adders (CSA) to reduce the delay in array multiplication process. The CSAs compress the three number addition to n number addition so, that three operands are added at a time.

The multiplier delay in addition of partial products like in array multiplier is reduced by some multiplication techniques based on shift and add techniques. The multiplier bit decides whether to shift the partial product or add the multiplicand to the product. Here we explained how conventional addition is performed. In order to fasten the multiplication procedure custom multiplication process divided into two

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

sections. The first section focuses on producing partial products and the second section focuses on accumulation and addition of the partial products. Before adding of partial products they need to be aligned in their corresponding positions by shifting.

Booth technique is the most dominating method of multiplication for signed numbers. In this technique multiplication of both positive and negative operands are similarly performed. This technique is based on add-shift algorithm. In conventional multiplication procedures the number of partial products depends upon the operand size of the multiplier. If the size of the multiplier increases number of partial products also increases resulting in large delay when they get added to produce the end result. Since the delay of the multiplier is dominated by addition operation he focused to reduce the number of additions occurs in a multiplication task.

The multiplication of signed numbers must be observed through the operation to produce the appropriate sign of the result. Whereas in case of unsigned numbers there is no need to think about sign of the operands. If the multiplication of signed 2's complement numbers is performed in the way of positive number multiplication would results in incorrect output. Therefore, booth's algorithm introduced a technique to perform multiplication of signed numbers with the sign protection. In this technique the LSB bits of the multiplier are bi and bi-1 are tested at every clock cycle. If the two bits are zeros results shifting one bit position of the multiplier to the right. In case of sequence of 1's arithmetic operations like addition and subtraction are need to be performed at the edges of block of ones while changing from 1 to 0 and 0 to 1.

III. EXISTED SYTEM

The below figure (1) shows the block diagram of fixed width booth multiplier. The FWBM is surrounded by the DST circuit and consists of a Booth encoder, a carry-save adder (CSA) tree, and a parallel prefix adder. The CSA, which consists of either full adders or half adders, adds the partial products from the MP, T Pma, and the estimated T Pmi in all the low-error FWBMs tested. Finally, the high-speed parallel prefix adder calculates the products Pd, and the final results Pq are obtained by using the DST circuit.

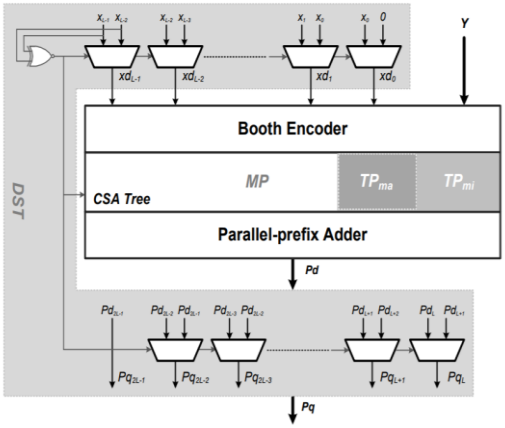


Fig. 1: BLOCK DIAGRAM OF FIXED WIDTH BOOTH MULTIPLIER

There are two DST (Data Scaling Technology) Modules (DS Module and reDS Module). One of them is inserted above the low-error FWBM, and the other is inserted below the FWBM. The DS Module shifts the Scale bit according to the redundant bit of the multiplicand X, and the reDS Module reconstructs the results according to the corrected weight.

The Scal values are calculated using the number of redundant bits in the MSBs of the multiplicand X. In general, the range of Scal is

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

[0, L − 1]. However, a high value of Scal requires numerous bits to be shifted, which implies that more calculations and an increased circuit area would be required. Thus, a limited shift bits (DSb) factor is introduced to limit the value of Scale.

IV. PROPOSED SYSTEM

The below figure (2) shows the block diagram of accurate booth multiplier. The entire system is divided into following modules. The following modules are inputs A and B, partial products reduction and generation, shifter, rounding and final output. This operation is mainly used in the coprocessor in parallel format. This system provides the functionality for coprocessor. First the alignment of partial products generator will be done. After that partial products takes this registers and generates the propagate and generate signals. After this multiplication operation is performed based on look up table. Now shifter will shift the data words by sequential bits. Now this bits perform the rounding operation and gives the final product.

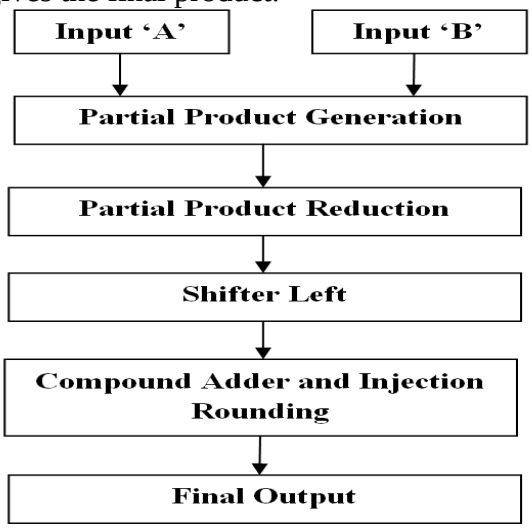


Fig. 2: BLOCK DIAGRAM OF ACCURATE BOOTH MULTIPLIER

Partial-Product Multiplication is an alternative method for solving multi-digit multiplication problems. This is a strategy that is based on the distributive (grouping) property of multiplication. The first partial product is created by the LSB of the multiplier, the second partial product is created by the second bit in the multiplier, etc. The final partial products are added with a accurate adder circuit.

The usual partial product reduction method consists of using structures based on combinational logic until only two summands are considered. The final addition, in the subsequent stage, produces the final result of the operation. These schemes often make use of some counter and compressor components organized into different topological configurations. There is a huge list of works that deal with improving the performance of these organization

A shifter is a digital circuit that can shift a data word by a specified number of bits without the use of any sequential logic, only pure combinational logic. An adder is a kind of calculator that is used to add two binary numbers. In many computers and other types of processors, adders are used to calculate addresses, similar operations and table indices in the ALU and also in other parts of the processors. Rounding is a fundamental method to reduce the size of a word, such as after arithmetic operations. Rounding is a fundamental method to reduce the size of a word, such as after arithmetic operations.

IV. RESULTS

The below figure (4) shows the RTL schematic of accurate booth multiplier.

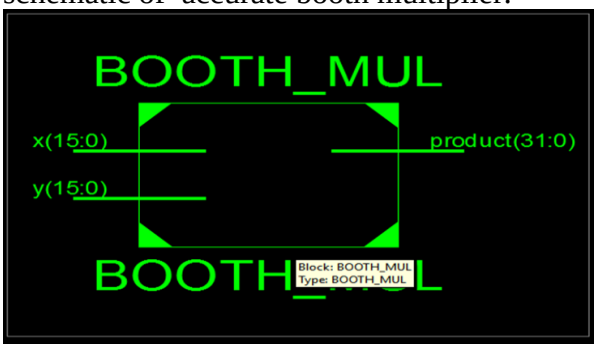


Fig. 3: RTL SCHEMATIC

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

The below figure (5) shows the technology schematic of accurate booth multiplier.

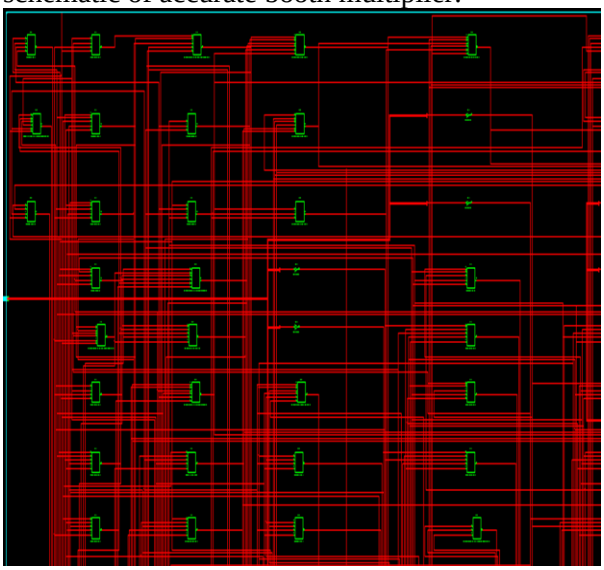


Fig. 4: TECHNOLOGY SCHEMATIC

The below figure (6) shows the output waveform of accurate booth multiplier. The output is obtained as "00000000000000000000000000 1100"".

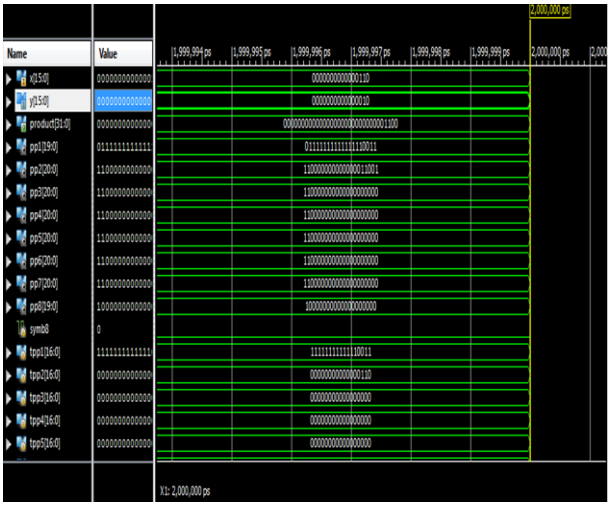


Fig. 5: OUTPUT WAVEFORM

The below figure (7) shows the comparison of fixed width booth multiplier and accurate booth multiplier. Compared with fixed width booth multiplier, accurate booth multiplier will reduces the total delay in very effective way.

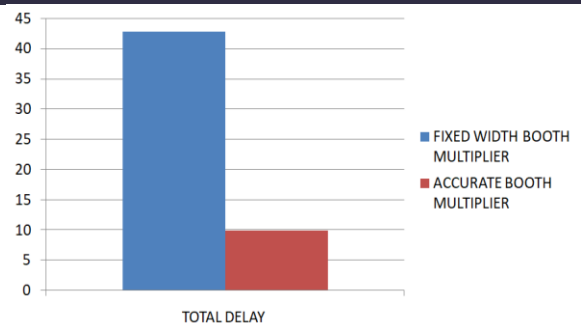


Fig. 6: COMPARISON OF TOTAL DELAY

The below figure (8) shows the comparison of fixed width booth multiplier and accurate booth multiplier. Compared with fixed width booth multiplier, accurate booth multiplier reduces the logic delay in very effective way.

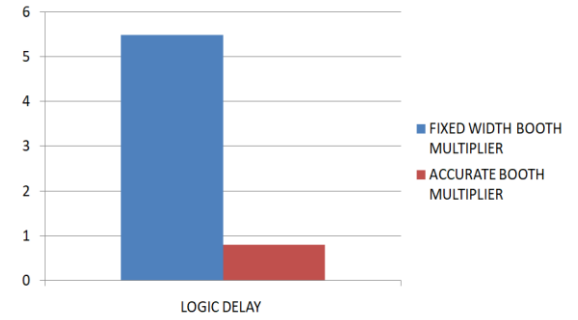


Fig. 7: COMPARISON OF LOGIC DELAY

The below figure (9) shows the comparison of fixed width booth multiplier and accurate booth multiplier. Compared with fixed width booth multiplier, accurate booth multiplier er reduces the route delay in very effective way.

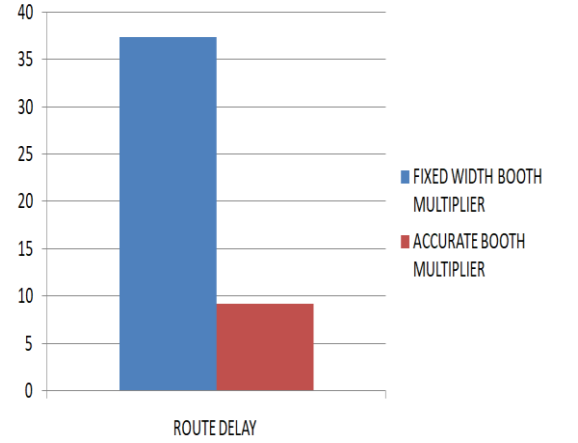


Fig. 8: COMPARISON OF ROUTE DELAY

The below figure (10) shows the comparison of fixed width booth multiplier and accurate booth

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

multiplier. Compared with fixed width booth multiplier, accurate booth multiplier reduces the usage of memory in very effective way.

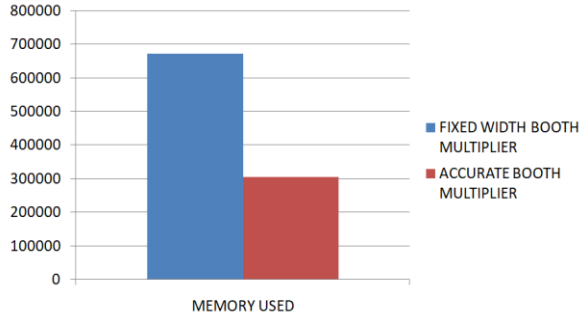


Fig. 9: COMPARISON OF MEMORY USED

V. CONCLUSION

Hence in this paper was high speed and accurate booth multiplier for communication applications were implemented. The accurate booth multiplier performs the multiplication in very fast. The proposed system will reduce the switching activities that are produce in the system. To reduce the delay partial product unit is introduced. Hence the memory of complexity is reduced in accurate booth multiplier. This system is mainly used in the applications of low delay and high speed applications.

VI. REFERENCES

[1] Yuan-Ho Chen, "Improvement of Accuracy of Fixed-Width Booth Multipliers Using Data Scaling Technology", 1549-7747 (c) 2020 IEEE.

[2] "Power-delay-area efficient design of vedic multiplier using adaptable manchester carry chain adder", Raghava Katreepalli , Themistoklis Haniotakis, 2017 International Conference on Communication and Signal Processing (ICCSP).

[3] "Low power array multiplier using modified full adder", S. Srikanth , I. Thahira Banu , G. Vishnu Priya , G. Usha, 2016 IEEE International Conference on Engineering and Technology (ICETECH).

[4] "Design of high speed multiplier using modified booth algorithm with hybrid carry look-ahead adder"
R Balakumaran , E Prabhu, 2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT).

[5] "Design of area and delay efficient Vedic multiplier using Carry Select Adder", G. R. Gokhale , S. R. Gokhale, 2015 International Conference on Information Processing (ICIP).

[6] "Design of ultra low power multipliers using hybrid adders", Thottempudi Pardhu , N.Alekhya Reddy, 2015 International Conference on Communications and Signal Processing (ICCSP).

[7] "Comparative study of performance vedic multiplier on the basis of adders used", Josmin Thomas , R. Pushpangadan , S Jinesh, 2015 IEEE International WIE Conference on Electrical and Computer Engineering (WIECON-ECE).

[8] "Design of area efficient and low power multipliers using multiplexer based full adder"
S. Murugeswari , S. Kaja Mohideen, Second International Conference on Current Trends In Engineering and Technology - ICCTET 2014.

[9] "A vertical-MOSFET-based digital core circuit for high-speed low-power vector matching", Yitao Ma , Tetsuo Endoh , Tadashi Shibata, 2011 International SoC Design Conference.

[10] H. Hinkelmann, P. Zipf, J. Li, G. Liu, and M. Glesner, "On the design of reconfigurable multipliers for integer and Galois field multiplication," Microprocessors Microsyst., vol. 33, no. 1, pp. 2–12, Feb. 2009.

ANKEM SUDARSINI completed B.Tech from Eluru College of Engineering and Technology, Duggirala Village, Eluru, Jntuk and pursuing M.Tech from Eluru College of Engineering and Technology, Duggirala Village, Eluru, Jntuk. Her M.Tech specialization is VLSI design.

BALA KRISHNA KONDA completed B.Tech from Sri Vasavi engineering college, tadepalligudem and M.Tech from Sri Vasavi engineering college, tadepalligudem. His area of interest is low power VLSI design. At present he is working as assistant professor in Eluru College of Engineering and Technology, Duggirala Village, Eluru, Jntuk.