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CONTROL OF REDUCED RATING DYNAMIC VOLTAGE RESTORER WITH BATTERY ENERGY STORAGE SYSTEM

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ABSTRACT

In this paper, different voltage injection schemes for DVRs (Dynamic Voltage Restorers) are analyzed with particular focus on a new method used to minimize the rating of the VSC (Voltage Source Converter) used in DVR. A new control technique is proposed to control the capacitor supported DVR. The control of a DVR is demonstrated with reduced rating VSC. The reference load voltage is estimated using the unit vectors. The SRF (Synchronous Reference Frame) theory is used for the conversion of voltages from rotating vectors to the stationary frame. The compensation of the voltage sag, swell and harmonics is demonstrated using a reduced rating DVR.

Index Terms: Dynamic Voltage Restorer, Power Quality, Unit Vector, Voltage Harmonics, Voltage Sag, Voltage Swell.

I. INTRODUCTION

POWER quality problems in the present day distribution systems are addressed in the literature [1-6] due to the increased use of sensitive and critical equipments such as communication network, process industries, precise manufacturing processes etc. Power quality problems such as transients, sags, swells and other distortions to the sinusoidal waveform of the supply voltage affect the performance of these equipments. The technologies such as custom power devices are emerged to provide protection against power quality problems [2]. Custom power devices are mainly of three categories such as series-connected compensators known as DVR (Dynamic Voltage Restorer), shunt connected compensators such as DSTATCOM (Distribution Static Compensator), and a combination of series and shunt-connected compensators known as UPQC (Unified Power Quality Conditioner) [2-6]. The DVR can regulate the load voltage from the problems such as sag, swell, harmonics etc. in the supply voltages. Hence it can protect the critical consumer loads from tripping and consequent losses [2]. The custom power devices are developed and installed at consumer point to

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meet the power quality standards such as IEEE-519 [7].

Voltage sags in an electrical grid are not always possible to avoid because of the finite clearing time of the faults that cause the voltage sags and the propagation of sags from the transmission and distribution systems to the low-voltage loads. Voltage sags are the common reasons for interruption in production plants and for end user equipment malfunctions in general. In particular, tripping of equipment in a production line can cause production interruption and significant costs due to loss of production. One solution to this problem is to make the equipment itself more tolerant to sags, either by intelligent control or by storing "ride-through" energy in the equipment. An alternative solution, instead of modifying each component in a plant to be tolerant against voltage sags, is to install a plant-wide uninterruptible power supply (UPS) system for longer power interruptions or a DVR on the incoming supply to mitigate voltage sags for shorter periods [8-23]. DVRs can eliminate most of the sags, and minimize the risk of load tripping for very deep sags, but their main drawbacks are their standby losses, the equipment cost and also the protection scheme required for downstream short circuits.

Many solutions and their problems using DVRs are reported such as the voltages in a three phase system are balanced [8] and an energy-optimized control of DVR is discussed in [10]. Industrial examples of DVRs are given in [11] and different control methods are analyzed for different types of voltage sags in [12-18]. A comparison of different topologies and control methods are presented for a DVR in [19]. The design of a capacitor supported DVR that protects sag, swell, distortion, or unbalance in the supply voltages is discussed in [17]. The performance of a DVR with the HFL (High Frequency Link) transformer is discussed in [24]. In this paper, the control and performance of a DVR are demonstrated with a reduced rating VSC (Voltage Source Converter). The SRF (Synchronous Reference Frame) theory is used for the control of the DVR.

II. OPERATION OF DVR

The schematic diagram of a DVR connected system is shown in Fig. 1 (a). The voltage V_{inj} is inserted such that the load voltage, V_{load} is constant in magnitude and undistorted, though the supply voltage V_s is not constant in magnitude or distorted. Fig.1(b) shows the phasor diagram of different voltage injection schemes of the DVR. VL(pre-sag) is a voltage across the critical load prior to the voltage sag condition. During the voltage sag, the voltage is reduced to Vs with a phase lag angle of θ. Now the DVR injects a voltage such that the load voltage magnitude is maintained at the pre-sag condition. According to the phase angle of the load voltage, the injection of voltages can be realized in four ways [19]. V_{inj1} represents the voltage-injected in-phase with the supply voltage. With the injection of V_{inj2}, the load voltage magnitude remains same but it leads V_s by a small angle. In V_{inj3}, the load voltage retains the same phase as that of the pre-sag condition, which may be an optimum angle considering the energy source [10]. V_{inj4} is the condition where the injected voltage is in quadrature with the current and this case is

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suitable for a capacitor supported DVR as this injection involves no active power [17]. However, a minimum possible rating of the converter is achieved by $V_{in}j1$. The DVR is operated in this scheme with a BESS (Battery Energy Storage System).

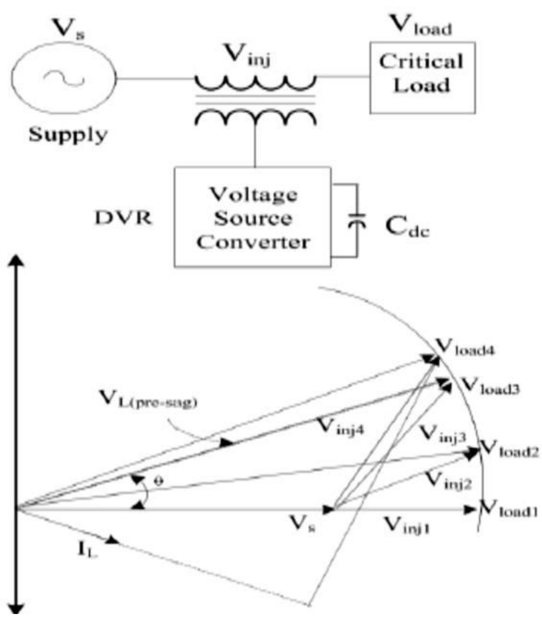

Fig. 1. (a) Basic circuit of DVR, (b) Phasor diagram of the DVR voltage injection schemes.

Fig. 2 shows a schematic diagram of a three-phase DVR connected to restore the voltage of a three phase critical load. A three phase supply is connected to a critical and sensitive load through a three phase series injection transformer. The equivalent voltage of the supply of phase A, (v_{Ma}) is connected to the point of common coupling (PCC) (v_{Sa}) through short circuit impedance (Z_{sa}). The voltage injected by the DVR in phase A (v_{Ca}) is such that the load voltage (v_{La}) is of rated magnitude and undistorted. A three phase DVR is connected to the line to inject a voltage in series using three single-phase transformers, T_r. L_r and C_r represent the filter components used to filter the ripples in the injected voltage. A three-leg VSC with IGBTs (Insulated Gate Bipolar Transistors) is used as a DVR and a BESS is connected to its dc bus.

III. CONTROL OF DVR

The compensation for voltage sags using a DVR can be performed by injecting or absorbing the reactive power or the real power [17]. When the injected voltage is in quadrature with the current at the fundamental frequency, the compensation is made by injecting a reactive power and the DVR is with a self supported dc bus. But, if the injected voltage is in-phase with the current, DVR injects a real power and hence a battery is required at the dc bus of VSC. The control technique adopted should consider the limitations such as the voltage injection capability (converter and transformer rating) and optimization of the size of energy storage.

A. Control of DVR with BESS for Voltage Sag, Swell and Harmonics Compensation

Fig. 3 shows a control block of the DVR in which SRF theory is used for reference signal estimation. The voltages at PCC (v_S) and at load terminal (v_L) are sensed for deriving the IGBTs gate signals. The reference load voltage (VL*) is extracted using the derived unit vector [23]. Load voltages (V_{La},V_{Lb},V_{Lc}) are converted to the rotating reference frame using abc-dqo conversion using Park's transformation with unit vectors (sinθ, cosθ) derived using a PLL (phase locked loop) as,

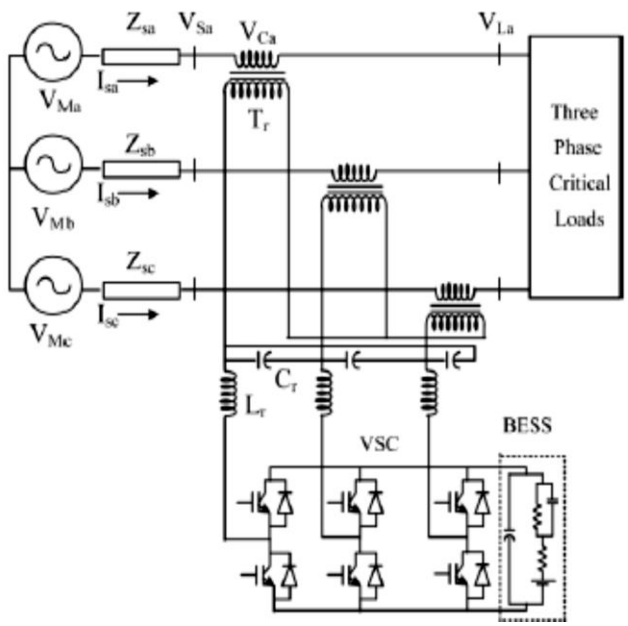

Fig. 2. Schematic diagram of the DVR connected system.

$$\begin{bmatrix} v_{Lq} \\ v_{Ld} \\ v_{L0} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta-\frac{2\pi}{3}\right) & \cos\left(\theta+\frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta-\frac{2\pi}{3}\right) & \sin\left(\theta+\frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} v_{Laref} \\ v_{Lbref} \\ v_{Lcref} \end{bmatrix} \quad (1)$$

Similarly, reference load voltages (V_{La}*,V_{Lb}*,V_{Lc}*) and voltages at PCC (v_S) are also converted to the rotating reference frame. Then, the DVR voltages are obtained in the rotating reference frame as,

$$v_{Dd} = v_{Sd} - v_{Ld}$$

$$v_{Dq} = v_{Sq} - v_{Lq}$$

The reference DVR voltages are obtained in the rotating reference frame as,

$$v_{Dd}^{*} = v_{Sd}^{*} - v_{Ld}$$

$$v_{Dq}^{*} = v_{Sq}^{*} - v_{Lq}$$

The error between the reference and actual DVR voltages in the rotating reference frame are regulated using two PI (Proportional-Integral) controllers. Reference DVR voltages in abc frame are obtained from a reverse Park's transformation taking V_{Dd}* from (4), V_{Dq}* from (5), V_{D0}* as zero as,

$$\begin{bmatrix} v_{dvra}^{*} \\ v_{dvrb}^{*} \\ v_{dvrc}^{*} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos\left(\theta-\frac{2\pi}{3}\right) & \sin\left(\theta-\frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta+\frac{2\pi}{3}\right) & \sin\left(\theta+\frac{2\pi}{3}\right) & 1 \end{bmatrix}\begin{bmatrix} v_{Dq}^{*} \\ v_{Dd}^{*} \\ v_{D0}^{*} \end{bmatrix} \quad (6)$$

Reference DVR voltages (v_{dvra}*, v_{dvrb}*, v_{dvrc}*) and actual DVR voltages (v_{dvra}, vdvrb, v_{dvrc}) are used in a PWM controller to generate gating pulses to a VSC of DVR. The PWM controller is operated with a switching frequency of 10 kHz

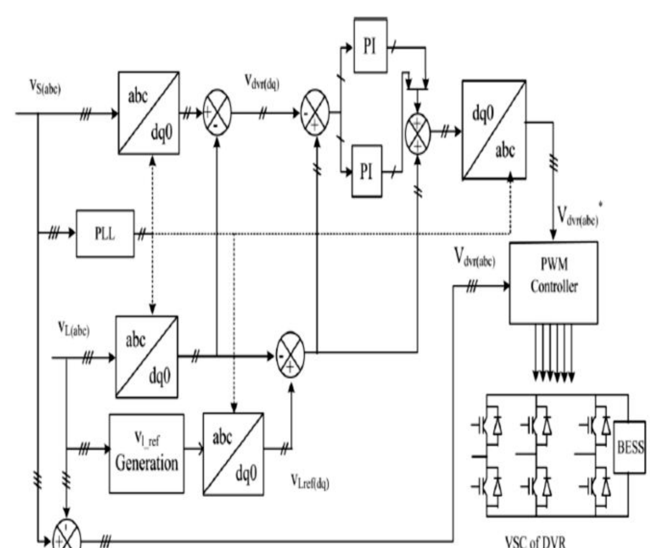

Fig. 3. Control block of the DVR which use the SRF method of control.

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B. Control of Self Supported DVR for Voltage Sag, Swell and Harmonics Compensation

Fig. 4(a) shows a schematic diagram of a capacitor supported DVR connected to three phase critical loads and Fig. 4(b) shows a control block of the DVR in which SRF theory is used for the control of self supported DVR. Voltages at PCC (v_S) are converted to the rotating reference frame using abc-dqo

conversion using the Park's transformation. The harmonics and the oscillatory components of the voltage are eliminated using LPFs (Low Pass Filters). The components of voltages in d-axis and q-axis are,

$$v_d = v_{ddc} + v_{dac} \tag{7}$$

$$v_q = v_{qdc} + v_{qac} \tag{8}$$

The compensating strategy for compensation of voltage quality problems considers that the load terminal voltage should be of rated magnitude and undistorted.

In order to maintain the dc bus voltage of the self-supported capacitor, a PI controller is used at the dc bus voltage of DVR and the output is considered as a voltage (v_{cap}) for meeting its losses.

$$v_{cap(n)} = v_{cap(n-1)} + K_{p1}\left(v_{de(n)} - v_{de(n-1)}\right) + K_{i1} v_{de(n)} \tag{9}$$

where,$v_{dn}(n)=v_{dc}*-v_{dc}(n)$ is the error between the reference ($v_{dc}*$) and sensed dc voltage (v_{dc}) at the nth sampling instant. K_{p1} and K_{i1} are the proportional and the integral gains of the dc bus voltage PI controller.

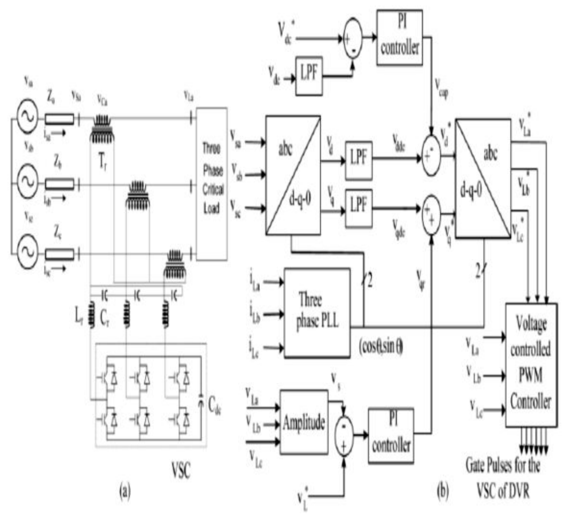

Fig. 4. (a) Schematic diagram of self supported DVR (b) Control block of the DVR which uses the SRF method of control.

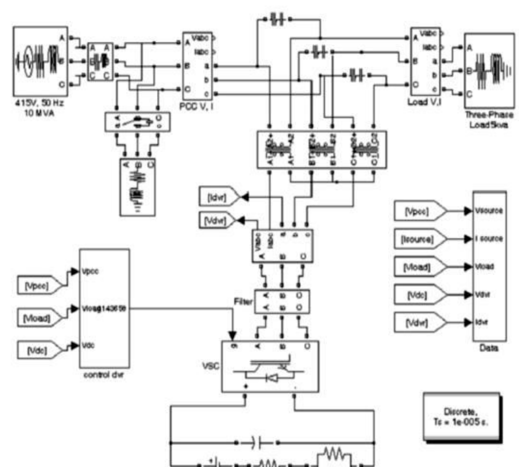

Fig. 5 MATLAB based model of the BESS supported DVR connected system.

The reference d-axis load voltage is, therefore, as,

$$v_d^* = v_{ddc} - v_{cap}$$

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The amplitude of load terminal voltage (V_L) is controlled to its reference voltage (V_L*) using another PI controller. The output of PI controller is considered as the reactive component of voltage (v_{qr}) for voltage regulation of the load terminal voltage. The amplitude of load voltage (VL) at PCC is calculated from the ac voltages (v_{La}, v_{Lb}, v_{Lc}) as,

$$V_L = (2/3)^{1/2}(v_{La}{}^2 + v_{Lb}{}^2 + v_{Lc}{}^2)^{1/2} \quad (11)$$

Then, a PI controller is used to regulate this to a reference value as,

$$v_{qr(n)} = v_{qr(n-1)} + K_{p2}(v_{te(n)} - v_{te(n-1)}) + K_{i2}v_{te(n)} \quad (12)$$

where, $v_{te(n)}=v_L{}^*-v_{L(n)}$ denotes the error between reference (V_L*) and actual ($V_{L(n)}$) load terminal voltage amplitudes at nth sampling instant. K_{p2} and K_{i2} are the proportional and the integral gains of the dc bus voltage PI controller.

The reference load quadrature axis voltage is as,

$$v_q^* = v_{qdc} + v_{qr} \quad (13)$$

Reference load voltages (v_{La}*, v_{Lb*}, v_{Lc}*) in abc frame is obtained from a reverse Park's transformation as in (6). The error between sensed load voltages (v_{La}, v_{Lb}, v_{Lc}) and reference load voltages are used over a controller to generate gating pulses to VSC of DVR.

IV. MODELING AND SIMULATION

The DVR connected system consisting of a three phase supply, three phase critical loads and the series injection transformers shown in Fig.2, is modeled in MATLAB/ Simulink environment along with SPS (Sim-

Power System) toolbox and is shown in Fig. 5. An equivalent load considered is a 10 kVA, 0.8pf lag linear load. Parameters of the considered system for the simulation study are given in Appendix.

The control algorithm for the DVR shown in Fig.3 is also modeled in MATLAB. The reference DVR voltages are derived from sensed PCC voltages (v_{sa}, v_{sb}, v_{sc}.) and load voltages (v_{La},v_{Lb},v_{Lc}). A pulse width modulated (PWM) controller is used over the reference and sensed DVR voltages to generate the gating signals for the IGBTs of the VSC of the DVR.

The capacitor supported DVR shown in Fig. 4 is also modeled and simulated in MATLAB and the performance of the systems are compared in three conditions of DVR.

V. PERFORMANCE OF DVR SYSTEM

The performance of the DVR is demonstrated for different supply voltage disturbances such as voltage sag and swell. Fig. 6 shows the transient performance of the system under voltage sag and voltage swell conditions. At 0.2 s, a sag in supply voltage is created for 5 cycles and at 0.4 s, a swell in the supply voltages is created for 5 cycles. It is observed that the load voltage is regulated to constant amplitude under both sag and swell conditions. PCC voltages (v_S), load voltages

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(v_L), DVR voltages (v_C), amplitude of load voltage (V_L) and

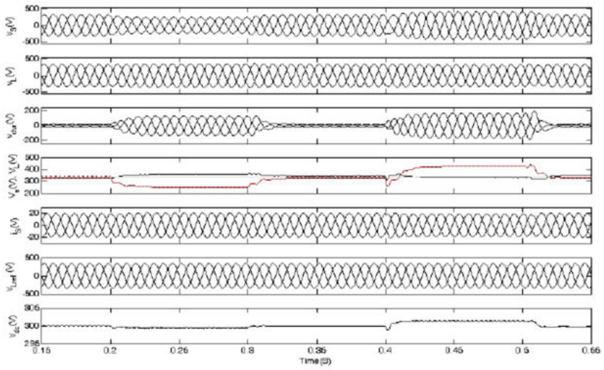

Fig. 6 Dynamic performance of DVR with inphase injection during voltage sag and swell applied to critical load.

PCC voltage (V_s), source currents (i_S), reference load voltages (v_{Lref}) and dc bus voltage (v_{dc}) are also depicted in Fig. 6. The load and PCC voltages of phase A are shown in Fig. 7, which shows the in-phase injection of voltage by the DVR. The compensation of harmonics in the supply voltages is demonstrated in Fig. 8. At 0.2 s, the supply voltage is distorted and continued for 5 cycles. The load voltage is maintained

TABLE-I
COMPARISON OF DVR RATING FOR SAG MITIGATION

	Scheme-1	Scheme-2	Scheme-3	Scheme-4
Phase Voltage (V)	90	100	121	135
Phase Current (A)	13	13	13	13
VA per phase	1170	1300	1573	1755
KVA (% of Load)	37.5%	41.67%	50.42%	56.25%

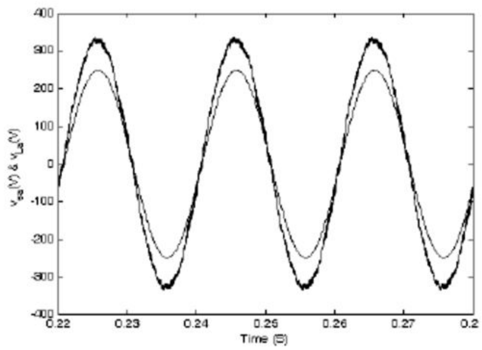

Fig. 7. Voltages at PCC and Load terminals.

sinusoidal by injecting proper compensation voltage by the DVR. The THD (Total Harmonics Distortion) of the voltage at PCC, supply current and load voltage are shown in Figs. 9, 10 and 11 respectively. It is observed that the load voltage THD is reduced to a level of 0.66% from the PCC voltage of 6.34%.

The magnitudes of the voltage injected by the DVR for mitigating the same kinds of sag in the supply with different angle of injection are observed. The injected voltage, series current and kVA ratings of the DVR for the four injection schemes are given in Table-I. In Scheme-1 of Table-1, the in-phase injected voltage is V_{inj1} in the phasor diagram of Fig.1. In Scheme-2, a DVR voltage is injection at a small angle of 30° and in Scheme-3 is the DVR voltage is injected at an angle of 45°. The injection of voltage in quadrature with the line current is in Scheme-4. Required rating of compensation of the same using Scheme-1 is much less than that of Scheme- 4. Performance of self supported DVR (Scheme-4) for compensation of voltage sag is shown in Fig. 12(a) and of a voltage swell is shown in Fig. 12(b). It is observed that the injected voltage is in quadrature with the supply current and hence a capacitor can support the dc bus of DVR. But,

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the injected voltage is higher compared to an in-phase injection (Scheme-1).

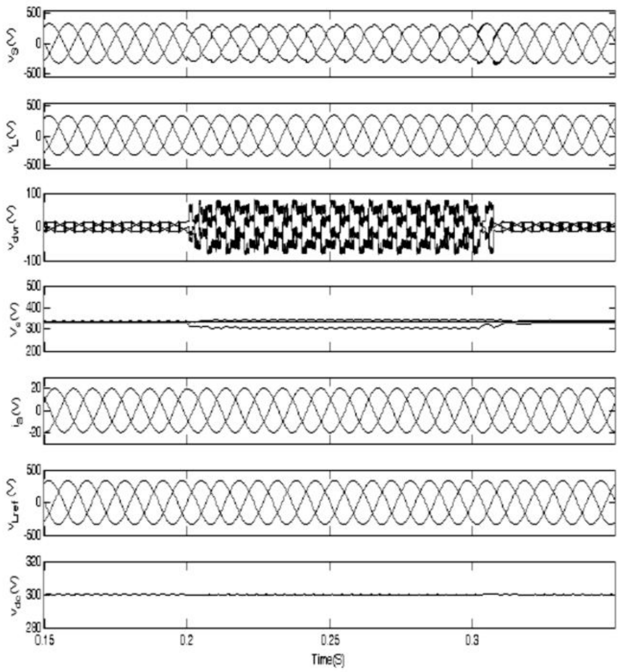

Fig. 8. Dynamic performance of DVR during harmonics in supply voltage applied to critical load.

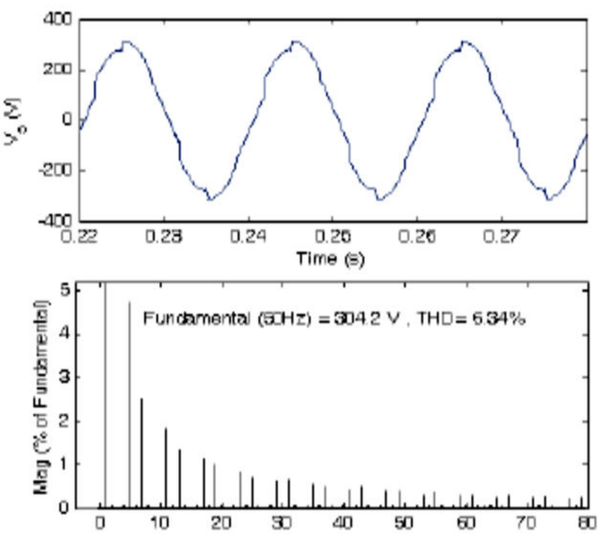

Fig. 9. PCC Voltage and harmonic spectrum during the disturbance.

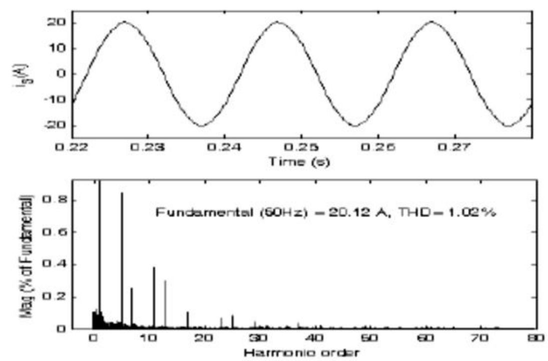

Fig.10. Supply current and harmonic spectrum

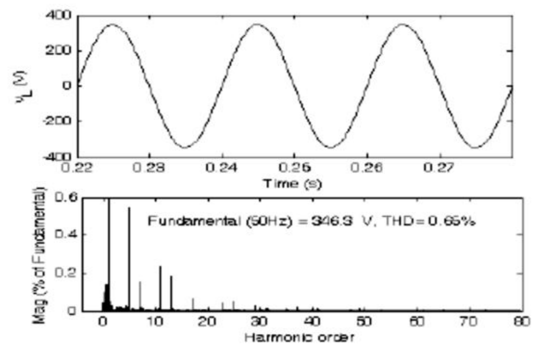

Fig.11. Load voltage and harmonic spectrum during the disturbance.

APPENDIX

AC line voltage: 415 V, 50 Hz
Line Impedance: Ls= 3.0 mH, Rs=0.01 Ω.
Loads: Linear: 10 kVA, 0.80 pf lag
Ripple filter: C_f = 10 μF, R_f = 4.8 Ω.
DVR with BESS:
DC voltage of DVR: 300 V
AC inductor: 2.0 mH
Gains of d-axis PI controller: K_{p1}=0.5, K_{i1}=0.35.
Gains of q-axis PI controller: K_{p2} =0.5, K_{i2} =0.35.
PWM switching frequency: 10 kHz
DVR with DC bus Capacitor supported:
DC voltage of DVR: 300 V

AC inductor: 2.0 mH
DC bus voltage PI controller: K_{p1} =0.5, K_{i1} =0.35
AC load voltage PI controller: K_{p2} =0.1, K_{i2} =0.5
PWM switching frequency: 10 kHz
Series Transformer:
Three-phase transformer of rating 10kVA, 200V/300V

VI. CONCLUSION

The operation of a DVR has been demonstrated with a new control technique using various voltage injection schemes. A comparison of the performance of DVR with different schemes has been performed with reduced rating VSC including capacitor supported DVR. The reference load voltage has been estimated using the method of unit vectors and the control of DVR has been achieved which minimizes the error of voltage injection. The SRF (Synchronous Reference Frame) theory has been used for estimating the reference DVR voltages. It is concluded that the voltage injection in-phase with the PCC voltage results in minimum rating of DVR but at the cost of an energy source at its dc bus.

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