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DESIGN HIGH SPEED IMPLEMENTATION OF VLSI ARCHITECTURE FOR CONSTANT RETIMING MULTIPLER

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ABSTRACT:

This paper constitutes a new low power multiplication algorithm and VLSI architecture. In proposed algorithm we can find NXN unsigned binary number multiplication by using 2^n -1 constant for both multiplicand and multiplier. It exhibits the utilization of the hardware resource results that are low power consumption and better power delay product which are compared to the conventional multiplier. The performance of the 32 bit multiplication provides a savings of 46.34% in power delay product over the existing conventional multiplier. To design the fast multiplication, the optimization technique like retiming approach is adopted. The retiming analysis results are compared with the conventional multiplier and constant multiplier.

I.INTRODUCTION

Rapid multiplication creates the essential need for more sophisticated digital VLSI signal processing application which is being implemented on a soc. A multiplier block is required for the expansion of modern smart phones, wearable small devices, electronic devices and digital signal processor. Multiplier is more frequently used computational blocks in VLSI digital signal processing in battery operated power devices. There are various ways for developing the multiplier. On the performance front, there is a need for optimized constant multiplier architecture which is established to design fast and low power chips. As the word size increases the complexity of the multiplication logic also increases and it is very difficult to implement using hardware devices. The proposed constant multiplier algorithm is examined the minimum number of steps for higher order word size. The proposed pseudo code is implemented as a basement of vedic sutra and reconfigurable constant multiplier for improving the higher order multiplier.

Data flow graph is used for organizing the diagrammatical sketch of the algorithm. It changes the structure of the graph without changing its output performance. A directed graph which is shown in fig 1 denotes a linear transforms from the signal at node j to the signal at node k.

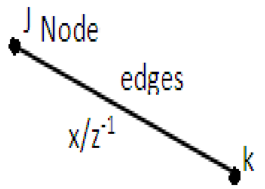

FIG 1. DIRECTED GRAPH

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A Data flow graph for constant multiplier is G = (V,E) where V is the input or output to the multiplier block and e denotes the wire or gate delay of the multiplier.

Fig 2. Shows the multiplication result for the constant multiplier. DFG indicates the concept of one less than LHS digit and the answer which is minus by one are RHS digits. The multiplication result is LHS and RHS. Efficient realization of timing concept is proposed by Leiserson and Saxe. In a synchronous sequential circuit the flip-flop can be reordered by introducing well-known retiming optimization method. The minimum delay retiming and minimum register retiming is achieved for polynomial time algorithm.

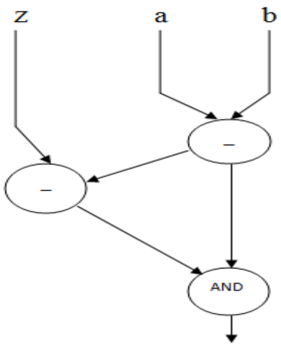

FIG 2. DATA FLOW GRAPH FOR CONSTANT MULTIPLIER

As a result for synchronous sequential circuit the switching activity is more at the flip-flops inputs than the flip-flop outputs. These computations occur due to many unwanted transitions at the flip-flop inputs to the outputs. Low power consumption is achieved by applying retiming. One of the researchers implemented the timing approach for linear feedback shift registers (LFSR) circuit. The experimental result shows high speed for proposed parallel filter design. The hardware complexity and power consumption has been reduced by combining parallelism, pipelining and retiming. The proposed 4-bit multiplier block is used to build the 16-bit multiplier to realize the hardware reusability. Retiming, folding and unfolding techniques are used for modified multiplier architecture which has less area consumption than Wallance multiplier and 4-bit modular multipliers. The survey on retiming concept tells that the squaring algorithm improves the speed compared with the existing algorithm.

II. ARCHITECTURE OF CONSTANT MULTIPLIER

In latest VLSI technology more gates are arranged in a single chip. For implementing multiple architecture we can adopt a “Ekanyunena Purvena” vedic sutra. The architecture of constant multiplier is shown in fig 3. To achieve lesser power consumption the constant multiplier (CM) block can be reused up to low order word size. The proposed hardware architecture is composed by multiplier, comparator, subtractor and Half subtractor. The existing architecture has a deficiency in terms of timing when multiplier size has been increased but this is improved in the proposed architecture.

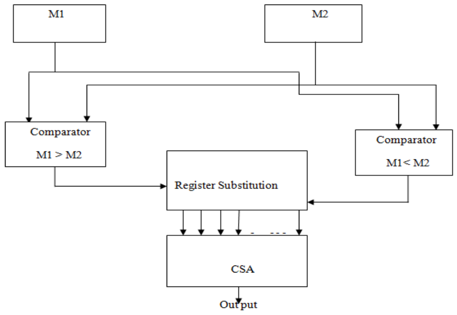

FIG 3. Architecture of constant multiplier

In architecture of constant multiplier the comparator is used to determine the greater than/equal or less than of the 2 unsigned binary numbers. Then subtraction of greater/equal number is subtracted from the constant number.

To generate CM output again subtractor (SUB) block can be used to decrement the smaller number and subtract this decremented value from the constant number. Then decremented output is MSB bits and the subtracted output is the LSB bits. Finally, the output is the combination of both subtracted output and decremented output. By Urdhva Tiryakbhyam sutra the remaining subtracted low order word size number is multiplied. Then, to get final multiplication the CM results and multiplier output is again subtracted. The proposed architecture can be constructed by using basic data path elements.

The multiplier block is utilized for handling the corner cases. Any of the primary input is low then the output generated by the multiplier is directly zero. Based on constant multiplier algorithm if the select line is logic high then the multiplier output is generated. The output of the multiplier is stored in the memory element. The proposed design is modeled by using Verilog HDL and power delay analysis is done by the RTL compiler.

III. RESULTS AND DISCUSSION

1.Functional verification of the design: The simulation of the test-case verification of constant multiplier is done by using XILINX Tools. To complete the verification of the design timing simulation for a set of stimuli input values are injected, to verify the output proved.

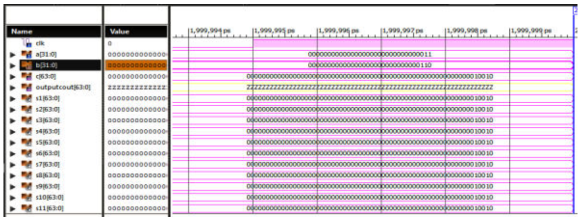

FIG 4. Functional verification of 32-bit multiplier result

2. Synthesis Results: Secondly gate level synthesis of the design is done by the RTL compiler.

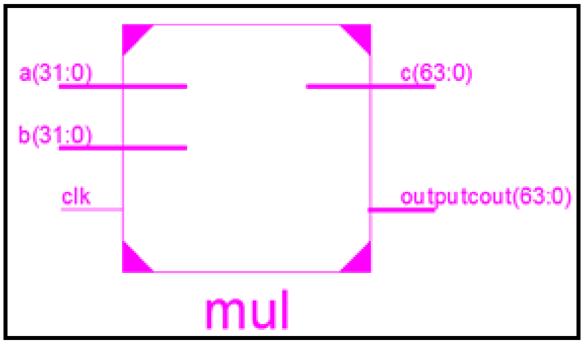

FIG 5. RTL Synthesis

IV.CONCLUSION

The proposed work deals with reusability of the hardware resources using constant number. We presented a constant multiplier algorithm which is beneficial in power if the sub modules can be made reusable for higher order bits. We provide the retiming techniques for analyzing the speed requirement in large bit multiplication processes. Constant Multiplier is not only simpler than Conventional Multiplier but also yield less power consumption. Compared to the general multiplier the optimal speed is obtained by using retiming technique. An experiment previses the proposed method successfully by achieving the improvement in both power and clock when compared to conventional methods. Therefore the proposed multiplier requires the least power than the conventional algorithm.

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