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A THREE-PHASE MULTILEVEL HYBRID SWITCHED-CAPACITOR PWM PFC RECTIFIER FOR HIGH-VOLTAGE-GAIN APPLICATIONS

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ABSTRACT

This paper presents a three-phase multilevel power factor correction rectifier using the hybrid switched-capacitor concept is proposed. The converter is suitable for high-voltage-gain applications from conventional three-phase low-voltage sources. The three-level voltage operation reduces the weight and bulk of the magnetic devices. The main advantages of the proposed converter are low number of active switches, high voltage gain, sinusoidal currents, low voltage stress across all components, and simple control. Both steady-state and dynamic analyses are investigated.

I. INRODUCTION

For low-power levels, single-phase voltage multiplier circuits are often employed due to robustness and simple operation. With the increase of the power load, the use of three-phase converters becomes necessary. However, mechanisms should be provided to reduce the voltage stress across the components and increase the ac current quality. In a three-phase symmetrical multistage voltage multiplier has been presented. This converter merges three voltage multiplier cells connected to isolated three-phase voltage source to achieve high gain conversion. It has the advantage that all semiconductors are subjected to low voltage, which allows the operation with high dc-link voltage. As a drawback, the capacitors operate at the grid frequency, leading to an increase of the bulk and weight of the conversion system. Moreover, the ac currents have high harmonic distortion due to absence of active control. Because of related problems, in a three-phase step-up multiplier with a switching device is proposed. It comprises a three-phase diode bridge connected to a boost converter and a voltage multiplier cell. The voltage gain can be increased by just adding diode–capacitor cells. The active switch is subjected to low voltage and the capacitors operating at high frequency.

In contrast, the ac currents do not have the shape of the input voltages; thus, the unitary power factor is not possible. In order to increase the ac current quality, three-level pulse width modulation (PWM) rectifiers have become an interesting alternative to three-phase applications . They feature high performance for power factor correction (PFC) operation, high efficiency, and high power density. On the other hand, these converters are suitable for low dc-link voltage (lower than 1000 V). To higher dc-link voltages, converters with four and five levels are more attractive. However, the number of active switches and voltage sensors is increased substantially, raising the cost and complexity of the system. Recently, The ac output voltage of the matrix converter is connected to a single voltage multiplier, from which a high voltage gain is achieved. Furthermore, the currents have sinusoidal shape, resulting in a power factor nearly unity. A drawback of this concept is the high number of active switches required for power conversion. Due to troubles related to listed

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topologies, a three-phase multilevel PFC rectifier for high-voltage-gain applications is proposed in this paper. This new topology integrates a three level boost PFC converter with a diode–capacitor cell, resulting in a hybrid concept1 with high-voltage-gain conversion and PFC operation, simultaneously.

II. OPERATION PRINCIPLE OF THE PROPOSED CONVERTER

A) Features of the Proposed Converter

The proposed converter is shown in Fig. The topology comprises six active switches,2 18 fast diodes, six slow diodes, and 12 capacitors. It presents the PFC operation and has gain twice of to one-fourth of the output voltage *Vo* having, therefore, considerable reduction of the switching losses, enabling the use of low-voltage devices.

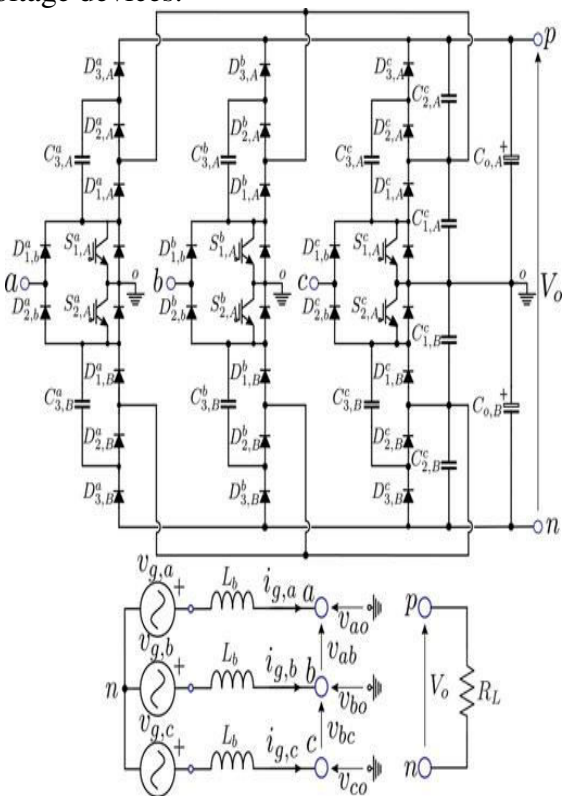

Fig. 1. Proposed high-gain three-phase multilevel hybrid switched-capacitor PWM PFC rectifier.

The voltage across the capacitors *Ck i,j* , $i \in \{1, 2, 3\}$, $j \in \{A,B\}$, $k \in \{a, b, c\}$, has the self-regulation ensured by the PWM modulator, and therefore, the use of the voltage sensors is not necessary for these capacitors. For the output voltage regulation, two voltage sensors are necessary. At switching terminals *a, b,* and *c*, three-level voltages can be generated leading to reduction of bulk of the magnetics devices, increasing the current quality and power density. The capacitors *Co,j* are connected to load and they must meet hold-up time requirements.

B) Principle of Operation and Switching States

Through of the sign of the currents and state of the switches, the topological stages can be determined. In total, there are 25 possible states. In this paper, only six topological stages will be described. In Fig. 2, the switching states valid to $ig,a > 0$, $ig,b < 0$, $ig,c < 0$, and $ig,c > ig,b$ are depicted. For simplicity, the input ac voltage sources *vg,k* , $k \in \{a, b, c\}$, inductors *Lb* , and load resistance *RL* are omitted in the figure. In the following, the basic principle of operation of the threephase hybrid PFC rectifier is explained based on some simplifying assumptions: 1) the converter operates in the steady state; 2) the voltage across the capacitors *Ck i,j* , *vk Ci,j* , is ripple-free and approximately equal to *Vo*4 ; 3) the voltage *vkC*1,*j* is simultaneously slightly higher than *vkC*3,*j* and slightly lower than *vkC* 2,*j* ; 4) all components are ideal; The other switching stages have similar operation and, therefore, will not be explored herein. The topological stages shown in Fig. 2 are listed in Table I. The remaining voltage vectors, related to switching states, are not listed in the table, but they can be found by easily knowing the sign of the input currents and the state of the switches. It can be noted in all operation stages that the maximum voltage stress on the each device is *Vo*/4. As previously

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mentioned, this feature enables the use of semiconductors with lower voltage ratings.

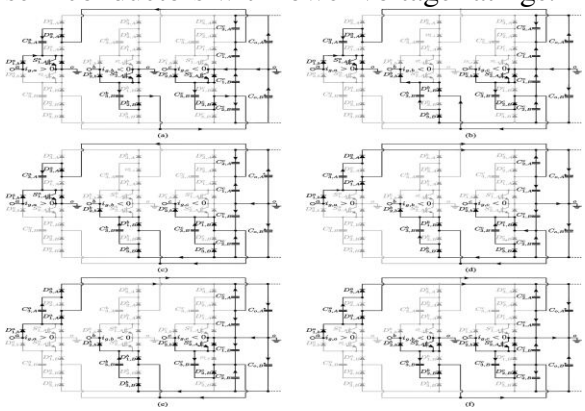

Fig. 2. Topological stages of the proposed three-phase converter valid to $ig,a > 0$, $ig,b < 0$, $ig,c < 0$, and $ig,c > ig,b$: (a) state V0 = (0, 0, 0); (b) state V1 = (0,−1, 0); (c) state V2 = (0,−1,−1); (d) state V3 = (1,−1,−1); (e) state V4 = (1,−1, 0); (f) state V5 = (1, 0, 0).

III. CONTROL STRATEGY

In principle, any control strategy used in conventional unidirectional three-level PWM rectifiers may be extended for the proposed converter. Due to simplicity and acceptance in the literature, the synchronous reference frame control strategy is employed in this paper. The control scheme and the block diagram are shown in Figs, respectively.

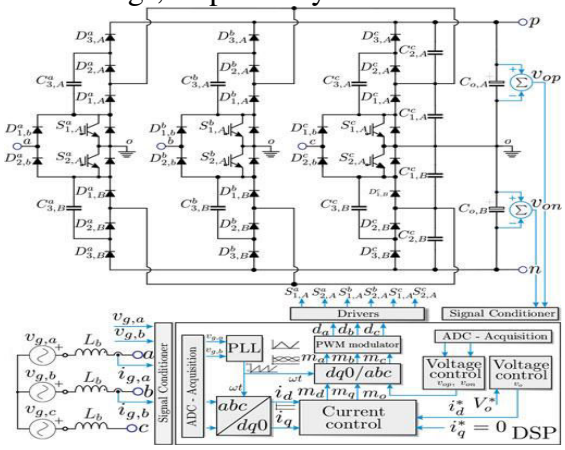

Fig 3. Synchronous reference frame control strategy applied to the proposed converter.

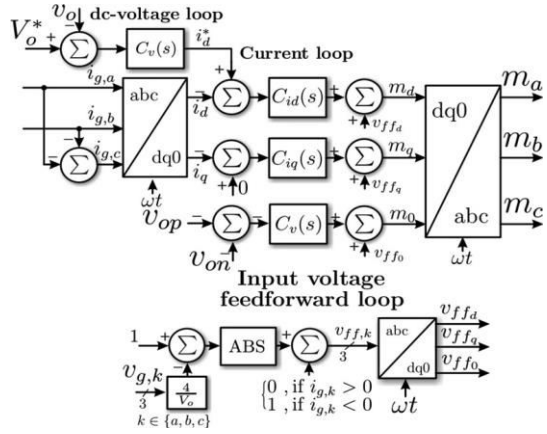

Fig4. Control block diagram of the proposed converter.

and, where input currents and input/output voltages are measured to guarantee PFC operation and partial output voltage regulation. Because there is no connection between the midpoint *o* and the neutral point *n*, only two currents are necessary to perform the control. The input currents *ig,a* and *ig,b* are converted to *id* and *iq* components through the transformation block *abc/dq*0. The angle *ωt* is synchronized with the positive sequence of the grid voltages, and it is extracted from the PLL block. The grid voltages *vg,a* and *vg,b* are also used to feed forward loop of the duty cycles. The current error of the *d*- and *q*-axes is fed to their respective regulators *Cj* (*s*), *j* ∈ {*d*, *q*}, where the output signals, added to feed forward signals *vf fj* , generate the modulation signals *md* and *mq* [cf., Fig. 8]. In order to establish the instantaneous output voltage *vo* regulation, the partial output voltages *vop* and *von* are measured. The dc-voltage loop generates the direct axis current reference *i**d* by means of the difference between *vo* and voltage reference *V* **o* . The voltage error is fed to the proportional integral regulator *Cv* (*s*), where its output corresponds to *i**d* . For the unity power factor, the quadrature axis current reference should be set to 0. To ensure that the voltages *vop* and *von* have the same average value, an additional dc-voltage balance control loop is

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required. As a result, a zero-axis modulating signal $m0$ is generated. In Section IV-D, the zero-sequence component will be detailed where a transfer function will be derived.

IV.SIMULATION RESULTS

A) SIMULATION MODEL OF EXSTING SYSTEM

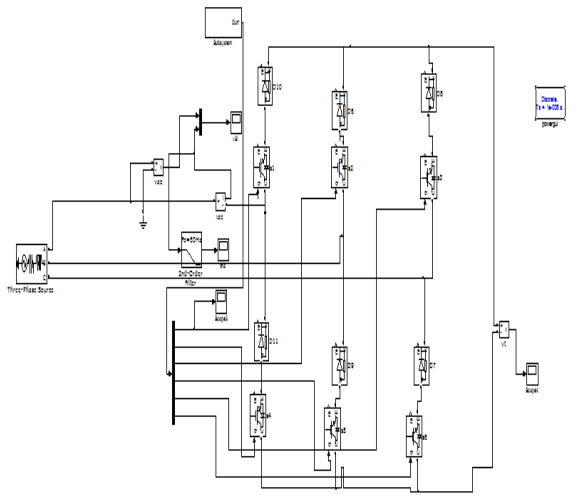

Fig 5MATLAB/SIMULATION diagram of existing model

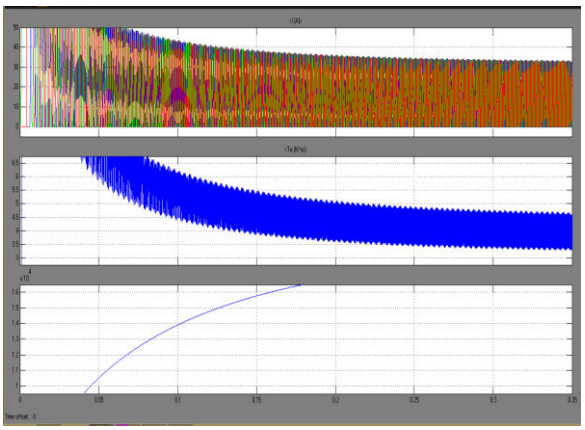

Fig.6 simulation output waveforms of existing system

B) SIMULATION MODEL OF EXTENSION SYSTEM

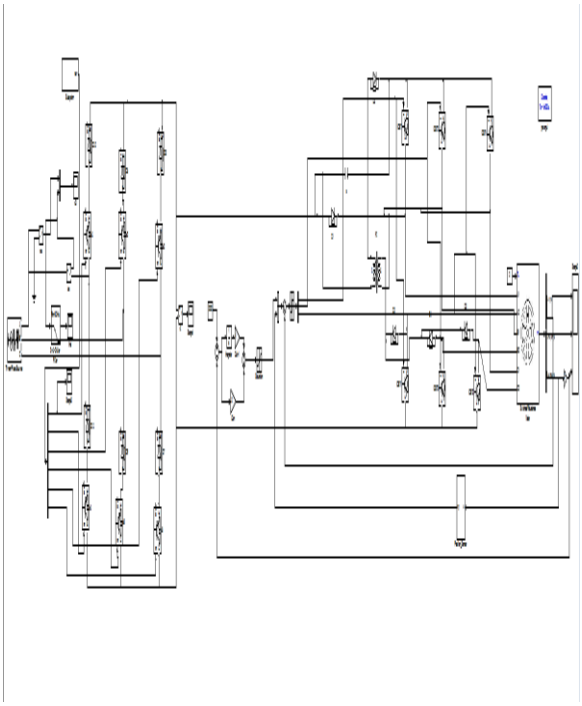

Fig 7 SIMULATION MODEL OF EXTENSION SYSTEM

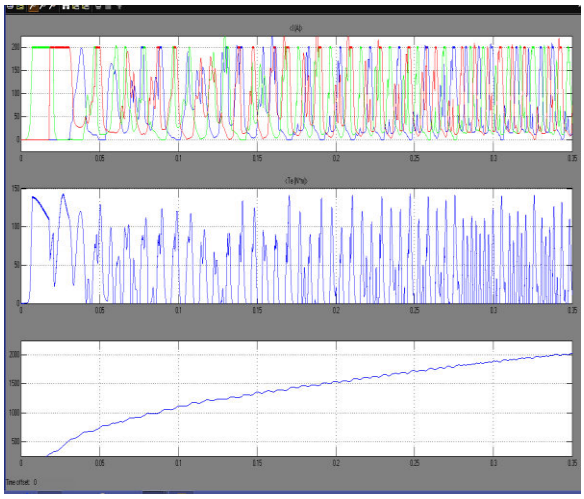

Fig.8 Simulation Output Waveforms Of Extension System

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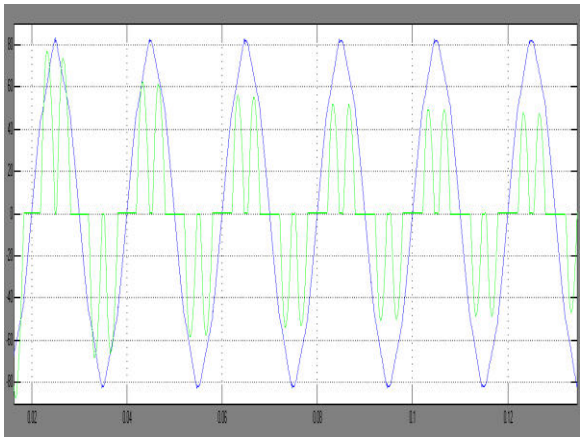

Fig.8. SIMULATION MODEL OF INPUT CURRENT OF SRM DRIVE IN EXISTING SYSTEM

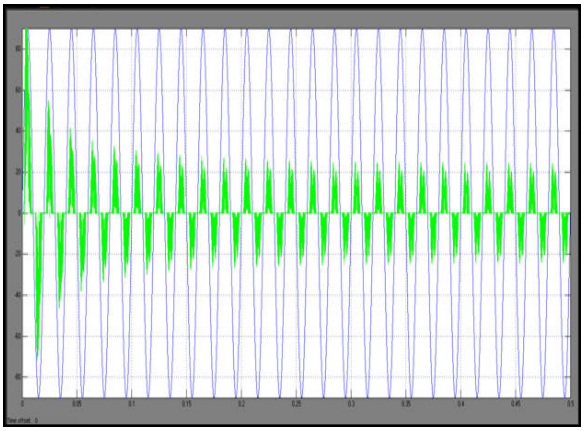

Fig.9 SIMULATION MODEL OF INPUT CURRENT OF SRM DRIVE IN EXTENSION SYSTEM

CONCLUSION

A three-phase hybrid switched-capacitor multilevel PFC PWM rectifier aiming high-voltage-gain applications has been presented in this paper. This topology use, at the same time, the inductive storage and the switched-capacitor concept to achieve a high voltage conversion and PFC operation, simultaneously. The three-level operation enables the bulk/weight reduction of the magnetic components. The main feature are low number of active switches and the fact of all components are subjected to one-fourth of output voltage, allowing the use of reduced ratings power semiconductor devices. A suitable control scheme has been presented, where it can be seen that synchronous reference frame strategy, used in conventional three-level converters, can also be employed in the proposed converter. Transfer functions for the design of the current regulators and voltage regulators were presented. In summary, the current topologies, presented in the introduction, have interesting features for high-voltage-gain applications, but do not have at same time high voltage gain, robustness, low number of active switches and sinusoidal-shape currents. Because of this, the proposed concept presented may be an attractive alternative to high voltage gain in three-phase rectification, with low impact to the grid.

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