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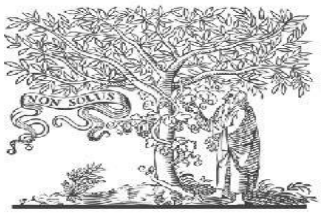

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Paper Authors
BATTU SAILU BHANU, R.S.V.S ARAVIND

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HIGH-SPEED AND AREA EFFICIENT VLSI ARCHITECTURE OF MULTIPLIER USING MODIFIED BRENT KUNG ADDER

[1]BATTU SAILU BHANU, [2]R.S.V.S ARAVIND

[1]M.Tech scholar, Dept of ECE, Eluru College of Engineering & Technology, Andhra Pradesh, India
[2]Assistant Professor, Dept of ECE, Eluru College of Engineering & Technology, Andhra Pradesh, India

ABSTRACT: In this paper, a high-speed and area efficient VLSI architecture of multiplier using modified Brent kung adder is implemented. Basically, multipliers are key arithmetic circuits in many of these applications including digital signal processing (DSP). This multiplier architecture using modified Brent kung adder limits its carry propagation. Partial products are used to generate propagate and generate signal's. Pipeline register is used for sequential logic to increase the speed of operation. Hence this paper reduces the delay and increases the speed in effective way.

Key Words: **VLSI, Digital signal processing (DSP), Partial products, Brent Kung Adder, Multiplier.**

I.INTRODUCTION

Basically, in communication systems like error correction codes and cryptography, finite field is most widely used. Arithmetic operations are performed using the field elements. Two basis are normally used to implement a system that is normal basis and polynomial basis. Normal basis is used to implement the hardware and perform the low cost squaring operations. In the same way, polynomial basis is used to implement the software and in the same way this also performs the low cost squaring operations [1].

Accuracy could be compromised to a defined extent in most of the present-day applications like image recognition and processing. Multiplier is the basic building block of such applications which involve a lot of mathematical processing. This leads to a win-win balancing between the energy consumed by the circuit and the required accuracy.

The energy consumed by any system is directly proportional to the multiplication accuracy of those systems. If a system requires high accuracy then it consumes more energy and vice versa. Also, there could be section or module of that systems which needs lesser accuracy than other parts of the system. If the accuracy is kept constant across all such modules it greatly increases the amount of energy consumed by the overall system. However, if the accuracy of the multiplier is characterized to change as per the need of that particular module or section of the entire system, this would have a great impact in reducing the amount of energy consumed by the system [2].

This method of configuring and adjusting the accuracy of a multiplier based on the requirement of the system or application is achieved using different adder sub module of the multiplier module to characterize the accuracy based on the approximation technique. There should be reconfigurable multipliers in various program stages or applications [3]. So, in this paper we designed a multiplier which has an accuracy decided on the go based on the requirement of the application.

Montgomery's multiplier is classified into three types, they are bit-serial, bit-parallel, and digit serial architectures. Bit-parallel shape is rapid; however it's far steeply-

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priced in phrases of vicinity. Bit-serial structure is region efficient, but it's far too sluggish for plenty packages. The digit-serial structure is flexible which may change the space and velocity, consequently, it achieves a moderate pace, reasonable price of implementation and hence it is most appropriate for practical use. Montgomery presented a technique for figuring modular multiplication productively. He introduced to move the portrayal of numbers from the Zn to an alternate area, called Montgomery Residual portrayal or Montgomery Domain [2-3].

Here for the purpose of security, the computers and communication system brought with a demand from private sector [4]. The Montgomery multiplication is the calculation that permits effectively for registering. The expense of the particular duplication is equivalent to three whole numbers which increases in addition to the expense of the change in the Montgomery area. Yet, in the event that the large scale task is an exponentiation, at point the change cost is insignificant contrasted with the quantity of augmentations executed in the Montgomery area. In the process of Montgomery multiplication, pre-processing unit and post-processing units are used [5]. The pre-processing unit produces N-Residue operands and in the same way post processing unit will eliminate the constant factor 2n. Hence to form N-Residue operands in the system, modular exponentiation is used.

Here for the purpose of supplanting division activities, shifting tasks are used. After the shifting process the least critical bits will remain zero. Now to eliminate these bits in the modular multiplication, add products are used. After the process of eliminating the bits, the remaining bits are augmented in the multiplicand. Hence from this it can observe that the process of multiplicand is completed. Now the output is obtained after the subtraction of bits. Here if the bits are increased then Montgomery bits also increases. At last the multiplicand bits are controlled without the use of subtraction calculation.

II. BRENT KUNG ADDER BASED FAST MULTIPLIER

The below figure (1) shows the Brent kung adder using fast multiplier. The Brent kung adder computes the prefix for the 2-bit cluster. Their prefixes area unit used to find the prefixes for the 4-bit teams, that in term area unit used to compute the prefixes for 8-bit groups and then on. These prefixes are then used to compute the performance of the actual bit stage. These carriers are used together with the cluster propagate of the following stage to compute the total bit of that stage.

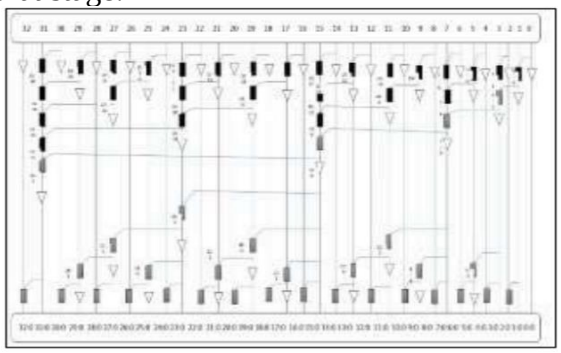

Fig. 1: BRENT KUNG ADDER USING FAST MULTIPLIER

It is evident from the above figure that the interpolated pixel intensity is calculated using four of its neighboring pixels. These neighboring pixels are displayed in the figure using four black dots at the corner of the square. The length of the arms of the square in Fig. 1 is taken as '1'. Likewise, the horizontal and vertical distances between the interpolated pixel and the co-ordinates of the

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neighboring pixels are calculated.

Brent kung adder will be used in this stage. Since we are coming up with a 32-bit adder, the number of stages is nine. The fan out for every bit stage is limited to two. The diagram below shows the fan out being decreased and also the further stages being reduced, but whereas actually implemented, the buffers are generally omitted.

As stated before, the shifters are realized by bus cross-connection. Naturally, the shifters offer no propagation delay. The delay of the single logic gate can also be neglected.

III. MULTIPLIER ARCHITECTURE USING MODIFIED BRENT KUNG ADDER

The below figure (2) shows the multiplier architecture using modified Brent kung adder. The entire system is divided into following modules. The following modules are register X, register Y, partial product unit, pipeline register, partial generation unit, black cells and grey cells. This operation is mainly used in the coprocessor in parallel format. This system provides the functionality for coprocessor. First the alignment of partial products generator will be done. After that partial products takes this registers and generates the propagate and generate signals. After this multiplication operation is performed based on look up table. Now these bits perform the addition operation and give the final product.

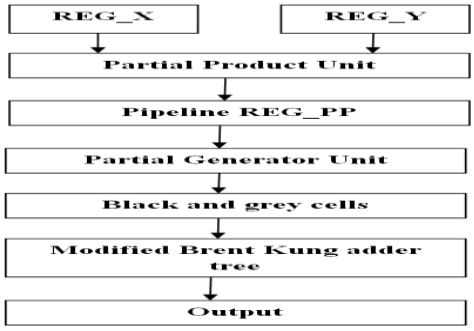

Fig. 2: MULTIPLIER ARCHITECTURE USING MODIFIED BRENT KUNG ADDER

Here firstly, the operands are loaded in the multiplier. The arithmetic operations like addition and multiplication operations are performed. The obtained result of this will be saved in the barrel shifter. Here irreducible polynomial function is not used in the system. The main intent of register multiplier is to store the bit representation and give polynomial output a(t). Here parallel load operation is performed in the most significant bit position. In the same way left shift operations are performed in MSB bit.

The X select enable is used b(t) value to store the value in register. The parallel load operation is also applied in the multiplicand. The obtained value is stored in the register. The right shift operation is performed in the multiplicand register block. crypto core processor is used to transfer the data in multiplicand register.

The result x select enable and y select enable is processed to the partial product generator block. The both A select enable and B select enable values are assigned in the barrel shifter blocks. The obtained values in the propagator and generator block will generate the signals. This block will perform the addition operation.

An adder is a digital circuit that performs addition of numbers. A multiplexer or mux is a combinational circuits that selects several analog or digital input signals and forwards the selected input into a single output line.

Final value is the combination of output. Where all bits gets mixed to get the final output. Hence from results it can observe that the proposed system, will reduce the delay and memory usage in very effective way.

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PG logic is an example of a prefix computation. This prefix computation forms an integral part of the parallel prefix tree. The key of building any prefix tree is to implement the structure according to the grey cell and black cell logic.

IV. RESULTS

The below figure (3) shows the RTL schematic of proposed system. here a and b are the inputs and cout is the output.

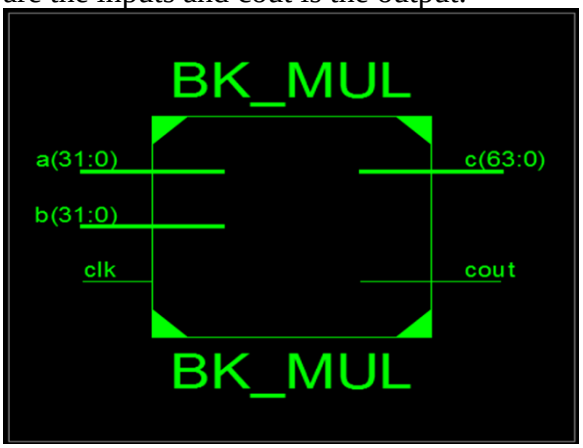

Fig. 3: RTL SCHEMATIC OF PROPOSED SYSTEM

The below figure (4) Technology schematic of proposed system. RTL schematic is the combination of Look up tables, truth tables, K-MAP and equation.

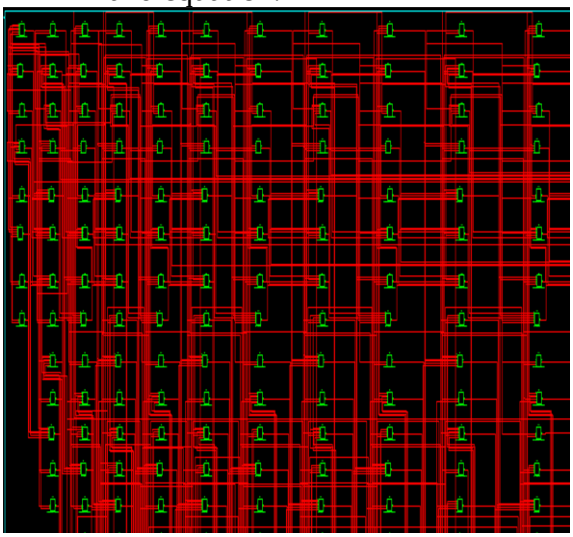

Fig. 4: TECHNOLOGY SCHEMATIC OF PROPOSED SYSTEM

Fig. 5: OUTPUT WAVEFORM OF PROPOSED SYSTEM

V. CONCLUSION

Hence in this paper, a high-speed and area efficient VLSI architecture of multiplier using modified Brent kung adder is implemented. Basically, multipliers are key arithmetic circuits in many of these applications including digital signal processing (DSP). Hence this paper reduces the delay and increases the speed in effective way.

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