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Volume 06, Issue 05, Page No: 2023 – 2029.

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A MULTILEVEL ACTIVE BUCK PFC RECTIFIER FOR BATTERY AND DC MOTOR APPLICATIONS

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ABSTRACT

The main aim the project is multilevel active buck PFC rectifier for battery and dc motor applications. This project presents a new family of buck type PFC (power factor corrector) rectifiers performance in CCM (continuous conduction mode) and generates multilevel voltage waveform at the input. Due to CCM operation, commonly used AC side capacitive filter and DC side inductive filter are removed from the proposed modified packed U-cell rectifier structure. Dual DC output terminals are provided to have a 5-level voltage waveform at the input points of the rectifier where it is supplied by a grid via a line inductor. Producing different voltage levels reduces the voltage harmonics which affects the grid current harmonic contents directly. Low switching frequency of the proposed rectifier is a distinguished characteristic among other buck type rectifiers that reduces switching losses and any high switching frequency related issues, significantly. In extension we observed simulation results of active buck pfc rectifier for battery and dc motor applications.

KEY WORDS: Continuous conduction mode, PFC, Filter, Rectifier

I. INTRODUCTION

PFC buck rectifiers are mainly known with their discontinuous conduction mode (DCM) which complicates formulating the output voltage. On the other hand, DCM operation makes the output DC voltage control depending on the load impedance and also makes it inevitable to use large inductive filters at DC side. Moreover, high switching frequency e.g. 65 kHz and more is a normal operating point in reported topologies that increases switching losses significantly. Large-size LC filters at the output as well as non-removable AC side filters are inherent disadvantages of PFC buck rectifiers. Detailed problems associated with such rectifiers are investigated in the literature. Another configuration to generate a reduced DC voltage is combination of diode-bridge and dc-dc buck converter in which the AC voltage is rectified by that diode-bridge and then DC voltage is stepped down at a desired level by the chopper. Such two stage structures present more power losses, low efficiency and high manufacturing costs in medium and high power applications due to using many semiconductors and reactive components. Regarding above-mentioned facts, PFC buck rectifiers are not so

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much welcome in industrial applications compared to boost type of those PFC rectifiers. Such boost types do not require bulky filters at AC or DC sides since ensuring harmonic suppression of input current, unity power factor operation of the system and constant DC voltage at the output terminal. To have a reduced DC voltage at the output, bridgeless PFC boost rectifiers are usually connected to the main grid after a step-down transformer. Therefore, to have a 125 V DC at the output terminal of a PFC boost rectifier from a 120V RMS grid, a transformer should be used to reduce the grid peak voltage to less than 125 V that has its own disadvantages.

In this paper, a new family of bidirectional bridgeless buck PFC rectifiers is introduced which is an efficient cure to all above mentioned issues. The proposed HPUC (Hani Packed U-Cell) rectifier operates in boost mode while splitting the output voltage terminals to have multiple-output with reduced voltage levels as buck mode. Supplying multiple-output terminals result in producing a multilevel voltage waveform at the rectifier input that reduces the harmonic content of the rectifier voltage and consequently the grid current harmonic without using large inductive filters at the AC side. Boost mode operation of the overall system helps removing bulky filters from both sides specially the DC side inductor. Moreover, CCM operation is guaranteed in a whole period.

II. OPERATION PRINCIPLE OF PFC BUCK RECTIFIER

The proposed rectifier topology has been shown in figure. It has 6 active switches and two output DC terminals. The output terminals are providing voltages V1 and V2 to loads that should be identical as E to have a five-level voltage waveform at the rectifier input. Rectifier input voltage is measured at points ‘a’ and ‘d’ as Vad. The switching states associated to the introduced rectifier have been listed in table I. The proposed HPUC rectifier is a modification to the well known PUC converter in which the lower U-cell components are connected in reverse direction. The PUC converter was proposed as an inverter to generate 7-level voltage waveform while using a single isolated DC source and a controlled capacitor. Moreover, it has been tested as a 7-level rectifier supplying a DC load in boost mode of operation. Another similar structure with cascaded cells was proposed in but as an inverter application with no control that only requires too many isolated DC sources. The idea of the HPUC is to introduce a rectifier by utilizing the similar structure of PUC with slight modification working in buck mode to supply DC loads with lower voltages than the grid where no transformer and additional filter would be required. It is clear from table I that each pair of switches S1-S4, S2-S5 and S3-S6 is working in complementary manner. All switching states and associated conducting paths are shown in figure. which will be used in voltage regulator design section. By controlling output DC voltages, Vad would have five levels including ±2E, ±E, 0 that the maximum value is +2E.The principal concept of proposing this topology as a buck rectifier relies on this maximum value of Vad which should be more than the AC source peak value (*vs max*). The following relations can be written, accordingly.

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$$V_{ad} \geq v_s \rightarrow 2E \geq v_{s\ max} \rightarrow E \geq \frac{v_{s\ max}}{2}$$

For instance, if RMS voltage of the AC source is 120V, then the maximum value would be 170V and the following relations would be obtained. To maintain the stable operation of the converter in buck mode, the maximum generating DC voltage is set at *vs max* which would be 170 V here.

$$\frac{v_{s\ max}}{2} \leq E \leq v_{s\ max} \rightarrow 85V \leq E \leq 170V$$

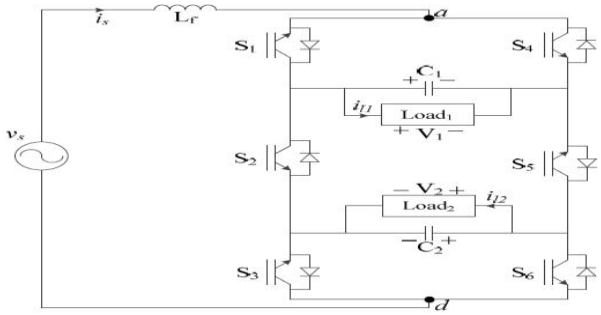

Fig1. Proposed HPUC five-level buck PFC rectifier

TABLE I
SWITCHING STATES OF THE PROPOSED HPUC FIVE-LEVEL BUCK PFC RECTIFIER

Switching State	S_1	S_2	S_3	S_4	S_5	S_6	V_{ad}	V_{ad} voltage levels
1	1	0	1	0	1	0	V_1+V_2	+2E
2	1	0	0	0	1	1	V_1	+E
3	0	0	1	1	1	0	V_2	+E
4	1	1	1	0	0	0	0	0
5	0	0	0	1	1	1	0	0
6	1	1	0	0	0	1	$-V_2$	-E
7	0	1	1	1	0	0	$-V_1$	-E
8	0	1	0	1	0	1	$-V_1-V_2$	-2E

As mentioned above, this rectifier is a boost converter in grid point of view due to generating peak voltage of V1+V2 at the input (Vad) which is always equal or greater than the *vs max*. On the other hand, by splitting the produced DC voltage between two output terminals, each one would have half voltage amplitude so their amplitude are always less than or equal to the *vs max* that guarantees the buck mode operation of proposed rectifier from loads points of view. It could be concluded that by using two output terminals, the grid is deluded by the converter. Therefore, the stepped down DC voltages are achieved however the overall rectifier is in step-up mode. As results, the bulky inductor at DC side as well as the capacitor filter at AC side of conventional PFC buck rectifiers would be removed. Moreover, low harmonic Vad and also low THD line current (*is*) are attained even when the proposed rectifier is running at low switching frequency leads to low power losses and high efficiency.

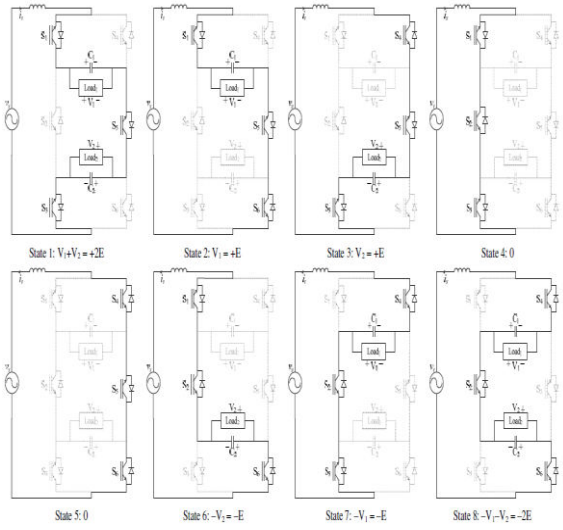

Fig.2. Operating sequences and conducting paths of proposed HPUC 5-level buck rectifier

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III. CONTROLLER FOR PFC RECTIFIER

A cascaded PI controller has been applied to regulate the three state space variables including capacitors voltages (V1 & V2) as well as grid current (*is*) and to provide a unity power factor operation of the five-level rectifier. Figure shows the block diagram of the implemented controller. A phase lock loop (PLL) block is used to extract the voltage angle and generate the synchronized current reference i_S* which should be drawn by the rectifier in order to ensure the power factor correction. The outer loop of the cascaded controller includes the voltage regulator which its output goes to the current controller (inner loop) as the reference signal amplitude.

Therefore, to have balanced voltages at the output DC terminals, sum of the DC voltages are regulated using a PI controller. Each DC voltage reference is assumed as Vref, thus the total DC voltage reference would be 2Vref. PI regulator minimizes the total DC voltages at 2Vref as shown in Figure. Afterwards, the voltage balancing technique integrated into the switching method (as described in section III) is applied to ensure equal voltage amplitude (V1 = V2 = Vref) at DC buses. Concluding that the controller is regulating total DC voltage as Vref using the flowing current through the converter while the switching technique and redundant states would charge and discharge the capacitors equally to have identical voltage levels (Vref) at the DC output terminals. That decoupled voltage control helps balancing capacitors voltages even in faulty conditions where the switching actions could not balance two DC voltages while the sum of DC voltages is regulated at 2Vref. This mode helps preventing any uncontrolled charging up of the capacitors to an unlimited level.

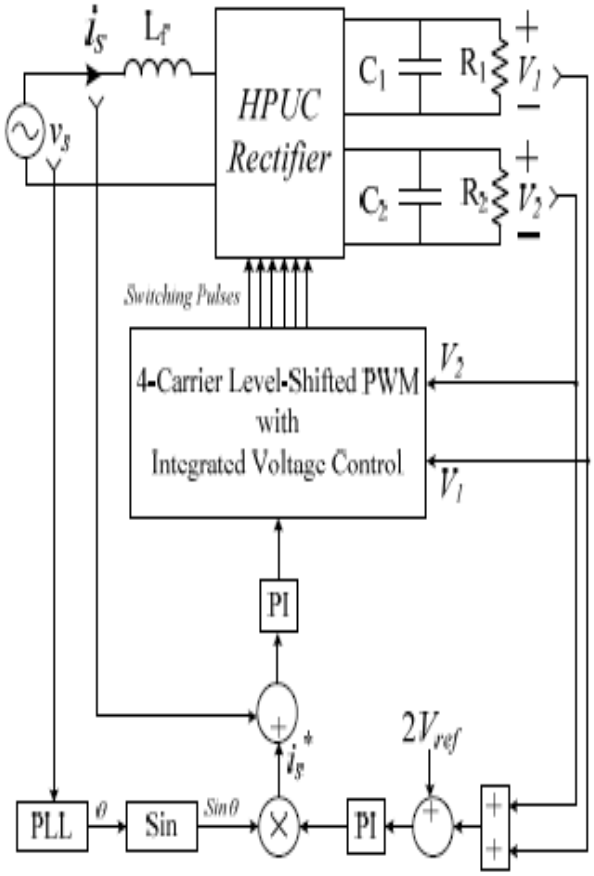

Fig 3. Block diagram of the HPUC rectifier and Implemented controller

It should be noted for the inner loop (current control) PI controller have good performance where the input signal frequency is low (e.g. outer loop as DC voltage regulator); while it shows some steady-state error when the input is a time-varying signal, like a sinusoidal current, leads to tracking error in the line current . To ensure the possible minimum error on the output current, the integral gain of the current control PI block should be small enough which makes the inner loop faster than outer loop as well as not that small which is required to eliminate steady state error and consequently results would be acceptable

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IV.SIMULATION RESULTS

A) EXISTING RESULTS

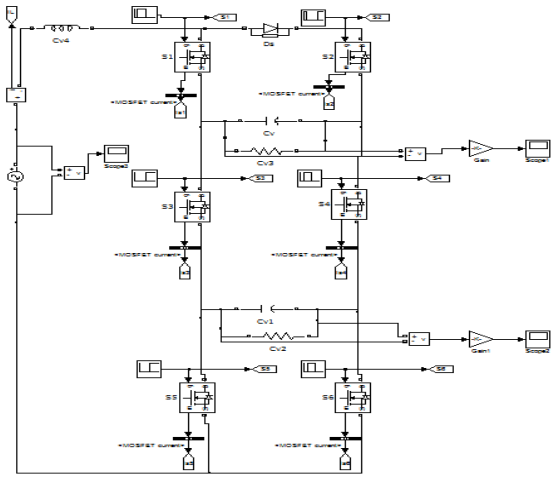

Fig 4. Matlab/Simulink Diagram of Existing Multi Output PFC Rectifier System

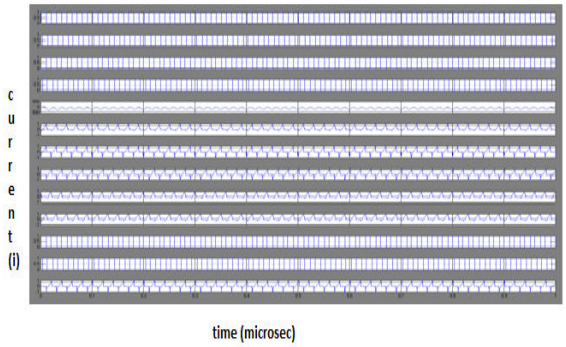

Fig .5 Switching pulses and switching currents

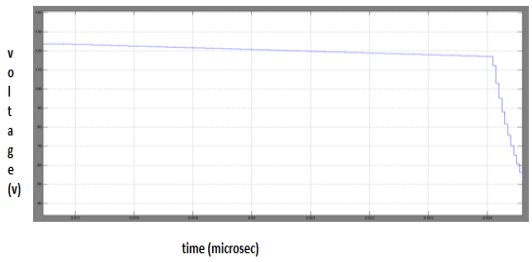

Fig.6 Dc voltage V1

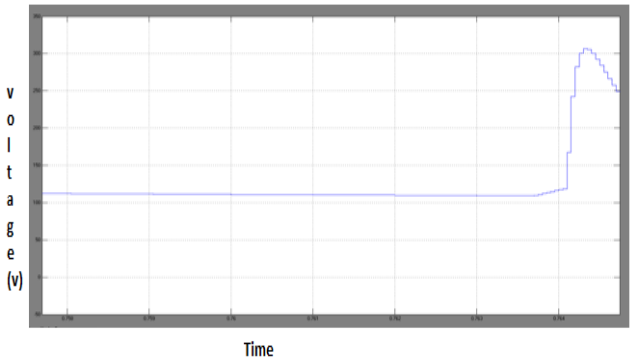

Fig.7 Dc voltage V2

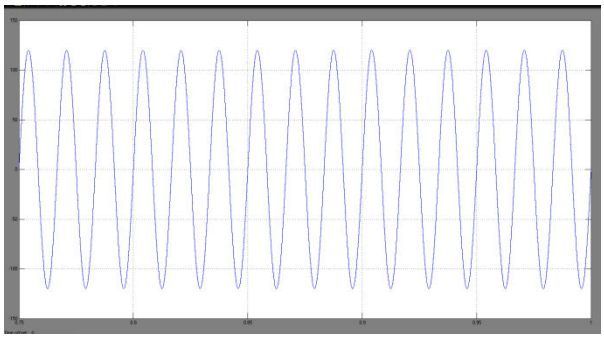

Fig.8 Grid voltage

B) EXTENSION RESULTS

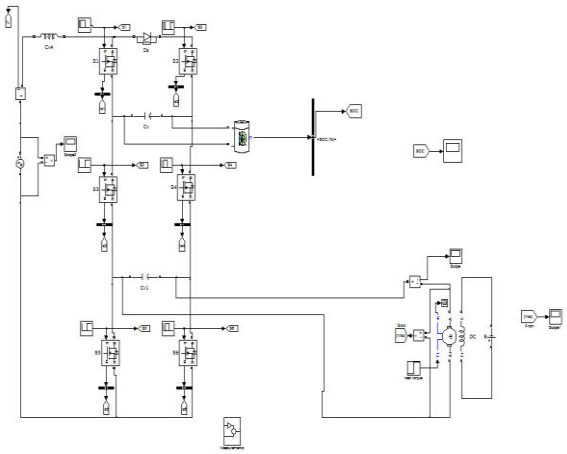

Fig 9. MATLAB/SIMULINK diagram of proposed multilevel rectifier with battery and dc motor

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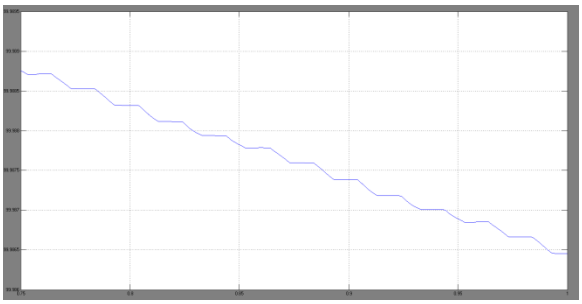

Fig 10. Battery SOC%

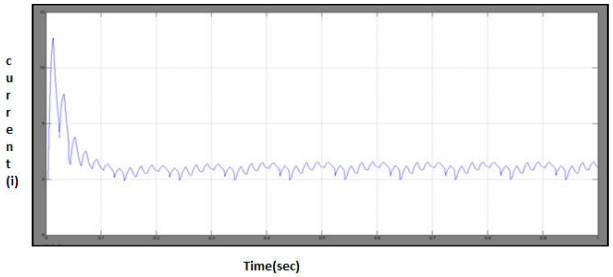

Fig 11. DC motor current

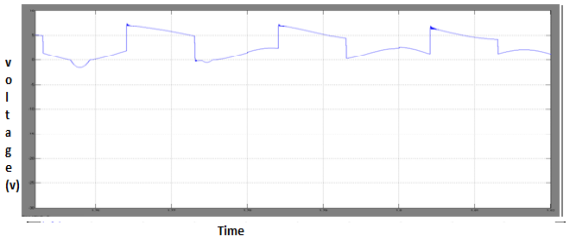

Fig 12. Voltage

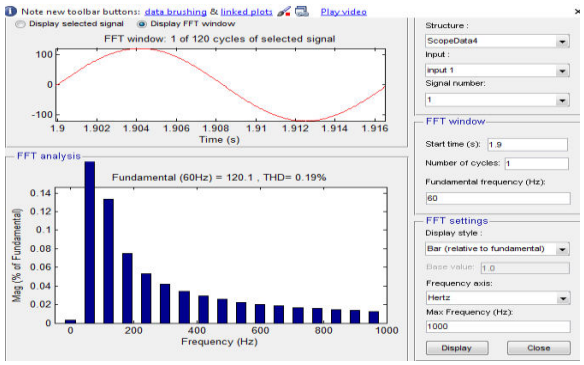

Fig13. THD% of voltage of rectifier

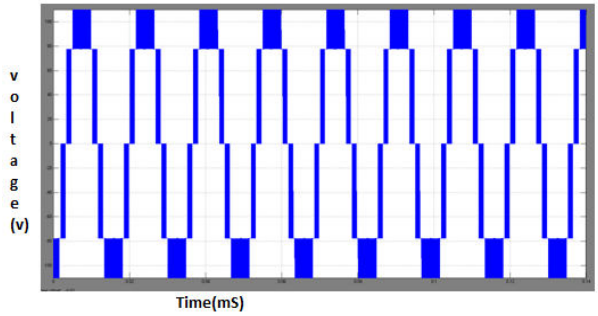

Fig 14. Five level rectifier voltage

CONCLUSION

A 5-level rectifier operating in buck mode has been proposed which is called HPUC as a slight modification to PUC multilevel converter. It has been demonstrated that the proposed rectifier can deceive the grid by generating maximum voltage level of 250V at AC side as boost mode while splitting this voltage value at its two output terminals to provide buck mode of operation with 125V DC useable for battery chargers or telecommunication boards' feeder. Although it has more active switches than other buck rectifier topologies and some limitations on power balance between loads, overall system works in boost mode and CCM which results in removing bulky AC and DC filters that usually used in conventional buck PFC rectifiers. Moreover, generating multilevel waveform leads to reduced harmonic component of the voltage waveform and consequently the line current. It also aims at operating with low switching frequency and small line inductor that all in all characterizes low power losses and high efficiency of the HPUC rectifier. Comprehensive theoretical studies and simulations have been performed on power balancing issue of the HPUC rectifier. Full experimental results in steady state and during

load and supply variation have been illustrated to prove the fact that HPUC topology can be a good candidate in a new family of buck bridgeless PFC rectifiers with acceptable performance. Future works can be devoted to developing robust and nonlinear controllers on the proposed rectifier topology.

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