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Implementation of an XOR Based 16-bit Carry Select Adder for Area, Delay and Power Minimization

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***Abstract*— In different types of processors and other digital circuits adders are most widely used. Low power and area efficient high-speed circuits are most substantial area in the research of VLSI design. The carry select adder is one of the fast adders which has less area and reduced power consumption. In this paper, a 16-bit carry select adder has been presented using modified XOR based full adder to reduce circuit complexity, area and delay. The modified full adder design requires only two XOR gates and one multiplexer. The modified 16-bit carry select adder gives better result than conventional carry select adder with respect to area, power consumption and delay.**

Keywords— low power, area efficient, XOR based adder, carry select adder

I. INTRODUCTION

In digital integrated circuit design, addition is the heart of computer arithmetic. It has special significance in processors and many other digital circuits. In rapidly growing mobile industry faster units, smaller area and less power become major concern [6]. For increasing portability of mobile electronics, area and power are the key factors. They also major concern to increase battery life. In VLSI system, reduction in area and power are the main focus point of research. Faster speed for addition and multiplication is a fundamental requirement of high-performance processors [7]. Arithmetic units are the work horse of a computational circuit and addition is the heart of this. In VLSI sub system the power efficient and high-performance adders are most desired digital circuit. Speed of adder is usually limited for carry propagation bit. The sum of each bit in an adder is generated sequentially after the addition of previous bit and a carry propagated to the next position [8].

There are plenty of adder designs available in the literature such as Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA), Carry Select Adder (CSA), Carry Skip Adder which have their own advantages and disadvantages. CSA is one of the fastest adders because of its less area and power consumption. In CSA there are two multiplexed RCA which act in parallel assuming carry in, Cin = 0 and in other Cin = 1, then final sum is selected through multiplexer. In conventional CSA, XOR, AND and OR gate based full adders are used. These adders consumes more area in the chip due to large number of transistors are used in these gates, the delay is higher and consumes more power [9]. In the present work, XOR based modified full adder have been used as the building blocks of the modified CSA to reduce area, delay and power consumption. The layout of the 16-bit CSA is designed in Micro wind software. The results obtained from the layout data is compared with the conventional CSA [10].

II. XOR BASED FULL ADDER

A full adder which is the main building block of n-bit adders gives the result of addition with output carry taking input carry in to consideration [11]. So, actually a one-bit full adder adds three one-bit numbers A, B, and Cin where A and B are the operands, and Cin is a bit carried in from the previous less-significant stage. A conventional full adder implementation based on basic logic gates is shown in Fig. 1.

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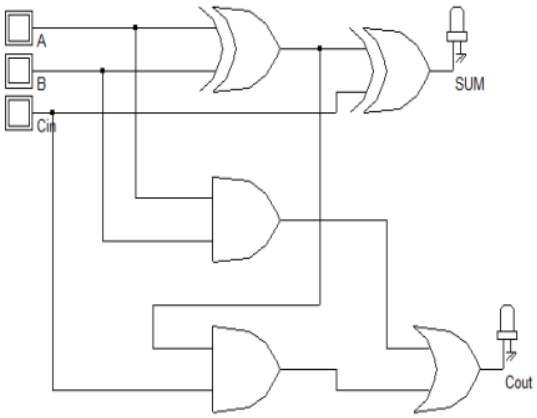

Fig. 1: Conventional 1-bit full adder

A binary full adder realization employing two XOR gates and one 2:1 MUX is shown in Fig. 2. The layout of conventional and XOR based 1-bit full adder are shown in Fig. 3 and Fig. 4 respectively. The advantage of XOR based adder is that it requires smaller number of transistors [12].

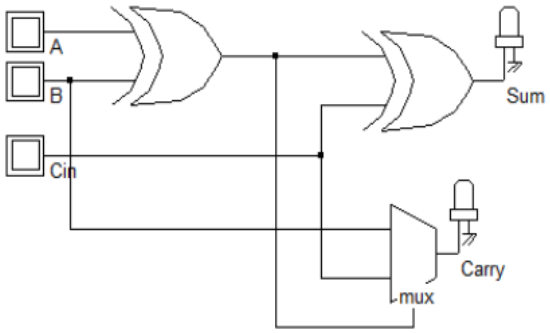

Fig. 2: XOR based 1-bit Full Adder

The main difference between the conventional and XOR based adders is that in XOR based adder other than two XOR gates only one 2:1 MUX is used which needs only 6 MOSFETs where as in conventional type adder other than two XOR gates two AND gates and one OR gate is needed which requires at least 18 number of MOSFETs. So, there is at least 12 numbers of MOSFET savings in XOR based 1-bit adders than conventional which in turn has less area and power consumption at the same time there is also a better delay performance [13].

III. CARRY SELECT ADDER

The CSA is constructed from two RCAs and a multiplexer. Addition of two n-bit numbers with CSA is nothing but adding two numbers taking input carry first as zero then using another adder taking input carry as one. After calculation of the two results depending on the correct carry-in the correct sum as well as the correct carry-out is selected with the multiplexer connected at last to get the final output.

The structure of a 16-bit CSA is shown in Fig. 5. A 16-bit CSA consists of 16-full adders with the carry signal that ripples from one full adder stage to the next, i.e. from LSB to MSB [4]. The layout and input-output wave shapes of a 4-bit CSA are shown in Fig. 6 and Fig. 7 respectively. Due to clarity of the pictures, layout and input output waves of 4-bit CSA are given here in place of 16-bit adder. Results of 16-bit CSA will be given later [14]. Since XOR based 1-bit adders have been used in the 16-bit CSA which are the main building blocks so the number of MOSFETs required is much less than conventional CSA [15].

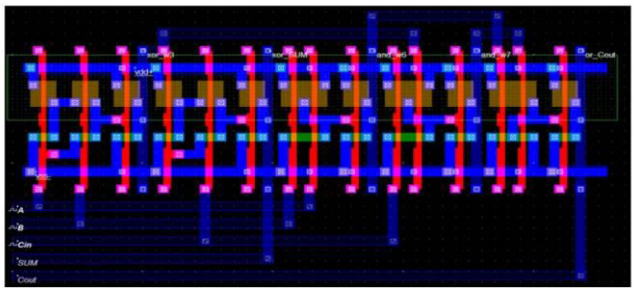

Fig. 3: Layout of conventional 1-bit full adder

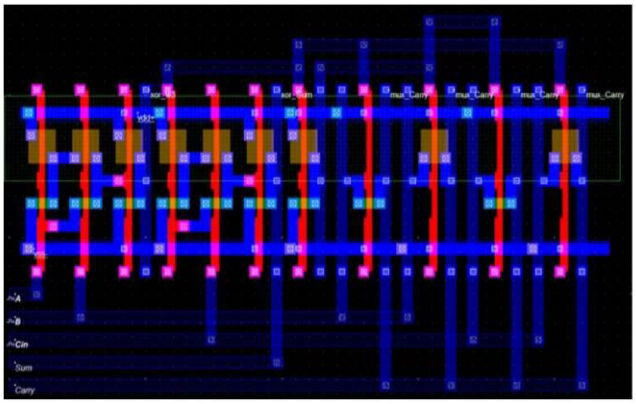

Fig. 4: Layout of XOR based 1-bit full adder

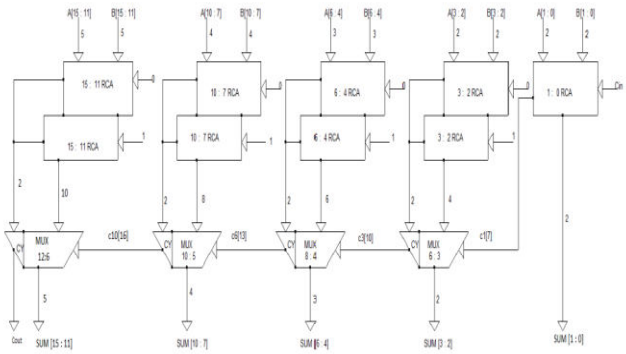

Fig. 5: 16-bit carry select adder

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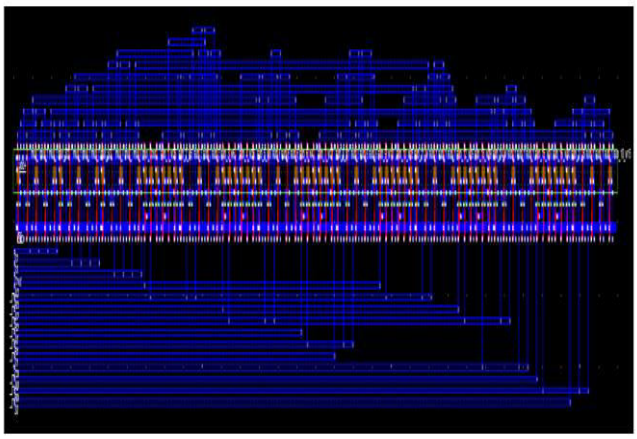

Fig. 6: Layout of 4-bit carry select adder

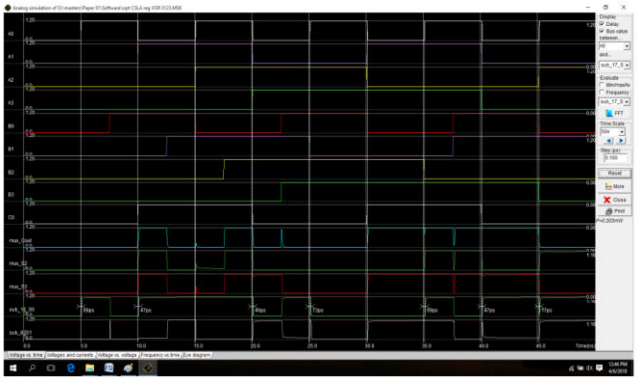

Fig. 7: Input-output wave shapes of a 4-bit carry select adder

IV. RESULTS AND DISCUSSION

The schematic circuit of the CSA has been designed using DSCH 3.1 simulator and synthesized using 90 nm CMOS technology. The layout was constructed from the Verilog file which is generated from the DSCH software. The obtained power, area and delay information of the adder is from Microwind layout simulation [16].

Table I shows the simulation results of both conventional and modified CSA (using XOR based adder) in terms of power, area, delay and power delay product (PDP). Every individual cell in the design adds to the aggregate cell zone and total power is the sum of leakage power, switching power and static power. The XOR-based circuit has the power reduction for 4-bit, 8-bit and 16-bit are 12.5%, 16.67% and 20.04% respectively. Similarly percentage reduction in area are 1.35%, 6.6% and 9.41% respectively. There is also a delay reduction of 0.8%, 1.3%, and 2.01% respectively. In Table II, gate count and Idd values are shown for 4-bit, 8-bit and 16-bit CSA respectively. In Table III, power, delay and area for 8-bit and 16-bit adders are compared with Ref [17].

TABLE I. COMPARISON OF POWER, AREA AND DELAY BETWEEN CONVENTIONAL CSA AND XOR BASED CSA

Bit size	Adder	Power (mW)	Area (μm²)	Delay (ns)	PDP (pWSec)
4-Bit	Conventional CSA	0.232	287.00	2.561	0.594
	XOR based CSA	0.203	283.12	2.538	0.515
	Percentage reduction	12.5%	1.35%	0.8%	13.29%
8-Bit	Conventional CSLA	0.300	580.855	2.520	0.756
	XOR based CSA	0.250	542.485	2.487	0.622
	Percentage reduction	16.67%	6.6%	1.3%	17.72%
16-Bit	Conventional CSLA	2.803	1170.14	5.117	14.34
	XOR based CSA	2.241	1060.01	5.014	11.24
	Percentage reduction	20.04%	9.41%	2.01%	21.62%

TABLE II. COMPARISON OF GATE COUNT, IDD MAX AND IDD AVG BETWEEN CONVENTIONAL CSA AND XOR BASED CSA

Bit size	Adder	Gate count			I_{dd} max (mA)	I_{dd} avg (mA)
		nMOS	pMOS	Total		
4-Bit	Conventional CSA	99	99	198	1.679	0.193
	XOR based CSA	63	63	126	1.389	0.169
	Percentage reduction	36.37%	36.37%	36.37%	17.28%	15.54%
8-Bit	Conventional CSA	195	195	390	2.231	0.550
	XOR based CSA	123	123	246	2.132	0.459
	Percentage reduction	36.93%	36.93%	36.93%	4.44%	16.55%
16-Bit	Conventional CSA	386	386	772	6.626	2.336
	XOR based CSA	243	243	486	5.023	2.316
	Percentage reduction	37.04%	37.04%	37.04%	24.19%	0.86%

TABLE III . COMPARISON WITH OTHER WORK

Bit size	Parameters	Ref. [5]	This work
8-Bit	Power (mW)	13.598	0.250
	Delay(ns)	2.094	2.487
	Area (μm²)	952.343	542.485
16-Bit	Power (mW)	29.311	2.241
	Delay (ns)	2.450	5.014
	Area (μm²)	1901.093	1060.01

V. CONCLUSION

A 16-bit CSA is implemented in this paper using XOR based 1-bit full adder as a building block. The schematic has been designed in DSCH software and synthesized using 90 nm CMOS technology. The layout has been created and simulated in Microwind software. From the simulation result 20.40% reduction in power consumption, 9.41% reduction in area and 2.01% reduction in delay has been achieved for an XOR-based 16-bit CSA than conventional CSA. Also 37.04% reduction in gate count and 24.19% current reduction were found.

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