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Volume 06, Issue 05, Page No: 1908 – 1912.

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A RECONFIGURABLE FIR FILTER ARCHITECTURE OF FIR FILTER PERFORMANCE FOR DYNAMIC POWER CONSUMPTION

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ABSTRACT:

Transpose form finite-impulse response (FIR) filters are inherently pipelined and support multiple constant multiplications (MCM) technique that results in significant saving of computation. However, transpose form configuration does not directly support the block processing unlike direct-form configuration. In this paper, we explore the possibility of realization of block FIR filter in transpose form configuration for area-delay efficient realization of large order FIR filters for both fixed and reconfigurable applications. Based on a detailed computational analysis of transpose form configuration of FIR filter, we have derived a flow graph for transpose form block FIR filter with optimized register complexity. A generalized block formulation is presented for transpose form FIR filter. We have derived a general multiplier-based architecture for the proposed transpose form block filter for reconfigurable applications. A low-complexity design using the MCM scheme is also presented for the block implementation of fixed FIR filters. The proposed structure involves significantly less area delay product (ADP) and less energy per sample (EPS) than the existing block implementation of direct-form structure for medium or large filter lengths, while for the short-length filters, the block implementation of direct-form FIR structure has less ADP and less EPS than the proposed structure. Application specific integrated circuit synthesis result shows that the proposed structure for block size 4 and filter length 64 involves 42% less ADP and 40% less EPS than the best available FIR filter structure proposed for reconfigurable applications. For the same filter length and the same block size, the proposed structure involves 13% less ADP and 12.8% less EPS than those of the existing direct-form block FIR structure. The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx.

Keywords: Finite-Impulse Response, Multiple Constant Multiplications.

I. INTRODUCTION

In this paper, we explore the possibility of realization of block FIR filter in transpose form configuration for area-delay efficient realization of large order FIR filters for both fixed and reconfigurable applications. Based on a detailed computational analysis of transpose form configuration of FIR filter, we have derived a flow graph for transpose form block FIR filter with optimized register complexity. A generalized block formulation is presented for transpose form FIR filter. We have derived a general multiplier-based architecture for the

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proposed transpose form block filter for reconfigurable applications. A low-complexity design using the MCM scheme is also presented for the block implementation of fixed FIR filters. The proposed structure involves significantly less area delay product (ADP) and less energy per sample (EPS) than the existing block implementation of direct-form structure for medium or large filter lengths, while for the short-length filters, the block implementation of direct-form FIR structure has less ADP and less EPS than the proposed structure. Applicationspecific integrated circuit synthesis result shows that the proposed structure for block size 4 and filter length 64 involves 42% less ADP and 40% less EPS than the best available FIR filter structure proposed for reconfigurable applications. For the same filter length and the same block size, the proposed structure involves 13% less ADP and 12.8% less EPS than that of the existing direct-form block FIR structure.

II.EXISTING SYSTEM:

The output of an FIR filter of length N can be computed using the relation:

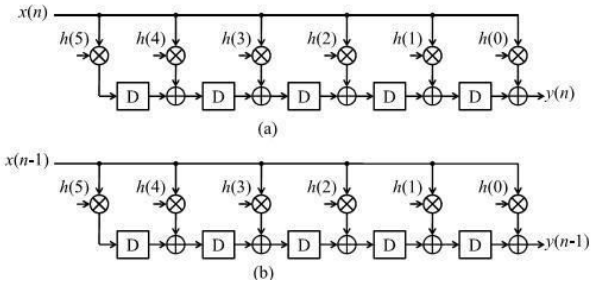

Fig. 1. DFG of transpose form structure for N =6. (a) DFG-1 for output y(n). (b) DFG-2 for output y (n−1).

A. Computational Analysis:

The data flow graphs (DFG-1 and DFG-2) of transpose form FIR filter for filter length N=6, as shown in Fig.1, for a block of two successive outputs{y(n),y(n−1)} that are derived from (2). The product values and their accumulation paths in DFG-1 and DFG-2 of Fig. 1 are shown in dataflow tables (DFT-1 and DFT-2) of Fig. 2. The arrows inDFT-1 and DFT-2 of Fig. 2 represent the accumulation path of the products.

ccs	M_1	M_2	M_3	M_4	M_5	M_6
1	$x(n-5)h(5)$	$x(n-5)h(4)$	$x(n-5)h(3)$	$x(n-5)h(2)$	$x(n-5)h(1)$	$x(n-5)h(0)$
2	$x(n-4)h(5)$	$x(n-4)h(4)$	$x(n-4)h(3)$	$x(n-4)h(2)$	$x(n-4)h(1)$	$x(n-4)h(0)$
3	$x(n-3)h(5)$	$x(n-3)h(4)$	$x(n-3)h(3)$	$x(n-3)h(2)$	$x(n-3)h(1)$	$x(n-3)h(0)$
4	$x(n-2)h(5)$	$x(n-2)h(4)$	$x(n-2)h(3)$	$x(n-2)h(2)$	$x(n-2)h(1)$	$x(n-2)h(0)$
5	$x(n-1)h(5)$	$x(n-1)h(4)$	$x(n-1)h(3)$	$x(n-1)h(2)$	$x(n-1)h(1)$	$x(n-1)h(0)$
6	$x(n)h(5)$	$x(n)h(4)$	$x(n)h(3)$	$x(n)h(2)$	$x(n)h(1)$	$x(n)h(0)$

(a)

ccs	M_1	M_2	M_3	M_4	M_5	M_6
1	$x(n-6)h(5)$	$x(n-6)h(4)$	$x(n-6)h(3)$	$x(n-6)h(2)$	$x(n-6)h(1)$	$x(n-6)h(0)$
2	$x(n-5)h(5)$	$x(n-5)h(4)$	$x(n-5)h(3)$	$x(n-5)h(2)$	$x(n-5)h(1)$	$x(n-5)h(0)$
3	$x(n-4)h(5)$	$x(n-4)h(4)$	$x(n-4)h(3)$	$x(n-4)h(2)$	$x(n-4)h(1)$	$x(n-4)h(0)$
4	$x(n-3)h(5)$	$x(n-3)h(4)$	$x(n-3)h(3)$	$x(n-3)h(2)$	$x(n-3)h(1)$	$x(n-3)h(0)$
5	$x(n-2)h(5)$	$x(n-2)h(4)$	$x(n-2)h(3)$	$x(n-2)h(2)$	$x(n-2)h(1)$	$x(n-2)h(0)$
6	$x(n-1)h(5)$	$x(n-1)h(4)$	$x(n-1)h(3)$	$x(n-1)h(2)$	$x(n-1)h(1)$	$x(n-1)h(0)$

(b)

Fig. 2. (a) DFT of multipliers of DFG shown in Fig. 1(a) corresponding to output y(n). (b) DFT of multipliers of DFG shown in Fig. 1(b) corresponding to output y (n−1). Arrow: accumulation path of the products.

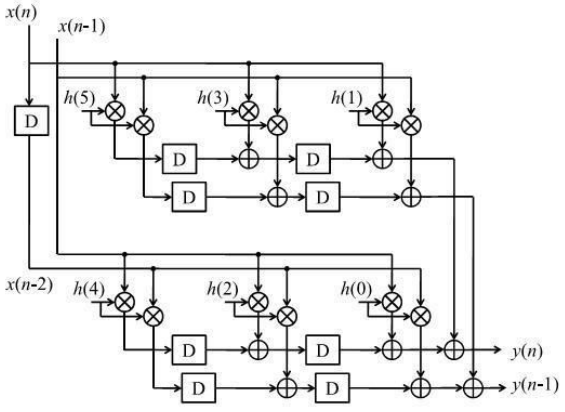

Fig 3. Merged DFG (DFG-3: transpose form type-I configuration for block FIR structure).

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B. DFG Transformation:

The computation of DFT-3 and DFT-4 can be realized byDFG-3 of non-overlapping blocks, as shown in Fig. 3. We refer it to block transpose form type-I configuration of block FIR filter. The DFG-3 can be retimed to obtain the DFG-4 of Fig. 4, which is referred to block transpose form type-II configuration.Note that both type-I and type-II configurations involve the same number of multipliers and adders, but type-II configuration involves nearly L times less delay elements than those of type-I configuration. We have, therefore, used block transpose form type-II configuration to derive the proposed structure. In Section II-C, we present mathematical formulation of block transpose form type-II FIR filter for a generalized formulation of the concept of block-based computation of transpose form FIR filers.

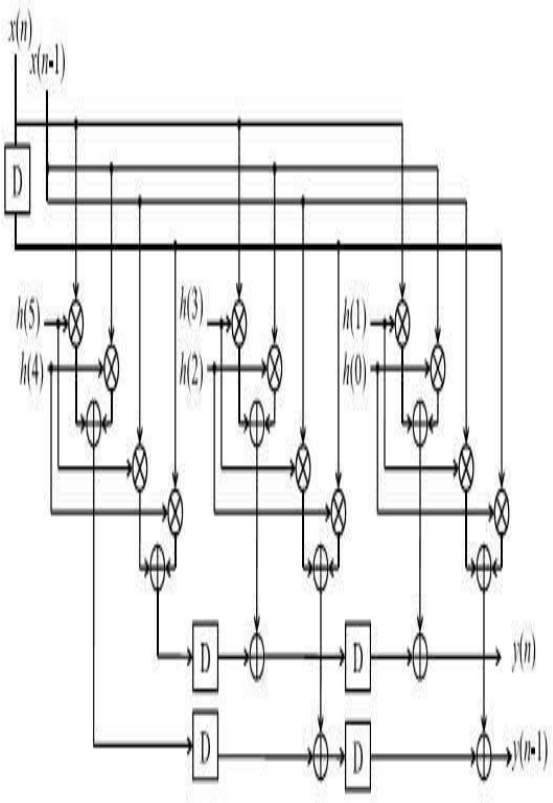

Fig. 4. DFG-4 (retimed DFG-3) transpose form type-II configuration for block FIR structure.

TABLE I MCM IN TRANSPOSE FORM BLOCK FIR FILTER OFLENGTH 16 AND BLOCK SIZE 4

Input sample	Coefficient Group
$x(4k)$	$\{h(0), h(4), h(8), h(12)\}$
$x(4k-1)$	$\{h(0), h(4), h(8), h(12)\}$ $\{h(1), h(5), h(9), h(13)\}$
$x(4k-2)$	$\{h(0), h(4), h(8), h(12)\}$ $\{h(1), h(5), h(9), h(13)\}$ $\{h(2), h(6), h(10), h(14)\}$
$x(4k-3)$	$\{h(0), h(4), h(8), h(12)\}$ $\{h(1), h(5), h(9), h(13)\}$ $\{h(2), h(6), h(10), h(14)\}$ $\{h(3), h(7), h(11), h(15)\}$
$x(4k-4)$	$\{h(1), h(5), h(9), h(13)\}$ $\{h(2), h(6), h(10), h(14)\}$ $\{h(3), h(7), h(11), h(15)\}$
$x(4k-5)$	$\{h(2), h(6), h(10), h(14)\}$ $\{h(3), h(7), h(11), h(15)\}$
$x(4k-6)$	$\{h(3), h(7), h(11), h(15)\}$

C. MCM-Based Implementation of Fixed-Coefficient FIR Filter:

We discuss the derivation of MCM units for transpose form block FIR filter, and the design of proposed structure for fixed filters. For fixed-coefficient implementation, the CSU of Fig. 5 is no longer required, since the structure is to be tailored for only one given filter. Similarly, IPUs are not required. The multiplications are required to be mapped to the MCM units for a low-complexity realization. In the following, we show that the proposed formulation for MCM-based implementation of block FIR filter makes use of the symmetry in input matrix $\mathbf{S}0k$to perform horizontal and vertical common sub expression elimination and to minimize the number of shift-add operations in the MCM blocks.

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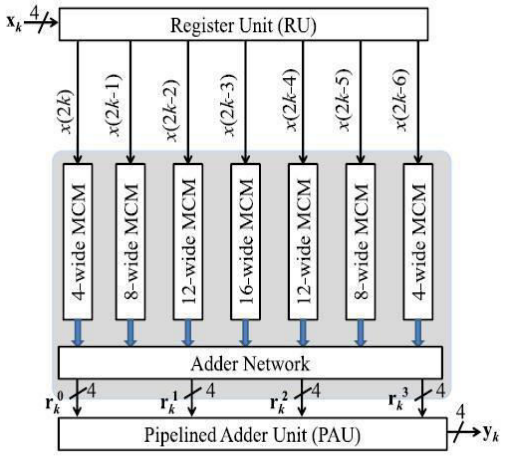

Fig 5. Proposed MCM-based structure for fixed FIR filter of block size L = 4 and filter length N = 16.

As shown in Table I, MCM can be applied in both horizontal and vertical direction of the coefficient matrix. The sample *x (4k−3)* appears in four rows or four columns of the followingWhereas x (4k) appears in only one row or one column. Therefore, all the four rows of coefficient matrix are involved in the MCM for the x (4k − 3), whereas only the first row of coefficients are involved in the MCM for x (4k). For larger values of N or the smaller block sizes, the row size of the coefficient matrix is larger that results in larger MCM size across all the samples, which results into larger saving in computational complexity.

Disadvantages

- Element usage is high
- Cycle period is high

III. PROPOSED SYSTEM

In phase 1 to discussed about 16 tap FIR filter for Low pass, High pass, Band pass, and band stop filter and to analysis the performance, efficiency, speed, and power consumption for the respective filter types. Fig.6 shows the block diagram of the proposed system. The NCO used for signal generation with required frequency range. NCO is used in the modulation block.

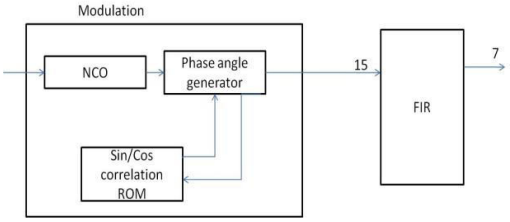

Fig6.

A. Filter types:

Basically filters are classified into 4 types based on rejection of the frequency range.

1. Low pass filter
2. High pass filter
3. Band pass filter
4. Band stop filter

Low pass filter is pass the below frequency range of the given or design frequency value and reject the above frequency range. High pass filter is pass the above frequency range of the given or design frequency value and reject the below frequency range. Band pass filter to pass the between the range of given values and reject the others frequency. But band stop filter to reject the between the range of given values and pass the others frequency.

Advantages:

- reduced filter length
- less element to used
- reduced cycle period

Software Implementation:

- Modelsim
- Xilinx 14.2

IV.CONCLUSION

In this paper, we have explored the possibility of realization of block FIR filters in transpose form configuration for areadelay efficient realization of both fixed and reconfigurable applications. A generalized block formulation is presented for transpose form block FIR filter, and based on that we have derived transpose form block filter for reconfigurable applications. We have presented a scheme to

identify the MCM blocks for horizontal and vertical subexpression elimination in the proposed block FIR filter for fixed coefficients to reduce the computational complexity. Performance comparison shows that the proposed structure involves significantly less ADP and less EPS than the existing block direct-form structure for medium or large filter lengths while for the short-length filters, the existing block direct-form structure has less ADP and less EPS than the proposed structure. Application-specific integrated circuit synthesis result shows that the proposed structure for block size 4 and filter length 64 involve 42% less ADP and 40% less EPS than the best available FIR filter structure of [10] for reconfigurable applications. For the same filter length and the same block size, the proposed structure involves 13% less ADP and 12.8% less EPS than that of the existing direct-from block FIR structure of [15].

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