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A 64-BIT FFT MULTIPLICATON USING VEDIC MULTILICATION SUTRA

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ABSTRCT: Fast Fourier Transform is widely used in various fields like image and signal processing, Voice recognition systems etc. This paper "FFT using Vedic multiplication sutra"proposes a novel technique in order to improve speed and reduce the time delay in FFT Multiplication process. Vedic mathematic comprises of 16 sutras in that one of sutras namely UrdhwaTiryakbhyam sutra used here to improve the performance of FFT multiplier.Here, the proposed method "FFT using Vedic multiplication sutra" is compared with the one of the popular multiplier namely Array multiplier in terms of delay which shows better result.

Keywords: Fast Fourier Transform, Array mlutiplier, UrdhwaTiryakbhyam sutra, Vedic Mathematics.

I.INTRODUCTION

FFT is a highly efficient procedure for computing the DFT of finite series and requires less number of computation than that of direct evaluation of the DFT.FFT reduces the computations that of direct the calculation of the coefficients of the DFT can be carried out iteratively. FFT reduces the computation time required to compute a Discrete Fourier Transform and improve the performance by a factor 100 or more over direct evaluation of the DFT. The complex multiplication in FFT algorithm is performed based on the Array algorithm. This algorithm is quite popular in modern VLSI design. A new approach to multiplier design based on ancient Vedic Mathematics is used to improve the speed of multiplication. UrdhwaTiryakbhyam sutra in Vedic mathematics explores a novel method for implementation of 32-point FFT using array multiplier was replaced by Vedic mathematics in Radix-2 algorithm. By using this Vedic mathematics in FFT algorithm, it improves the Speed of FFT algorithm which is used to compute the discrete Fourier transform.

II. FFT ALGORITHM

The Fast Fourier Transform is a highly efficient procedure for computing the Discrete Fourier Transform (DFT) of a finite series and requires less number of computations than that ofdirect evolution of DFT. The FFT is based on computation on

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decomposition and breaking the transform into smaller transforms and combing them to get total transform.The DFT of a sequence can be evaluated using the formula

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-j2\pi nk/N} \quad 0 \le k \le N-1$$

Here FFT multiplication was implemented based on Radix-2 algorithm. In Radix-2 algorithm, two bits are taken as input and we get two output bits dependence upon the arrow operations. The basic block diagram of DIF-FFT was shown in Figure.2.1.

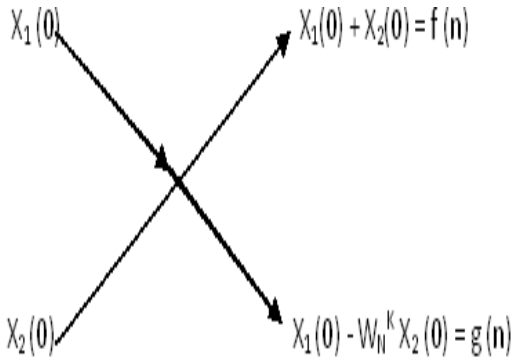

Figure.2.1: Basic butterfly structure of DIF-FFT using Radix-2 algorithm

III. 64-POINT FFT

In 64-point FFT, there are five stages, which contain unique butterfly structure. Input is taken in normal order at first stage and the inputs for other stages dependence upon output generated by preceding stage butterfly structure. The output is taken in bit-reversal order at last stage. The block diagram for 64-point FFT is shown in Figure.2.2

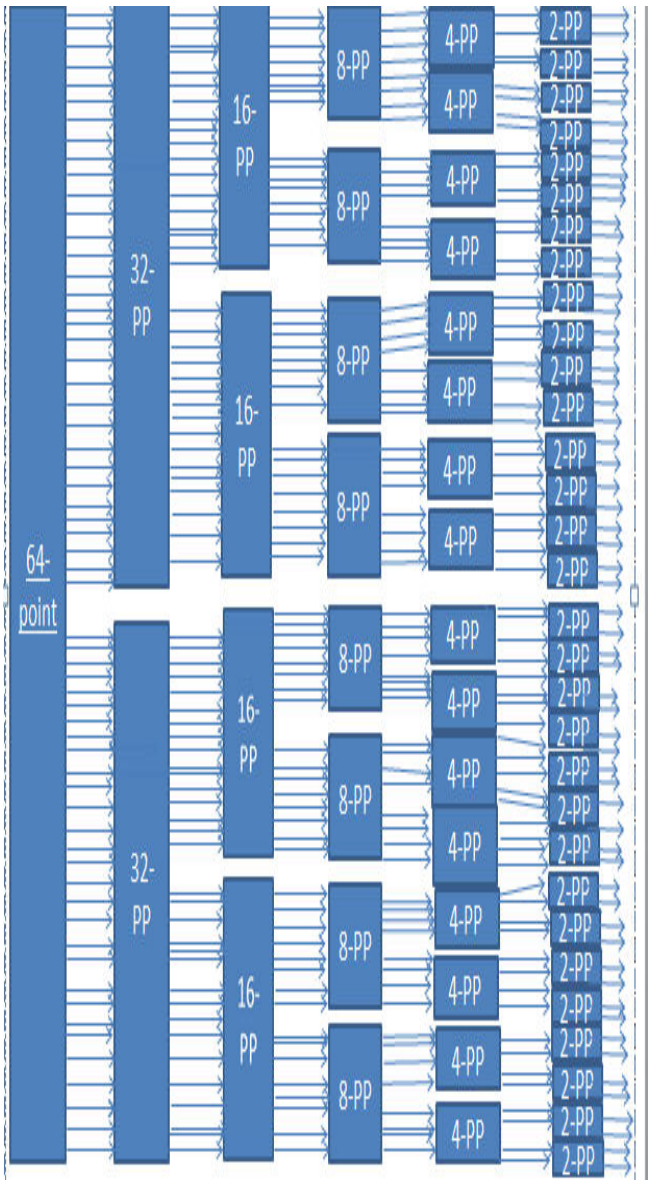

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Figure 3.1:64-point FFT block diagram

IV.ARRAY MULTIPLIER

Array multiplier is an electronic hardware device used in digital electronics or a computer or other electronic device to perform rapid multiplication of two numbers in binary representation. It is built using

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binary adders. The rules for binary multiplication can be stated as follows

1) If the multiplier digit is a 1, the multiplicand is simply copied down

2) If the multiplier digit is a 0 the product is also 0.

For designing a multiplier circuit we should have circuitry to provide or do the following three things:

1) It should be capable identifying whether a bit 0 or 1 is.

2) It should be capable of shifting left partial products.

3) It should be able to add all the partial products to give the products

4) It should examine the sign bits. If they are alike, the sign of the product will be a Positive, if the sign bits are opposite product will be negative. The sign bit of the Product stored with above criteria should be displayed along with the product.

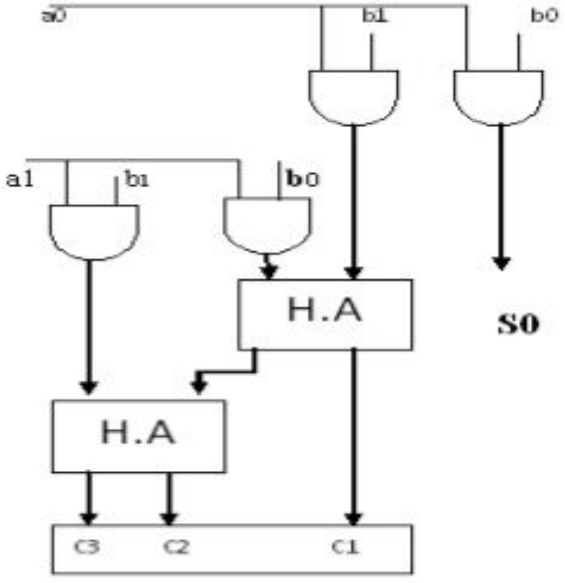

Figure.4.1 General Binary Multiplier

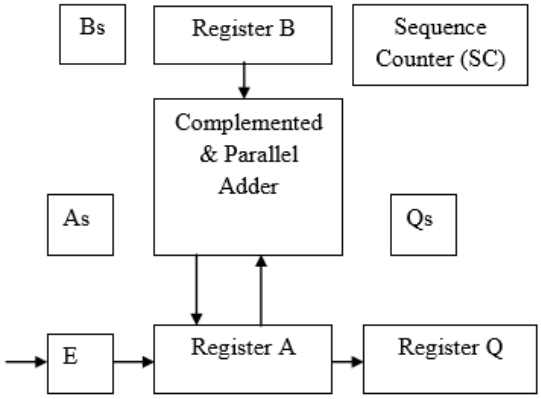

Figure.4.2 Hardware for General Binary Multiplier

V. PROPOSED VEDIC MATHEMATICS

Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc. The proposed Vedic multiplier is based on the Vedic multiplication formulae (Sutras). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. The multiplier is based on an algorithm UrdhvaTiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. UrdhvaTiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The parallelism in generation of partial products and their summation is obtained using UrdhavaTriyakbhyam explained in figure below. The algorithm can be generalized for n x n bit number.

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The proposed 8*8 Vedic multiplier produces was explained in Figure 4.1..

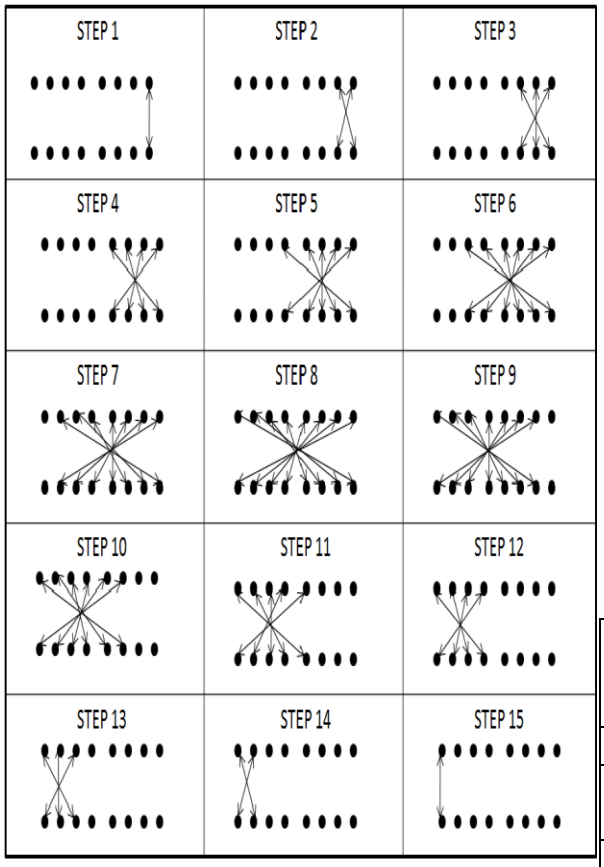

Figure 5.1: Multiplication Process in UrdhvaTiryakbhyam

Equations obtained in Vedic multiplier based on UrdhavaTriyakbhyam sutra are

P0 =A0 * B0
C1P1 = (A1 * B0) + (A0 * B1)

C5C4P3 = (A3 * B0) + (A2 * B1) + (A1 * B2) + (A0 * B3) + C2
C7C6P4 = (A4 * B0) + (A3 * B1) + (A2 * B2) + (A1 * B3) + (A0 * B4) +C3 + C4
C10C9C8P5 = (A5 * B0) + (A4 * B1) + (A3 * B2) + (A2 * B3) + (A1 * B4) + (A0 * B5) + C5
C13C12C11P6 = (A6 * B0) + (A5 * B1) + (A4 * B2) + (A3 * B3) + (A2 * B4) + (A1 * B5) + (A0 * B6) +C7 + C8
C16C15C14P7 = (A7 * B0) + (A6 * B1) + (A5 * B2) + (A4 * B3) + (A2 * B5) + (A1 * B6) + (A0 * B7) +C9 + C11
C19C18C17P8 = (A7 * B1) + (A6 * B2) + (A5 * B3) + (A4 * B4) + (A3 * B5) + (A2 * B6) +(A1 * B7) + C10+C12 + C14
C22C21C20P9 = (A7 * B2) + (A6 * B3) + (A5 * B4) + (A4 * B5) + (A3 * B6) + (A2 * B7) +C13 +C15 + C17
C25C24C23P10 = (A7 * B3) + (A6 * B4) + (A5 * B5) + (A4 * B6) + (A3 * B7) + C16 + C18 + C20
C27C26P11 = (A7 * B4) + (A6 * B5) + (A5 * B6) + (A4 * B7) + C19 + C21 + C23
C29C28P12 = (A7 * B5) + (A5 * B6) + (A5 * B7) + C22 + C24 + C26
C30P13= (A7 * B6) + (A6 * B7) + C25 + C27 + C28
P14 = (A7 * B7) + C29 + C30

VI.RESULTS&CONCLUSION

Here the proposed method "FFT using Vedic mathematics" is compared with existing multipliers in terms of delay with different families of Xilinx10.1 shows that the proposed method has a better result shown in below table.

Families	Radix-2 modified booth algorithm	Proposed Urdha tiryabhyam	
On Spartan-3	52.754	47.85	
On Spartan-3A & Spartan-3AN	47.178	38.72	
On Spartan-3E	46.406	36.66	
On Virtex-2	34.924	30.42	
On Virtex-4	29.51	25.876	
On Virtex-5	23.59	15.75	

Table.1: Time delay (ns) results of the FFT algorithm implementation on xilinx 10.1

REFERENCES:

[1] "Design and Implementation of 32-point FFT using Radix-2 Algorithm for FPGA Implementation" by AsmitaHaveliya, IEEE, Proc. Vol. 978-0-7695-4640-7/12.

[2] "High speed asic design of complex Multiplier using Vedic mathematics" by PrabirSaha, Banerjee and Partha

(3) C32C3C2P2 = (A2 * B0) +
(4)
(5)
(6)
(8)

Bhattacharyya, IEEE, Proc.vol. 978-1-4244-8943-5/11.

[3] "Novel high speed Vedic mathematics multiplier using compressors mathematics" by Sushma R. Huddar and SudhirRao, KalpanaM.andSurabhi Mohan, IEEE, Proc.vol. 978-1-4673-5090-7/13.

[4] **"**Design and performance analysis of 32 and 64-point FFT using Radix-2 algorithm" by K.Sowjanya&B.LeelaKumari, International Conference (IRAJ) ISSN: 978- 81-927147-9-0, 14th July-2013.

[5] "High speed Vedic multiplier" international journal of engineering research volume no.3 issue no: special 2, pp: 73-76, 22 March 2014.

[6] "Design and Implementation of 32-point FFT using Radix-2 Algorithm for FPGA" by Afreen.Fathima, IOSR Journal of Electrical and Electronics Engineering (ISOR-JEEE) e- ISSN: 2778-1676, p-ISSN: 2320-3331, Vol. 9, Jan 2014.

[7] "Efficient implementation of 16-bit Multiplier-accumulator using radix-2 modified booth algorithm and spst adder using verilog"by addankipurnaramesh, Dr.a.v.n.tilak and Dr.a.m.prasad, international journal of vlsi design & communication systems (vlsics) vol.3, no.3, june 2012.

[8] "Efficient Design and Implementation of FFT", by SnehaN.khrede, MeghanaHasamnis, International Journal of Engineering Science and Technology (IJEST), ISSN: 0975-5462 NCICT Special Issue Feb 2011.

[9] "Low Power High Speed 16x16 bit Multiplier using Vedic Mathematics" International Journal of Computer Applications (0975 – 8887) Volume 59– No.6, December 2012.

[10] "Design and performance analysis of 32 and 64-point FFT using multiple radix algorithms" by K.Sowjanyaand LeelaKumari.Ballvada, International Journal of Computer applications, ISSN: 0975-8887, Vol.78-1, September 2013.

[11] **"**Design and implementation of Vedic multiplier" international journal of engineering research and development" e-issn: 2278-067x, p-issn: 2278-800x, volume 8, issue 6 (September 2013), pp.23-28.

[12] "Implementation of Multiplier using Vedic Algorithm" by Poornima M, Shivaraj Kumar Patil, Shivukumar , Shridhar K P , Sanjay H International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-2, Issue-6, May 2013.

[13] "Implementation of power efficient vedic multiplier" international journal of computer applications volume 43– no.16, April 2012.

[14] "Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques" by G.Ganesh Kumar,

V.Charishma, International Journal of Scientific and Research Publications, Volume 2, Issue 3, March 2012, ISSN 2250-3153.