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HARDWARE AND ENERGY-EFFICIENT STOCHASTIC LU DECOMPOSITION SCHEME FOR MIMO RECEIVERS

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ABSTRACT:

In this paper, we design a hardware and energy-efficient stochastic lower–upper decomposition (LUD) scheme for multiple-input multiple-output receivers. By employing stochastic computation, the complex arithmetic operations in LUD can be performed with simple logic gates. With proposed dual partition computation method, the stochastic multiplier and divider exhibit high computation accuracy with relative short length stochastic stream. We have designed and synthesized the stochastic LUD with CMOS 130-nm technology. According to the postlayout report, the hardware efficiency of the stochastic LUD is as high as 1.5× compared with the exiting LUD methods, and the energy efficiency is also higher than the state-of-the-art LUD when the matrix dimension is 8 × 8 and larger.

1. INTRODUCTION

Matrix decomposition is an essential algorithm in the linear solution problem [1]. Especially, in the multipleinput multiple-output (MIMO) systems, matrix decomposition is the main burden for the implementation of hardware and the energy-efficient MIMO detector [2]. The existing matrix decomposition optimization methods aim at large-size matrices such as dimension with 16 kB [3]–[5]. However, in the practical MIMO systems, the scale of antennas is limited by the area of antenna array. For example, in the longterm evolution (LTE) standards, the MIMO systems employ a 4×4 dimension antenna array. Even in the large-scale MIMO system [21], the required inversion matrix dimension is no more than 100. The MIMO systems are interested in more hardware-efficient and energy-efficient VLSI implementation of matrix decomposition algorithm. Generally, there are two main approaches for the matrix decomposition method in MIMO systems: 1) QR decomposition and 2) lower–upper decomposition (LUD) [6]–[11]. QR decomposition algorithm, which transfers a matrix into an orthogonal matrix and an upper triangular matrix, is widely employed in the path-search-based MIMO-detection algorithm [12]. In the other aspect, LUD algorithm factorizes a matrix into a lower triangular matrix and an upper triangular matrix [8]–[11]. LUD has the same function as QR decomposition, which serves for a path search-based MIMO detection. Moreover, LUD is an indispensable processing in the zero-force (ZF) [13] and the minimum mean square error (MMSE)-based MIMO system [2]. In this paper, we focus on the implementation of LUD algorithm. Plenty of LUD methods have been proposed in [3], [4], and [9]–[11], such as parallel-processing-based, circularlinear-array-based, and blocking-based architectures that target on large-size matrices with high throughput. However, energy consumption and hardware complexity are two fatal design criterions in the wireless communication systems, especially for the mobile terminals. Hence, it is necessary to design a high-

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performance LUD scheme specific for the MIMO systems. In [9], an LUD based on computation sharing multiplier (CSHM) is proposed, which has considerable energy-saving capacity. An approximate matrix inversion structure for large-scale MIMO uplink is proposed in [21], which can only be used in the system with massive receiving antenas.

2. PROJECT DESCRIPTION

A. DPC-Based Stochastic Multiplier

The hardware scheme of DPC-based stochastic multiplier is given in Fig. 2. We highlight the logic gates with corresponding function to help understand the structure. Since AL, B L, C L, and DL are Boolean signals, the multiplications in (22) and (24) are implemented by AND gates. The subtraction "-AL(t) · C L(t) · 2k" is performed by operating MSB of the adder outputting signal. The adder is shared by (22) and (24) in 1 → L cycles and L+1 → 2L cycles. The function of (23) is performed by a sign detector, in which a k-input AND gate is employed to obtain the absolute signal a. The MSB represents the signed bit in TCS. Hence, signed signal s is obtained by MSB of register output. To feedback a k +1-bit TCS signal to the adder, we duplicate the MSB bit of register. The signal "Ctl" controls the stochastic multiplier to process two section of the stream E L and F L

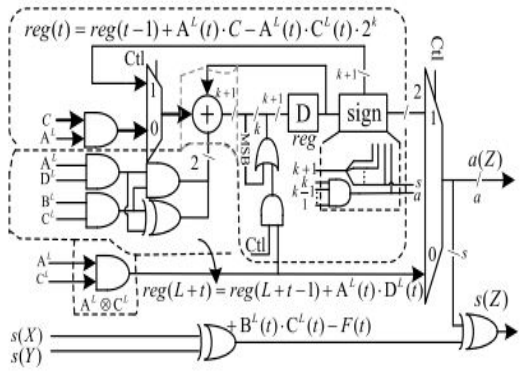

Fig. 2. High-accuracy stochastic multiplier.

B. DPC-Based Stochastic Divider

The hardware implementation scheme of proposed SD is given in Fig. 3. The back converter (B.C.) which converts stochastic stream to FP signal can be bypassed when the input signal is already a TCS signal. To obtain (AL(t) · 2k + B L(t))· 2k, a stream generator (S.G.) is employed with left shifting AL(t) to 22k-bits and B L(t) to 2k-bits. In the first L = 2k cycles, the register is updated with (38). A multiplexer is used to control the register storing the current value according to E L(t). The output signal E L(t) is generated by (37), where a comparison is performed by inverting the MSB of adder output. From 2k + 1 to 2k+1 cycles, the left shifting module at the register output is enabled to perform (41). Notice that "Ctl_p" is a pulse signal with the function.

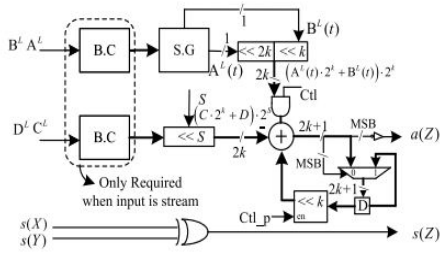

Fig. 3. High-accuracy SD.

Conversion Units

1) Back Conversion Unit: The B.C. unit converts the stochastic stream into the TCS signal, which is widely used in the stochastic logic-based system. The hardware implementation is simple, as shown in Fig. 5(a).

2) Stream Generation Unit: The S.G. unit performs a reverse function of B.C., which generates the stochastic stream with a given TCS signal. It contains an adder, a register, and a multiplexer as shown in Fig. 5(b).
3) DSC Generator: As discussed in Section III-C, uniform distribution vectors in (9) are required to perform the SM. We propose a

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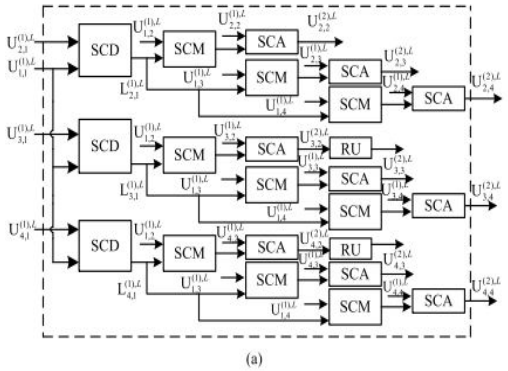
simple and effectively method to implement (9). As shown in Fig. 5(c), we employ a counter with k rising edge detectors. The uniform distribution vectors can also be shared by each signal generator.



(a)

Fig. 4. Parallel LUD scheme processing steps. (a) Stage 1. (b) Stage 2. (c) Stage 3.

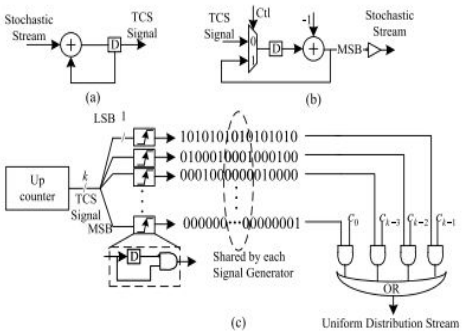


Fig. 5. Conversion units. (a) B.C. (b) S.G. (c) Uniform distribution generator.

E. Block LU Decomposition With Stochastic Computation

The block LUD algorithm can be employed for the large matrix based on stochastic computation. We first review the block LUD algorithm for A = LU where we have (a) A11 = L11U11, (b) A12 = L11U12 (c) A21 = L21U11, (d) A22 = L21U12 + L22U22.

In (a), L11 and U11 is obtained by LUD. Then, we submit L11 and U11 to (b) and (c) to obtain U21 and L21, respectively. Finally, after computing A22-L21U12, we perform LUD again to obtain L22 and U22 in (d). Matrix A22 can be further factorized by the block LUD method.

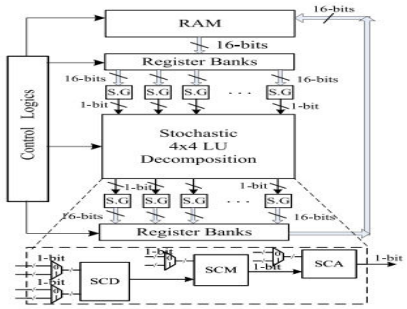


Fig. 6. Block LUD structure.

The hardware architecture is shown in Fig. 6. A RAM is employed to store the matrix elements. The control logic generates reading addresses to access the data from the RAM. The register banks hold the data to perform stochastic computations. After the FP data are converted by S.G., the 1-bit streams are input to the stochastic 4×4 matrix decomposition unit. The 1-bit multiplexers are employed to perform data routing.

3. CONCLUSION

In this paper, we proposed a stochastic-based LUD scheme with high hardware efficiency and power efficiency. In order to achieve high accuracy, we presented several novel techniques to improve stochastic computation performance. The proposed DPC has reduced the computation latency from 2k to 2k/2+1. The high-accuracy SM and SD can achieve SNR performance of 60 dB, which is capable of employing the proposed stochastic logic to the system that requires high computation. The scheme proposed in this paper can also be used in other DSP systems.

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