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POWER QUALITY IMPROVEMENT WITH NINE LEVEL MULTILEVEL INVERTER FOR SINGLE PHASE GRID CONNECTED SYSTEM

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ABSTRACT:
Multilevel inverters are promising, they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact. The inverter is capable of producing nine levels of output-voltage levels from the dc supply voltage. The proposed inverter system is capable of producing nine level of output voltage levels dc supply voltage by using three full bridge cascaded topology type inverter. In this project has used to three H-bridge inverter with different dc sources. The multi-level inverters promising the high performance with reduced EMI and harmonics. This project is focused on minimizing the number of semiconductors devices for a given number of levels. The proposed project is nine-level inverter was designed and results were also shown by using MATLAB/SIMULINK Software.

Keywords: Grid Connected System, Cascaded H-Bridge Multilevel Inverter, Nine level Inverter, Total Harmonic Distortion, Pulse Width Modulation.

I. INTRODUCTION

A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter systemfor a high power application. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources [1-4]. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage ofthe power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM).Multilevel inverters are three types.i. Diode clamped multilevel inverter 2. Flying capacitors multilevel inverter 3. Cascaded H-bridge multilevel inverter. Among those Cascade H-bridge MLI is used in this project

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due to following advantages. They are:i. Switching losses and device stress is less [5].ii. Least number of components are required.iii. Potential of electric shock is less. These inverters are nothing but series connection of single phase inverters with separate dc sources avoid extra clamping diodes and voltage balancing capacitors. N level cascaded H-bridge inverter consists of series connection of (N-1)/2 of cells in each phase. Four active devices in each cell produce three levels like +Vdc,-Vdc,0 as the number of levels M increases number of active switches required are also increases 2(M-1).

Carrier based modulation schemes for multilevel inverter is generally classified into two types:

1. Phase Shifted
2. Level Shifted

In m level multi carrier modulation schemes require (m-1) triangular carrier wave forms. All having same frequency and amplitude. In phase shifted carrier wave forms are horizontally disposed. In level shifted carrier wave forms are vertically disposed.

Most of the level shifted carrier based PWM techniques have been derived three carrier disposition categories. The phases of carrier signals rearrange to produce three main disposition techniques known as

1. PD (Phase Disposition)
2. POD (Phase Opposition and Disposition)
3. APOD (Alternate Phase Opposition and Disposition).

The reference wave positioned at centre of the carrier set continuously compared with carrier waves. When reference goes above all carriers a maximum output is obtained similarly when reference goes down each carrier the corresponding levels in the inverter output gets reduced [6]. CHB topology is advantageous because of individual dc voltage sources which are available like batteries and fuel cells. In diode clamped MLI excess clamping diodes are required as number of levels increases clamping diodes requirement increases rapidly and it is difficult to control the power flow in flying capacitor MLI excess numbers of storage capacitors are required and it is difficult to maintain voltage balance in between capacitors. Now coming to required total number of switches for same level are more in diode clamped and flying capacitor because of clamping diodes and storage capacitors [7-8]. This paper deals with different levels like three, five, seven, nine level topologies of CHB MLI and comparisons of THD of each inverter. By increasing no of levels we can reduce the total harmonic distortion for power quality improvement we have to reduce the harmonic content to meet the minimum harmonic distortion level of IEEE-519.The harmonic content decreases as the number of levels increases and filtering requirement reduces [9-12].

II. CASCADED H-BRIDGE MULTILEVEL INVERTER

Cascaded H-bridge (CHB) multilevel inverter is one of the popular topology for converter used in high power medium voltage drives. It contains multiple units of single phase H-bridge power cells. The H-bridge cells are normally connected in cascaded on its ac side to achieve low harmonic distortion and medium voltage operation. In practice, the number of power cells in a CHB inverter is mainly determines by its operating voltage and the cost

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required for manufacturing. The CHB multilevel inverter requires a number of isolated dc supplies each of which feeds an H-bridge power cell. The number of voltage levels in a CHB inverter can be found from

$$m = 2H + 1 \quad (1)$$

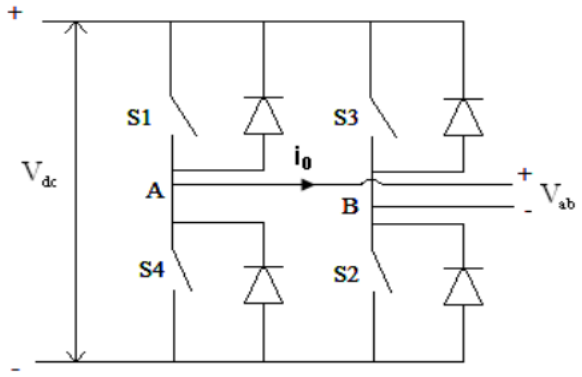
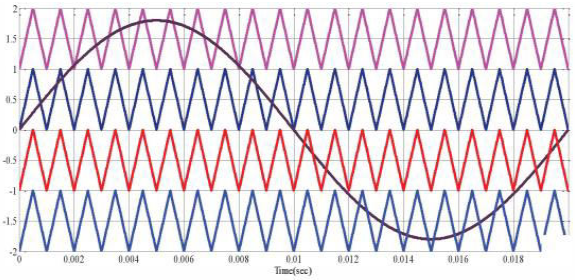


Fig1. Single Phase H-Bridge Inverter

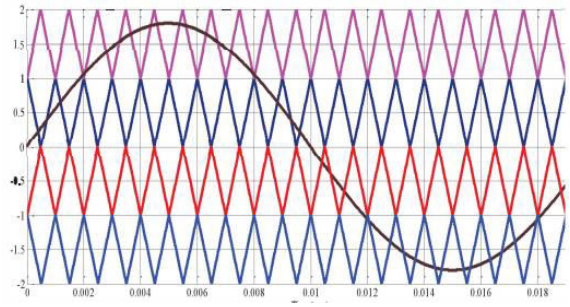
Where H is the number of cells per phase leg in H-bridge. For the CHB inverter, voltage level m is always an odd number while in other multilevel topologies like diode-clamped inverters it can have either an even or odd number of levels. Any carrier based PWM schemes can be used for CHB inverter. The carrier based modulation schemes for multilevelinverter can be classified in two categories as follows

A. Level shifted multicarrier modulation

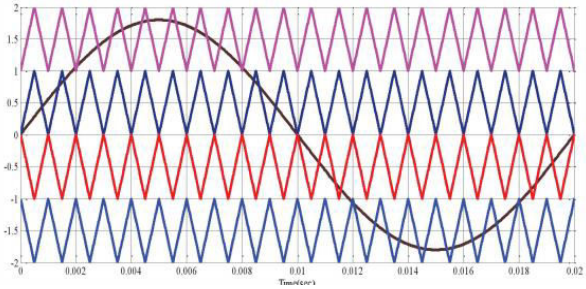
The level shifted modulation scheme requires (m-I) triangular carriers for m-level CHB inverter, all the carriers have the same frequency and the same amplitude. The (m-I) triangular carriers are vertically placed such that the bands forms by the carriers are contiguous. Following figure shows three schemes for the level shifted multicarrier modulation. (a) in-phase disposition (IPD), where all carriers are in phase; (b) alternative phase opposite disposition(APOD), where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition(POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference.



(A):IPD



(B):APOD



(C):POD

Fig.2. Level shifted PWM

The frequency modulation index is given by

$$m_f = f_{cr} / f_m \quad (2)$$

Which remains the same as that for the phase shifted modulation scheme whereas the amplitude modulation index is defined as

$$m_a = \frac{V_m}{V_{cr}(m-1)} \quad (3)$$

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Where Vm is peak amplitude of the modulating wave Vm and Vcr is the peak amplitude of each carrier wave.

B. Phase shifted multicarrier modulation

In general, a multilevel inverter with m voltage levels requires (m-l) triangular carriers. In the phase shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak to peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by

$$\phi_{cr} = 360^{\circ} /(m-1) \quad (4)$$

The modulating signal is usually a three phase sinusoidal wave with adjustable amplitude and frequency. The gate signals are generated by comparing the modulating wave with carrier waves.

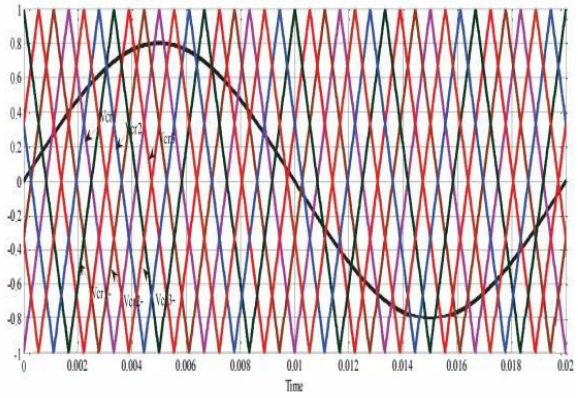

Fig.3. Phase shift PWM for seven-level inverter

The principle of the phase-shifted modulation for a seven level CHB inverter is shown in fig.3, where six triangular carriers are required with a 60° phase displacement (using equation (4)) between any two adjacent carriers. Modulating wave VMA is used. The carriers Veri, Vcr2, and Vcr3 are used to generate gatings for the upper switches Q_1, Q_5, and Q_9 in the left legs of power cells H_1, H_2 and H_3 as shown in fig.3, respectively. The other three carriers, Vcr_1-, Vcr_2-, and Vcr_3- , which are 1800 out of phase with V_{cr1}, V_{cr2}, and V_{cr3}, respectively, produce the gatings for the upper switches Q2, Q6 and Q10 in the right legs of the H- bridge cells. The gate signals for all the lower switches in the H-bridge legs are not shown since these switches operate in a complementary manner with respect to theircorresponding switches. The amplitude modulation index for phase shifted PWM as given in equation (5) is different than level shifted PWM. It does not depend on number of levels.

$$m_a = \frac{V_m}{V_{cr}} \quad (5)$$

Switching table for cascaded H-bridge seven-level inverter is as shown Table 1

Table 1 : Switching Table

Output Voltage	Switching States		
	(Q1,Q2,Q3,Q4)	(Q5,Q6,Q7,Q8)	(Q9,Q10,Q11,Q12)
3E	(1,0,1,0)	(1,0,1,0)	(1,0,1,0)
2E	(1,0,1,0)	(1,0,1,0)	(1,1,0,0)
E	(1,0,1,0)	(1,1,0,0)	(1,1,0,0)
0	(1,1,0,0)	(1,1,0,0)	(1,1,0,0)
-E	(0,1,0,1)	(0,0,1,1)	(0,0,1,1)
-2E	(0,1,0,1)	(0,1,0,1)	(0,0,1,1)
-3E	(0,1,0,1)	(0,1,0,1)	(0,1,0,1)

Basically separate PY panels can be used for delivering power to each unit of multilevel inverter in practical applications.

III. CONTROL STRATEGY

To deliver energy to the grid, the frequency and phase of the inverter must equal those of the grid; therefore, a grid synchronization method is needed. To synchronize the grid frequency with the supply frequency the control action is carried out which is shown in fig.4 below.

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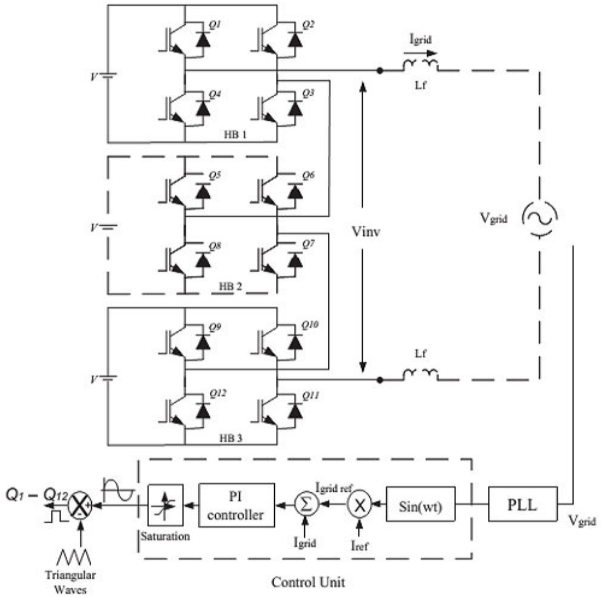


Fig.4. Circuit diagram of Cascaded Seven level Inverter for single phaseGrid Connected System

In this Phase locked loop (PLL) is used to synchronize the grid frequency with the supply frequency which makes the grid voltage and grid current are in phase with each other as shown in simulation result section. The L_f is the current limiting filter to limit the grid current. The current limiting inductor L_f is given by

$$L_f = \frac{V_{DC}}{8 \times f_{sw} \times \Delta I_{L\max}} \quad (6)$$

Where V_{DC} is the DC voltage of the inverter, f_{sw}", is switching frequency of the inductor andΔI_{Lmax} is ripple current of the inductor.

The feedback current controller is used for this application. In this PI algorithm, $I_{ref}$is generated by comparing grid voltage with the reference voltage. Ire f is then multiplied by the output of PLL to generate $I_{gridref}$. The current injected into the grid known as grid current I_{grid}, was sensed and fed back to a comparator that compared it with the reference current Igridref. The error from the comparison process of I_{grid} and I*gridref* was fed into the PI controller. The output of the PI controller, also known as V_{ref}, being compared with the triangular wave to produce the switching signals for Q,-Q'2'.

IV. MATLAB/SIMULINK RESULTS

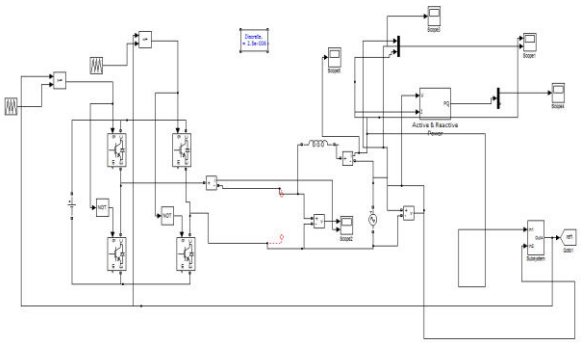
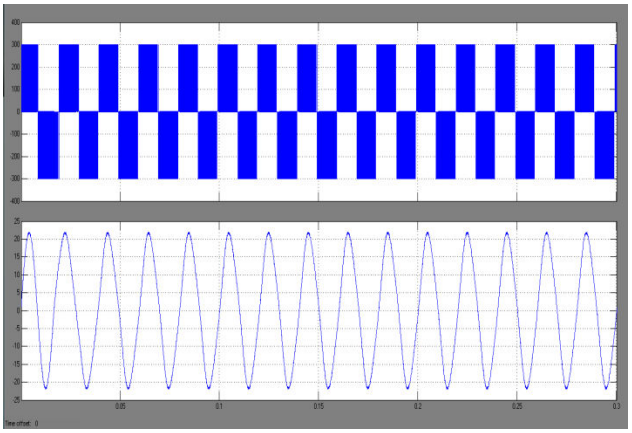


Fig.5. Matlab/Simulink Circuit diagram of Cascaded Three level Inverter for single phase grid connected System



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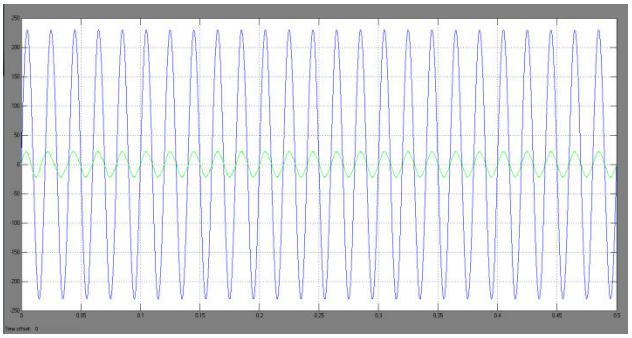

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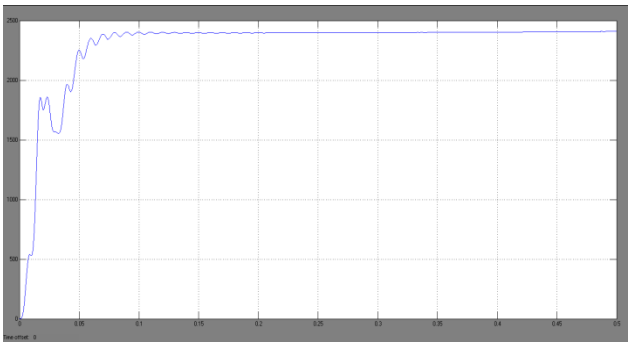

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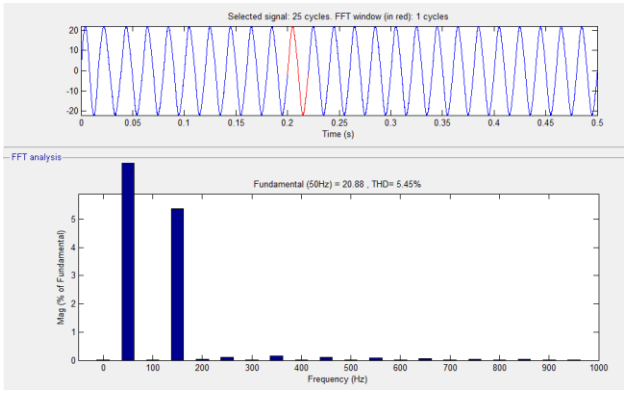


(d)

Fig,6.(a) Three level Output voltage of inverter and grid voltage (b) In phase waveform of grid voltage and grid current (c) Active and Reactive Power of Inverter (d) Harmonic Analysis of Grid Current

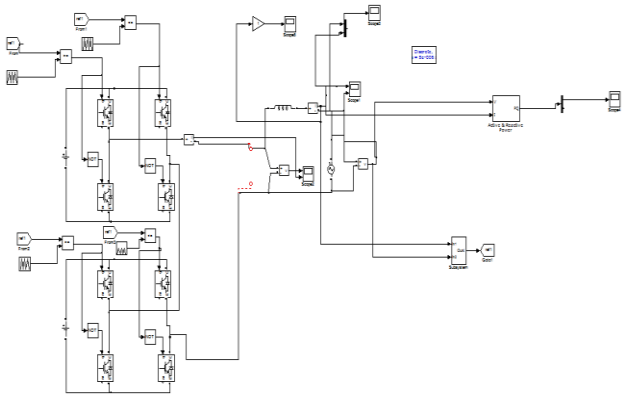
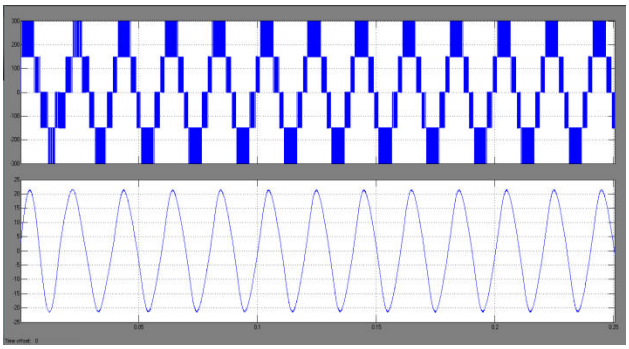


Fig.7.Matlab/Simulink Circuit diagram of Cascaded Five level Inverter for single phase grid connected System



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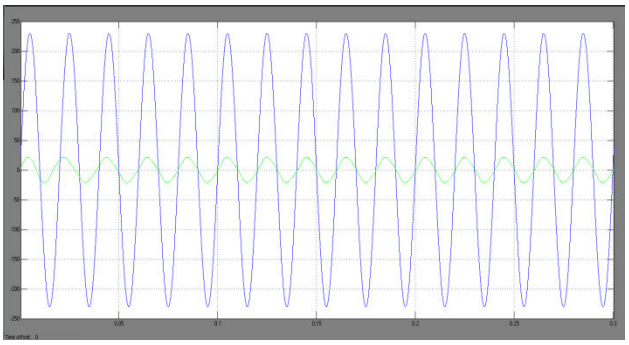

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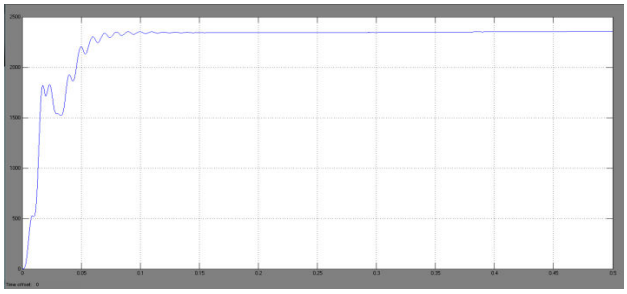

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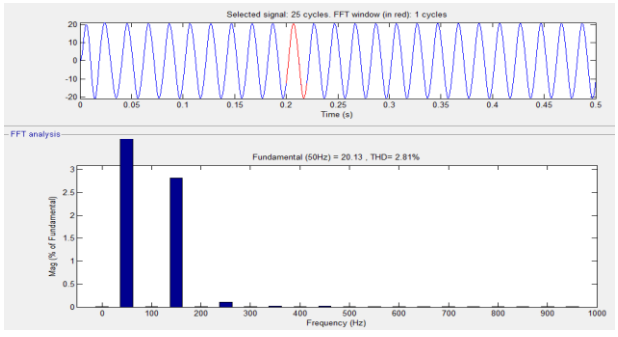

(d)

Fig.8. (a) Five level Output voltage of inverter and grid voltage(b) In phase waveform of grid voltage and grid current (c) Active and Reactive power of inverter (d) Harmonic Analysis of Grid Current

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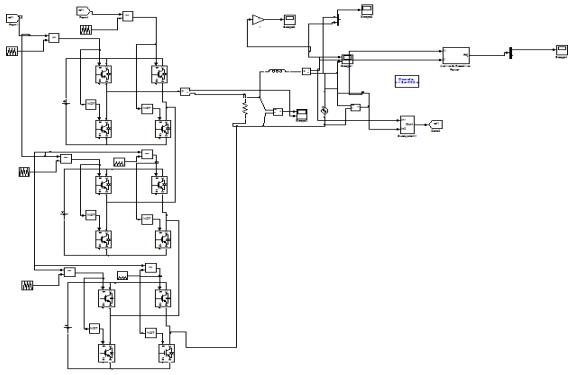
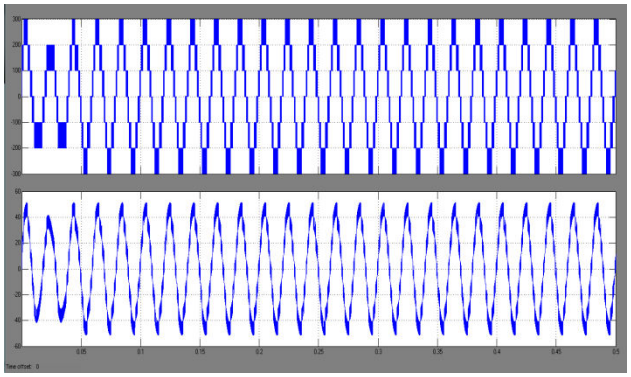
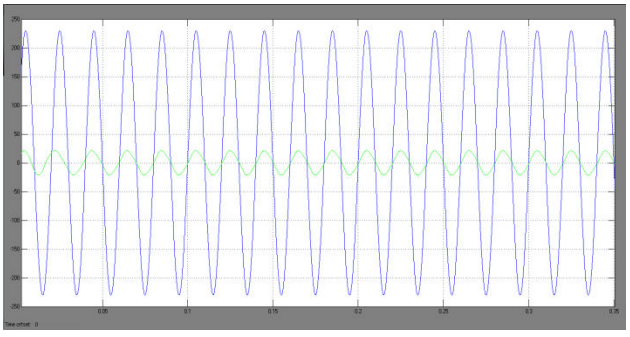


Fig.9.Matlab/Simulink Circuit diagram of Cascaded Seven level Inverter for single phase grid connected System



(a)



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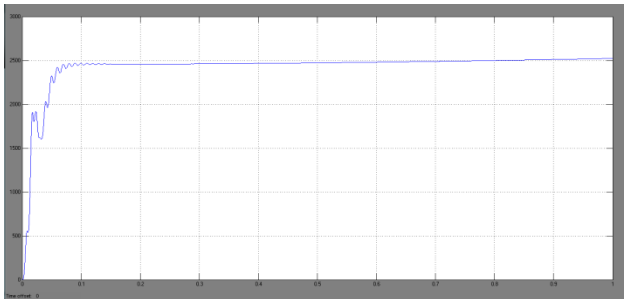

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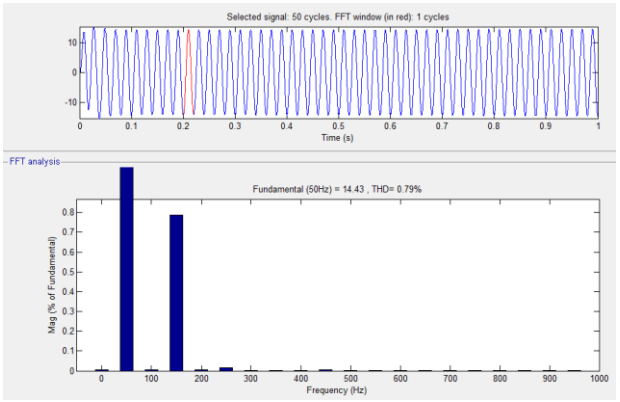


Fig.10. (a) Seven level Output voltage of inverter and grid voltage (b) Inphase waveform of grid voltage and grid current (c) Active and Reactive Power of inverter (d) Harmonic Analysis of Grid Current

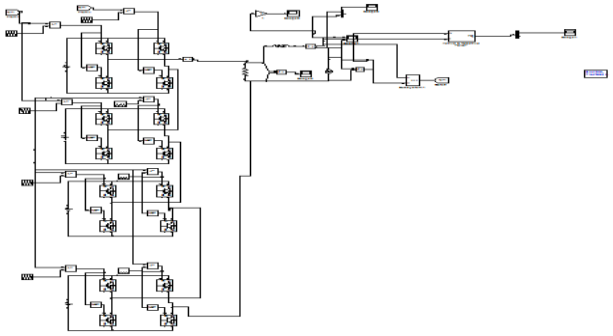
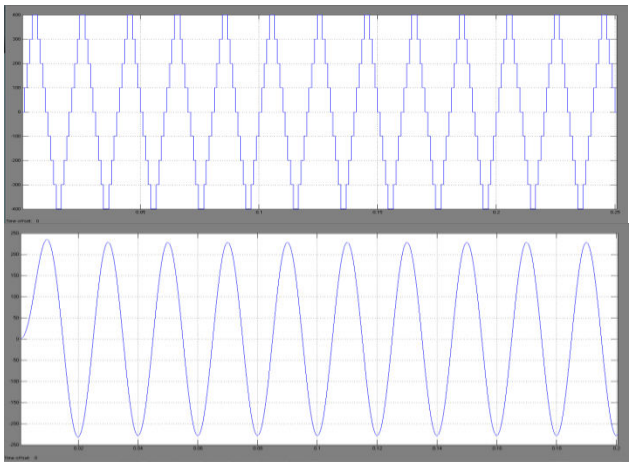


Fig.11.Matlab/Simulink Circuit diagram of Cascaded Nine level Inverter for single phase grid connected System



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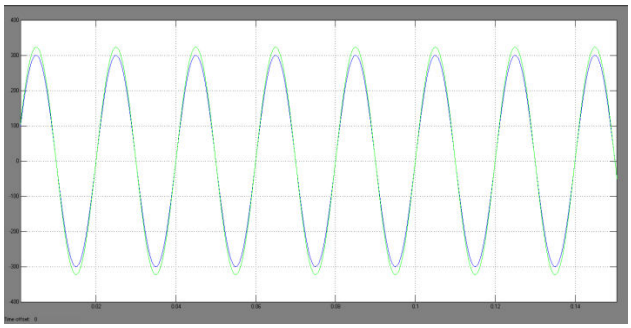

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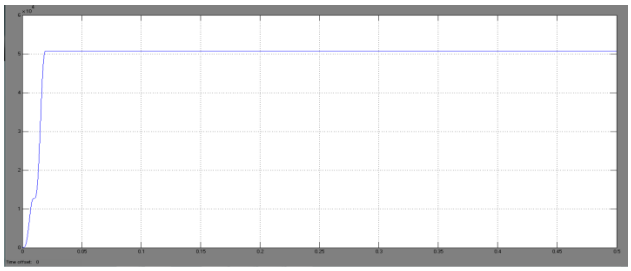

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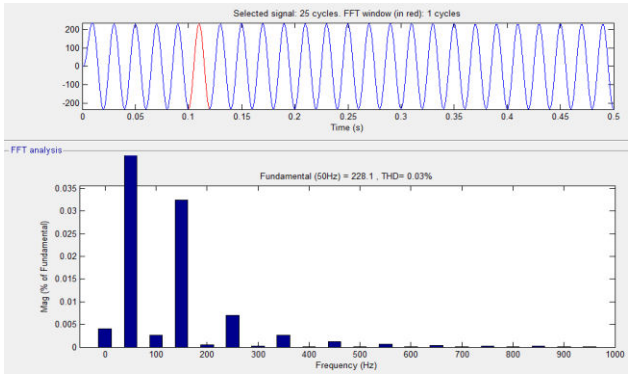

(d)

Fig.12.(a) Nine level Output voltage of inverter and grid voltage (b) Inphase waveform of grid voltage and grid current (c) Active and Reactive Power of inverter (d) Harmonic Analysis of Grid Current.

TABLE III: HARMONIC ANALYSIS

No of Levels	% THD
Three level	5.45%
Five Level	2.81%
Seven Level	0.79%
Nine Level	0.03%

V. CONCLUSION

CascadedH-bridge seven level inverter for single phase grid connectedsystem. Control strategy is carried out to synchronize the gridfrequency with the inverter frequency and to generate themodulating wave to fire the switches of the inverter. The behavior of the proposed multilevelinverter was analyzed in detail. By controlling the modulationindex, the desired number of levels of the inverter's outputvoltage can be achieved.Theharmonic analysis of grid current is carried out for differentlevels. From the analysis it is clear that as the number of levelsincreases the %THD decreases. So multilevel inverter is usedfor grid connected system to inject less harmonic current to thegrid. The level improvement of system is achieved. THD of the system is greatly decreased up to 0.03%.

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