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FLOATING-POINT BUTTERFLY ARCHITECTURE BASED ON CARRY SELECT ADDER REPRESENTATION

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ABSTRACT

Fast Fourier transform (FFT) coprocessor, having a noteworthy crash on the performance of communication systems. The FFT function consists of uninterrupted multiply add operations over complex statistics, dubbed as butterfly units. By applying floating-point (FP) arithmetic to FFT architectures, expressly butterfly units, has become more popular recently. It off-load compute-intensive errands from general-purpose processors by dismissing FP (e.g., scaling and overflow, underflow etc). However, the key downside of FP butterfly is its slowness in contrast with its fixed-point equal. This reveals the spur to develop a high-speed FP butterfly architecture to moderate FP slowness. This brief proposes a fast FP butterfly unit via a devised FP fused-dot-product-add (FDPA) unit, to compute AB ± CD ± E, based on carry select adder (CSA)representation. The FP three-operand CSA adder and the FP CSA constant multiplier are the constituents of the proposed FDPA unit. A CSA adder is planned and used in the three- operand adder and the parallel CSA multiplier so as to improve the speed of the FDPA unit. The blend results show that the proposed FP butterfly architecture is greatly faster than previous architecture. It has an advantage of speedup processes and reducing of gate developing area.

Index Terms – Carry Select Adder (CSA) representation, butterfly unit, Fast Fourier Trans-form (FFT), Floating-Point (FP), three-operand addition

1. INTRODUCTION

Fast Fourier transform (FFT) circuitry consists of numerous consecutive multipliers and adders over complex numbers; thus an appropriate number representation must be selected wisely. Mainly of the FFT architectures have been using fixed-point arithmetic, awaiting recently that FFTs based on floating-point (FP) operations grow up . The core advantage of FP in excess of fixed-point arithmetic is the wide active range it introduces; but at the expense of superior cost. Moreover, use of IEEE-754-2008 usual for FP arithmetic allows for an FFT coprocessor in alliance with general purpose processors. This off-load compute-intensive tasks from the processors and lead to higher performance. The main downside of the FP operations is their slowness in comparison with the fixed-point counterparts. A way to velocity up the FP arithmetic is to come together several operations in a single FP unit, and hence save delay, area, and power utilization. By means of redundant number systems is another renowned way of overcome FP slowness, where there is no word-wide carry propagation within the intermediate operation. A number system, distinct by a radix r and a digit-set [α, β], is outmoded if $\beta-\alpha+1>r$. The renovation, from non-redundant, to a redundant layout is a carry-free operation; on the other hand, the undo conversion requires carry-propagation. This make redundant representation extra of use everywhere numerous consecutive arithmetic operations are carry out prior to the final result. This brief proposes a butterfly architecture by means of redundant FP arithmetic, which is functional for FP FFT coprocessors and contribute to digital signal processing application. Even though there are other plant on the use of redundant FP number systems, they are not optimized for butterfly architecture

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in which together redundant FP multiplier and adder are obligatory. The put your feet up of this concise is structured as follows. Section II is constant tothe proposed FP butterfly architecture. Finally, the termination is drawn in Section III.The FFT possibly will be implemented in hardware based on an efficient algorithm in which the N-input FFT totaling is simplified to the computation of two (N/2)-input FFT. Abiding this decomposition leads to 2-input FFT block, also known as butterfly unit.The proposed butterfly unit is in reality a complex fused- multiply–add with FP operands. Expanding the complex numbers, Fig. 1 shows the required modules.

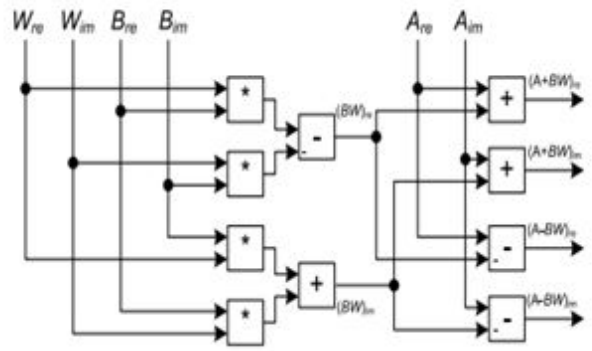

Figure 1 FFT Butterfly architecture with expanded complex numbers.

According to Fig. 1, the part operations for butterfly unit are a dot-product (e.g., Bre Wim +Bim Wre) follow by an addition/subtraction which lead to the projected FDPA operation (e.g., Bre Wim +Bim Wre +Aim). Implementation facts of FDPA, over FP operands, are discuss below.

2. RELATED WORK

The brief proposes a butterfly architecture using redundant FP arithmetic, which is useful for FP FFT coprocessors and contributes to digital signal processing applications. Although there are other works on the use of redundant FP number systems, they are not optimized for butterfly architecture in which both redundant FP multiplier and adder are required. The novelties and techniques used in the existing design include the following

1) All the significands are represented in binary signed digit (BSD) format and the corresponds carry-limited adder is designed.

2) Design of FP constant multipliers for operands with BSD significands.

3)Design of three-operand adders for operands with BSD significands.

4) Design of FP fused-Dot-Product-Add (FDPA) units. Redundant Floating-Point Multiplier

5) The multiplier, likewise other parallel multipliers, consists of two major steps, namely

- Partial Product Generation (PPG) and
- Partial Product Reduction (PPR).

However, contrary to the conventional multipliers, our multiplier keeps the product in redundant format and hence there is no need for the final carry-propagating adder. The exponents of the input operands are taken care of in the same way as is done in the conventional FP multipliers; however, normalization and rounding are left to be done in the next block of the butterfly architecture (i.e., three-operand adder)

Partial Product Generation:

The PPG step of the proposed multiplier is completely different from that of the conventional one because of the representation of the input operands (B, W, B, W). Moreover, given that Wre and Wim are constant, the multiplications in Fig. 1

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(over significant) can be computed through a series of shifters and adders. With the intention of reducing the number of adders, we store the significant of Win modified Booth encoding.

Given the modified Booth representation of Wre and Wim, one PP, selected from multiplicand B, is generated per two binary positions of the multiplier W, shows the required circuitry for the generation of PPi based on Table I where each PP.li consists of (n+1) digits (i.e., binary positions).

Partial Product Reduction:

The major constituent of the PPR step is the proposed carry- limited addition over the operands represented in CSA format. This carry-limited addition circuitry is shown in Fig. 2 (two- digit slice).Since each PP (PPi) is (n+1)-digit (n,...,0) which is either B (n−1,...,0) or 2B(n,...,1), the length of the final product may be more than 2n.

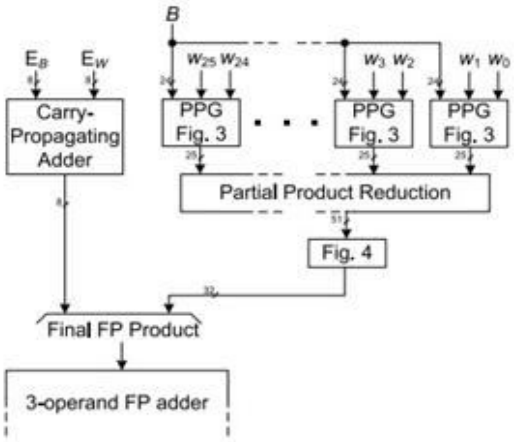

Figure 2 Existing redundant FP multiplier

1. PROPOSED MODELLING

The straightforward approach to perform a three-operand FP addition is to concatenate two FP adders which lead to high latency, power, and area consumption. A better way is to use fused three-operand FP adders.

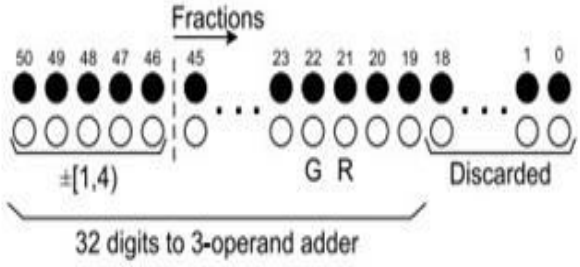

Figure 3 Digits to three-operand adder.

In the proposed three-operand FP adder, a new alignment block is implemented and BSD is replaced by the CSA adders (Figure.5). Moreover, sign logic is eliminated.

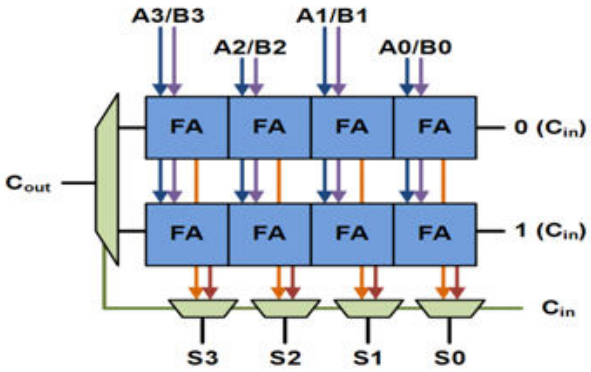

Figure 4 CSA adder

The carry-select adder in general consists of two ripple carry adders and a multiplexer. Adding up two n-bit numbers with a carry-select adder is ready with two adders (therefore two ripple carry adders) in arrange to perform the estimate twice, one time with the postulation of the carry-in being zero and the other haughty it will be one. After the two outcome are calculated, the accurate sum, as well as the correct carry-out, is then elected with the multiplexer once the right carry-in is known.

The number of bits in each carry select building block can be regular, or variable. In the regular case (Fig.3), the optimal delay occur for a block size of $\lfloor \sqrt{n} \rfloor$. When variable, the block

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size should have a delay, from adding up inputs A and B to the carry out, equal to that of the multiplexer series leading into it, so that the carry out is calculated just in time. The $O(\sqrt{n})$ delay is consequent from uniform sizing, where the model number of full-adder essentials per block is equal to the square root of the number of bits being supplementary, since that will yield an equal number of MUX delays. Theproposed FDPA consists of redundant FP multiplier followed by a redundant FP three-operand adder with construction of carry select adder (CSA).

The bigger exponent between EX and EY (called E Big) is deter- mined using a binary subtractor (= *EX – EY)* and the significand of the operand with smaller exponent (X or Y) is shifted bit to the right. Next, a CSA adder computes the addition result (SUM= X +Y), using the aligned X and Y. Adding third operand (i.e., SUM+A) requires another alignment. This second alignment is done in a different way so as to reduce the critical path delay of the three-operand adder. First, the value of A = EBig − EA + 30 is computed which shows the amount of right shifts required to be performed on extended A (with the initial position of 30 digits shifted to left). Fig. 5 shows the alignments implemented in the proposed three-operand FP adder. Next, a CSA adder adds the aligned third significand to SUM generated from the first CSA adder. Since the input operands have different number of digits, this adder is a simplified CSA adder.

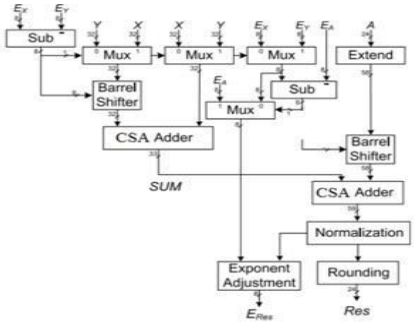

Figure 5 Proposed FP three-operand addition

Next steps are normalization and rounding, which are done using conventional methods for BSD representation It should be noted that the leading zero detection (LZD) block could be replaced by a four-input leading-zero-anticipation for speed up but at the cost of more area consumption. The other modification would replace our single path architecture withthe dual path to sacrifice area for speed. The proposed FP three-operand adder is implemented as shown in Figure 5 in which new alignment and addition blocks are introduced. Moreover, due to the sign-embedded representation of the significands (i.e., CSA), a sign logic is not required.

4. RESULTS AND DISCUSSIONS

A comparison of the proposed design with the conventional one is shown in Table I.

	CONVENTIONAL	PROPOSED
Exponent comparison& significant alignment	2x(8bit sub) 4xMUX 2x Shifter +30 Block	2x(8bit sub) 4xMUX 2X Shifter
Sig.Addition	2x BSD Adder	2 xCSA Adder
Critical Path Delay	Sub+MUX+Shifter +(+30)+Com.+BSD Adder	Sub+MUX+Shif ter+Com.+CSA Adder
Sign Logic	No	

Table 1 conventional and proposed design comparison

The critical path of the three-operand adder, consists of two 8-bit carry-propagating subtractor (0.25 ns each), a MUX (0.07 ns), a 30 block (0.17 ns), a barrel shifter (0.29 ns), and the final CSA adder (0.16 ns); plus normalization and rounding (0.75 ns) and registers (0.22 ns). Given that the proposed

butterfly architecture is meant to be used in an FFT unit, the reverse conversion is done in the very last iteration of the FFT unit. Therefore, the latency of each stage is equal to that of a butterfly unit plus those of registers.

5. CONCLUSION

We proposed a FP butterfly architecture, which occupy lesser area than the previous. The reason for this area decrement is twofold:
1) CSA representation of the significant which select the particular carry and
2) The new FDPA unit proposed in this brief.
This unit combines multiplications butterfly; thus reduced area is achieved by eliminating extra LZD, normalization, and rounding units. Further research may be envisaged on applying dual-path FP architecture to the three-operand FP adder and using other redundant FP representations.

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