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SINGLE PHASE CLOCK DISTRIBUTION USING LOWPOWER AND MULTIBAND PRESCALAR

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ABSTRACT

Normally the clock distribution network will consume about 70% of the total power consumed by the IC because this is the only signal which has the highest activity. Basically for a multi clock domain network we develop a multiple PLL to cater the need, but it consumes more power. So, the main aim of this project is developing a low power single clock multiband network which will supply for the multi clock domain network. It is highly useful and recommended for communication applications like Bluetooth, Zigbee, and WLAN. It is modeled using Verilog simulated using Modelsim and implemented in Xilinx.

Keywords – Prescaler, PLL, Programmable Counter, Swallow Counter, MOD, sel, clk, MC.

1. INTRODUCTION

Division operation is very important in the computer system. For division algorithm earlier they used Phased Lock loop (PLL), but now a day's we are using hardware module divider. There are so many techniques to implement the divider. In synchronous technique it always need clock signal to trigger the system. If we use this technique we may cause some problems like clock skew, dynamic power consumption etc. But in asynchronous circuits no need of system clock signals so it doesn't have the shortcomings mentioned above. The demand for lower cost, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. The integrated synthesizers for WLAN applications at 5 GHz consume up to 25 mW in CMOS realizations but it consumes large chip area and has a narrow locking range. To overcome this we used the best published frequency synthesizer at 5 GHz but it consumes power around 9.7 mW. In order to overcome this we used dynamic latches, which are faster and consume less power compared to static divider. The TSPC and E-TSPC designs are able to drive the dynamic latch with a single clock phase and avoid the skew problems. But E-TSPC prescaler will consume 6.25 mW. To overcome this we

used a low power wideband 2/3 prescaler and wideband multimodulus 32/33/47/48 prescaler which can consume power up to 158.43 mw. Frequency dividers are also called prescaler which are used in many communication applications like frequency synthesizer, timing-recovery circuits and clock generation circuits. A prescaler is loaded at the feedback path of the synthesizer, takes signal and generates a periodic output signal and frequency. It is one of the most critical blocks in frequency synthesizer because it operates at highest frequency and consumes large power. So there must be power reduction in the first stage of prescaler which will reduce the total power consumption. So low power wideband 4/5 prescaler and a wideband multimodulus 64/65/79/80 prescaler is used in this project.
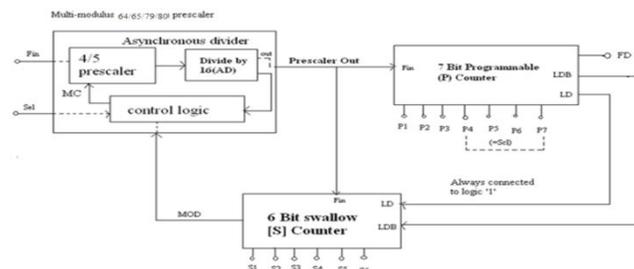

Fig.1. proposed dynamic logic multiband flexible Divider.

In this paper, a Dynamic logic multiband flexible integer – n divider based on pulse-swallow topology is proposed which uses a low power wideband 4/5 prescaler and a wideband multimodulus 64/65/79/80 prescaler as shown in Fig.1, the divider also uses an improved low power loadable bit-cell for the Swallow S-counter.

2. DESIGN CONSIDERATIONS

Basically in electronics, digital circuits and digital electronics the speed of the process depends up on the propagation delay or gate delay and length of the wire. When there is no change in input means stable and valid input then there is no change in output then we can get stable and valid output. When there is change in input it may take some time to produce the change output approximately 0.1% to 0.9%. In order to increase the speed of the processor we have to reduce the gate delay then we can get good performance. Propagation delay will increase due to temperature because of the increase in supply voltage and output load capacitance. The output of logic gate can connected to many gates due to this the delay will increase basically logic gates can have the delay of 10ns and wires may have 1ns for every 6inches. The propagation delay will decide the operating frequency of the process. In order to calculate the operating frequency we have to follow the formula mentioned below

$$F_{max} = \frac{1}{tpLH + tpHL} \qquad (1)$$

tpLH = low to high transition
tpHL = high to low transition

The total power consumption of the CMOS digital circuit is determined by the switching and short circuit power. The switching power is linearly proportional to the operating frequency and is given by the sum of switching power at each output node as in

$$P_{switching} = \sum_{i=1}^{n} f_{clk}\ C_{LiV}^2 dd \qquad (2)$$

n = number of switching nodes
fclk= clock frequency
CLi = load capacitance at the output node of the ith stage
Vdd = supply voltage

Basically the short circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by

$$P_{SC} = I_{SC} * V_{dd} \qquad (3)$$

Isc = short circuit current

The short circuit power is high in E-TSPC logic circuits than in TSPC logic circuits because TSPC logic circuits exhibit higher switching power than E-TSPC logic circuits due to high load capacitance. In E-TSPC the major problem is short-circuit power and it has merit of higher operating frequency but it consumes more power than TSPC circuit.

3. WIDEBAND 4/5 PRESCALER

The wideband single-phase clock 4/5 prescaler is used in this design and it consists of 3 D-flip-flops and 2 NOR gates as shown below
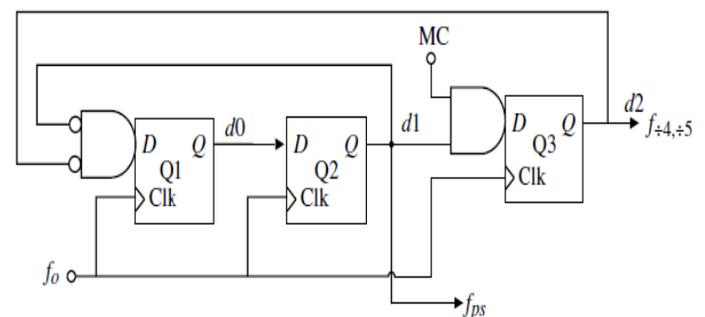

Fig.2. wideband single phase clock 4/5 prescaler

It depends on the logic value at MC. When MC = 0 the division ratio is 4 MC = 1 the division ratio is 5

A modulus control signal M is used to control the division ratio either N or N+1. When M = '0', D1 and D2 will form a divide-by-4 with q3 remaining at 'high' and NAND1 behaving like a NOT gate. When M = '1', NAND2 will behave like a NOT gate and NAND1 will output '0' when both q2 and q3 are at 'High'. Hence q1 will change from high-t0- low after 3 cycles of fclk, forming a divide-by-5.

4. DUALMODULUS 64 PRESCALER

The proposed wideband multimodulus prescaler which can divide the input frequency by 64 as shown below
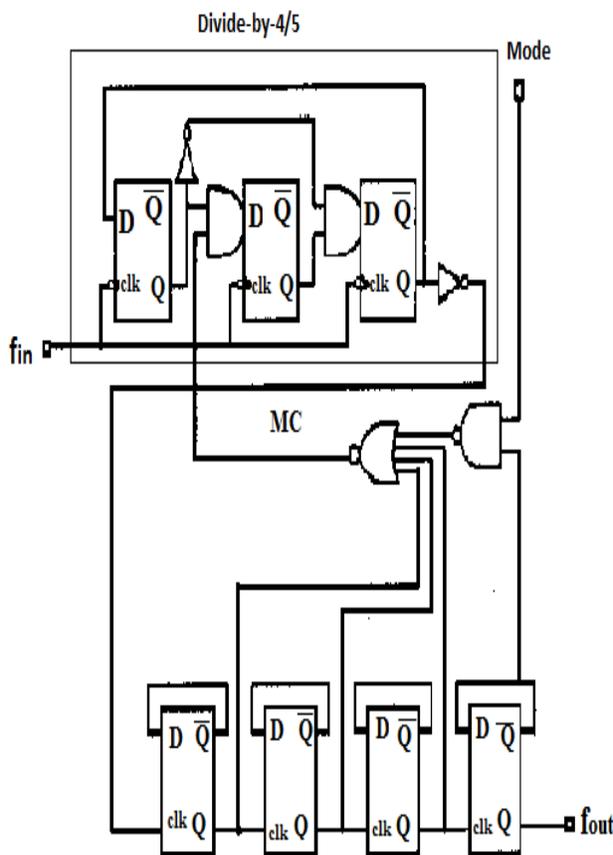
Fig.4. proposed dualmodulus 64 prescaler

The schematic of the low-voltage dual-modulus prescaler. The dual-modulus divide-by-64/65

prescaler consists of a synchronous divide-by-4/5 counter, an asynchronous divide-by-16 counter and a few static gates.

When   mode = 0   divide by 64

mode = 1   divide by 65

1) Case 1: mode = 0
If we give input as 1 i.e., reset is 1 it will resets the previous output and gives output as 0. If reset is 0 then the negated output of 4/5 prescaler is given as input to the multimodulus prescaler. The output of last DFF and MODE=0 is given as input to the NAND1, the output of NAND1 and the remaining DFF's are given as input to the NOR1. The output of NOR1 is treated as Mode Control (MC). The output of NOR1 and output of first DFF of 4/5 prescaler is given as input to the NAND2. The output of NAND2 is given as input to the second DFF of 4/5 prescaler. The output of second DFF of 4/5 prescaler and the negation of first DFF of 4/5 prescaler is given as input to the third DFF of 4/5 prescaler then it will perform the divide by 64.

2) Case 2: mode = 1
If we give input as 1 i.e., reset is 1 it will resets the previous output and gives output as 0. If reset is 0 then the negated output of 4/5 prescaler is given as input to the multimodulus prescaler. The output of last DFF and MODE=1 is given as input to the NAND1, the output of NAND1 and the remaining DFF's are given as input to the NOR1. The output of NOR1 is treated as Mode Control (MC). The output of NOR1 and output of first DFF of 4/5 prescaler is given as input to the NAND2. The output of NAND2 is given as input to the second DFF of 4/5 prescaler. The output of second DFF of 4/5 prescaler and the negation of first DFF of 4/5 prescaler is given as input to the third DFF of 4/5 prescaler then it will perform the divide by 65.

5. RESULTS AND CONCLUSION:

SIMULATED ENVIRONMENT
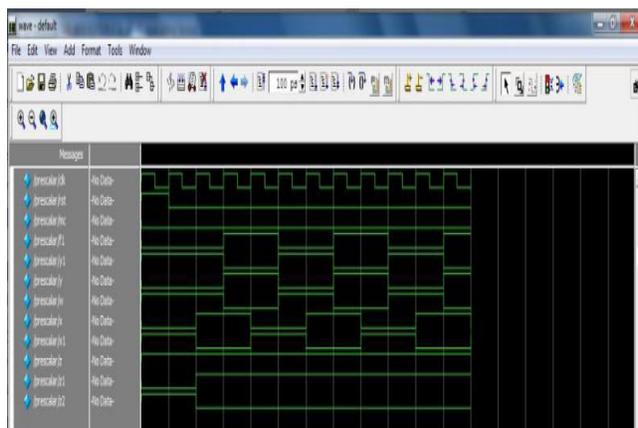

Fig.6 OUTPUT OF DIVIDE BY 4
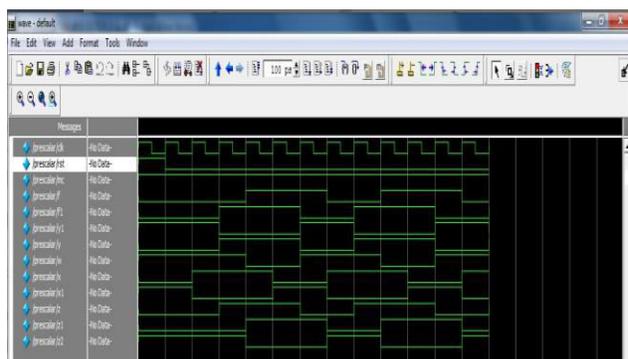

Fig .7 OUTPUT OF DIVIDE BY 5
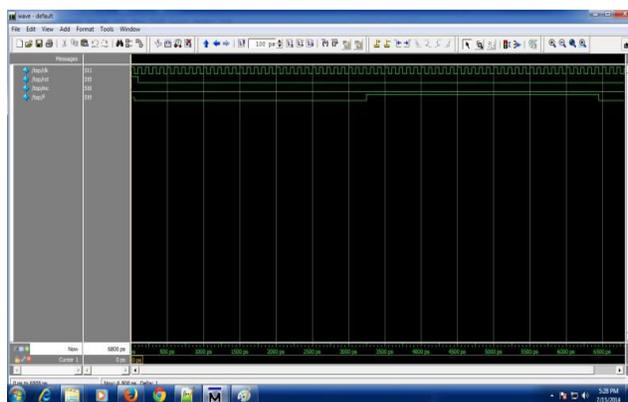
Fig.8 OUTPUT OF DIVIDE BY 64
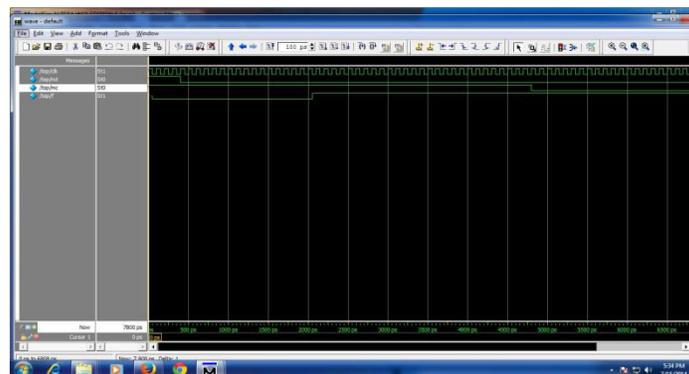
Fig.9 OUTPUT OF DIVIDE BY 65

	Total	Dynamic	Quiescent
Power (mW)	80.98	0.00	80.98

Fig.10 POWER CONSUMPTION OF 4/5
PRESCALER

CONCLUSION

In this paper, a multiband flexible divider is implemented which consist of a consist of program counter; swallow s counter and multimodulus prescaler. It is simulated by using modalism 6.4c.This type of divider is widely used in Bluetooth, Zigbee technologies which are the common wireless standards .A modified divider is also implemented in this paper by integrating p and s counters in the existing system to achieve high performance, to simplify the circuit etc. Also in the modified flexible divider existing 2/3 prescaler is replaced with modified 4/5 prescaler. By the implementation of modified divider we can achieve reduced power consumption.

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